

# PMN38EN

## N-channel TrenchMOS logic level FET

Rev. 02 — 3 October 2007

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features

- Logic level threshold
- Surface-mounted package
- Low threshold voltage
- Very fast switching

### 1.3 Applications

- Battery powered motor control
- High speed switch in set top box power supplies
- Driver FET in DC-to-DC converters
- Load switch in notebook computers

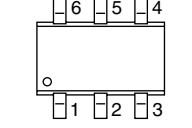
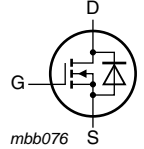
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> and <a href="#">3</a>	-	-	5.4	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	1.75	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$ ; $I_D = 2.8\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 8</a> and <a href="#">9</a>	-	38	46	mΩ

## 2. Pinning information

**Table 2. Pinning**

Pin	Symbol	Description	Simplified outline	Graphic Symbol
1	D	drain	 SOT457 (TSOP6)	 mbb076
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
PMN38EN	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

## 4. Limiting values

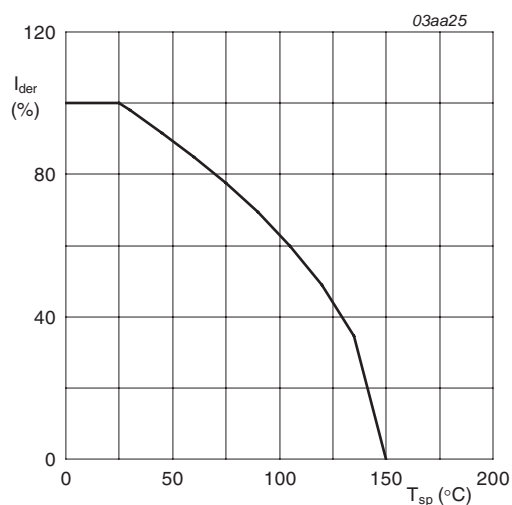
**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$T_{sp} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>	-	3.4	A
		$T_{sp} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> and <a href="#">3</a>	-	5.4	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; see <a href="#">Figure 3</a>	-	21.6	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	1.75	W
$T_{stg}$	storage temperature		-55	150	°C
$T_j$	junction temperature		-55	150	°C

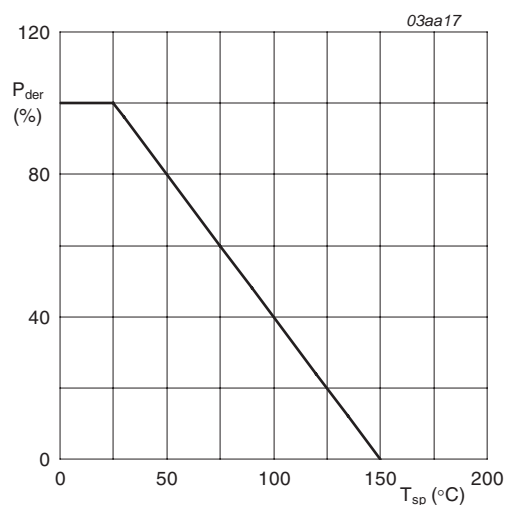
### Source-drain diode

$I_S$	source current	$T_{sp} = 25\text{ °C}$	-	1.45	A
$I_{SM}$	peak source current	$T_{sp} = 25\text{ °C}$ ; $t_p = 10\text{ }\mu\text{s}$ ; pulsed	-	5.8	A



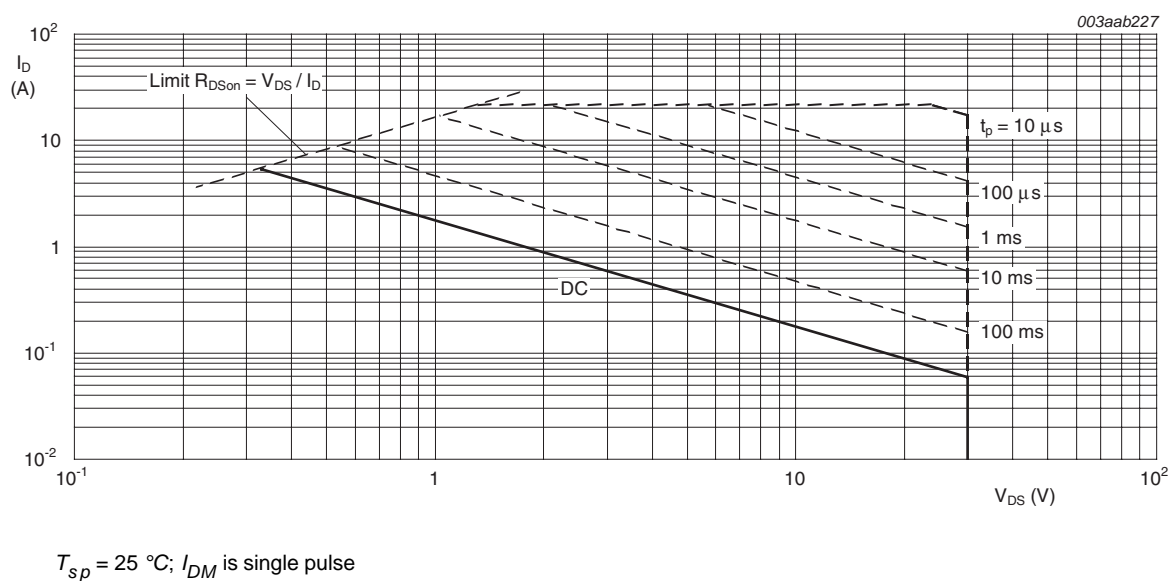
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

**Fig 1. Normalized continuous drain current as a function of solder point temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

**Fig 2. Normalized total power dissipation as a function of solder point temperature**



$T_{sp} = 25^\circ\text{C}$ ;  $I_{DM}$  is single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see <a href="#">Figure 4</a>	[1] -	-	70	K/W

[1] Mounted on a metal clad board

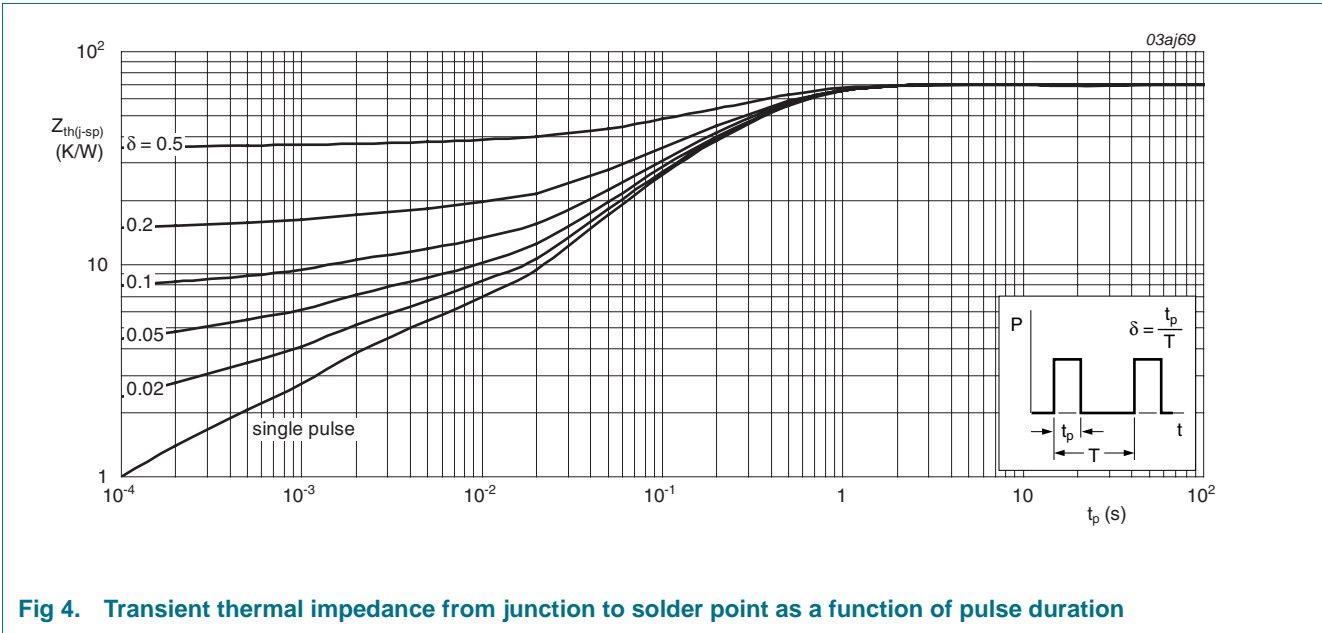


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = -55 \text{ }^\circ C$	27	-	-	V
		$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 150 \text{ }^\circ C$	0.6	-	-	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = -55 \text{ }^\circ C$	-	-	2.2	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 7</a>	1	1.5	2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	0.01	0.1	$\mu A$
		$V_{DS} = 30 V$ ; $V_{GS} = 0 V$ ; $T_j = 150 \text{ }^\circ C$	-	-	10	$\mu A$

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = +20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	10	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	10	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 3 A; T <sub>j</sub> = 150 °C	-	49.6	60.9	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 2.8 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 8</a> and <a href="#">9</a>	-	38	46	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 3 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 8</a> and <a href="#">9</a>	-	31	38	mΩ
Dynamic characteristics						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 10</a> and <a href="#">11</a>	-	6.1	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 10</a> and <a href="#">11</a>	-	1.7	-	nC
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 10</a> and <a href="#">11</a>	-	2.35	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	495	-	pF
C <sub>oss</sub>	output capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	100	-	pF
C <sub>rss</sub>	reverse transfer capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	70	-	pF
t <sub>d(on)</sub>	turn-on delay time	R <sub>G(ext)</sub> = 6 Ω; R <sub>L</sub> = 12 Ω; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C	-	14	-	ns
t <sub>r</sub>	rise time	R <sub>G(ext)</sub> = 6 Ω; R <sub>L</sub> = 12 Ω; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C	-	19	-	ns
t <sub>d(off)</sub>	turn-off delay time	V <sub>DS</sub> = 15 V; R <sub>L</sub> = 12 Ω; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C	-	28	-	ns
t <sub>f</sub>	fall time	R <sub>G(ext)</sub> = 6 Ω; R <sub>L</sub> = 12 Ω; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C	-	16	-	ns
Source-drain diode						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 1.7 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 13</a>	-	0.75	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 2.3 A; dI <sub>S</sub> /dt = 100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 30 V; T <sub>j</sub> = 25 °C	-	22	-	ns

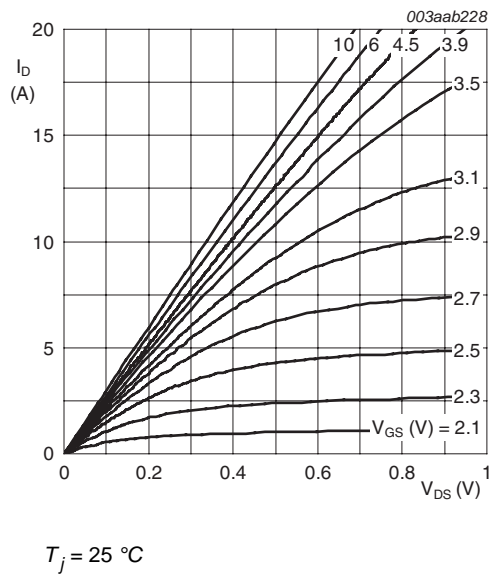


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

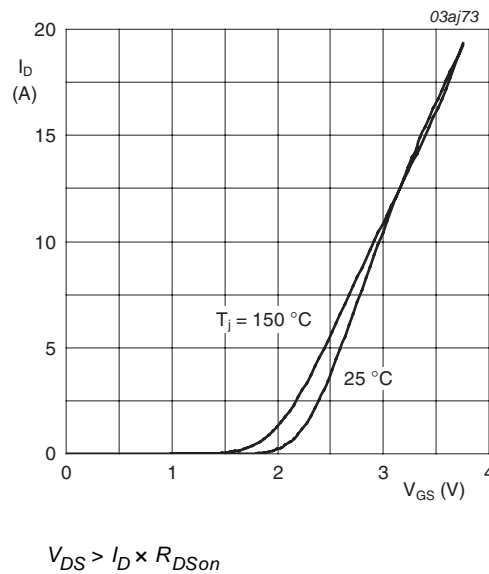


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

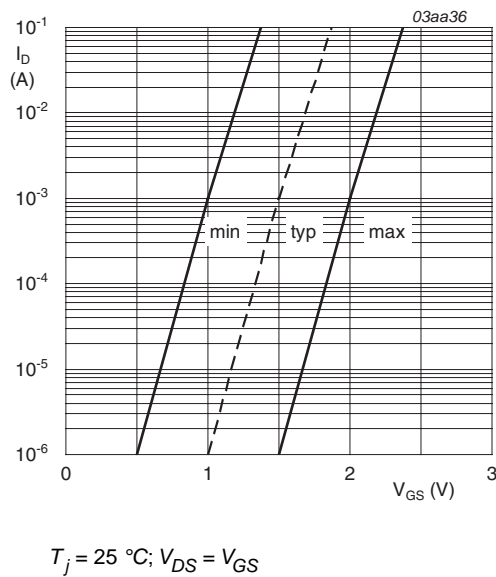


Fig 7. Sub-threshold drain current as a function of gate-source voltage

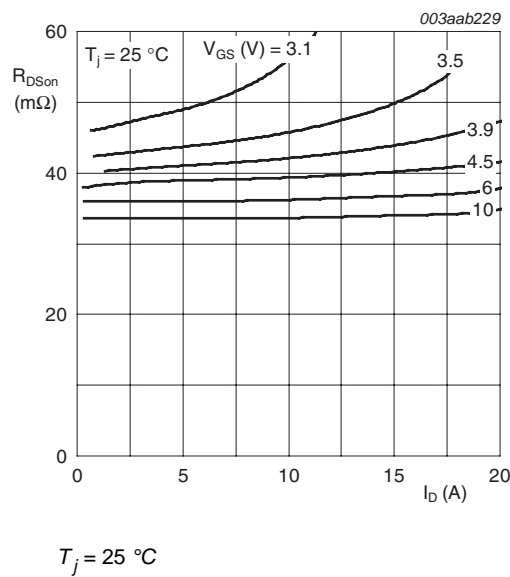


Fig 8. Drain-source on-state resistance as a function of drain current; typical values

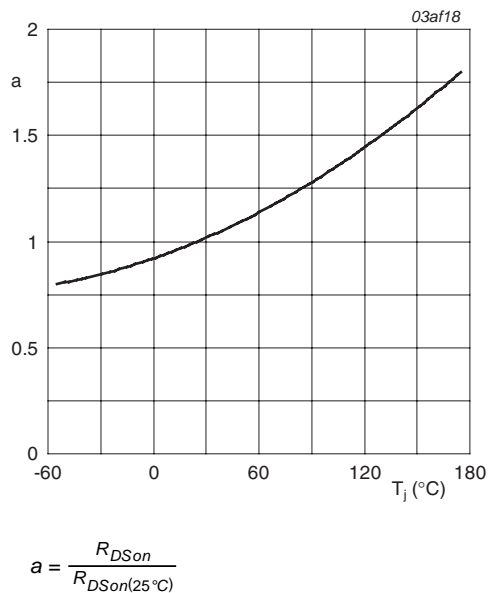


Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature

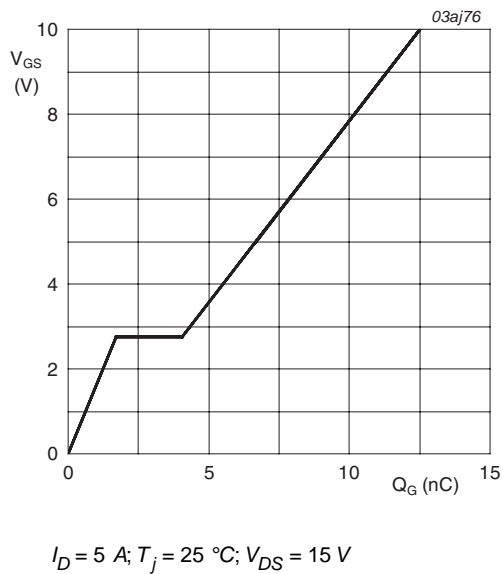


Fig 10. Gate-source voltage as a function of gate charge; typical values

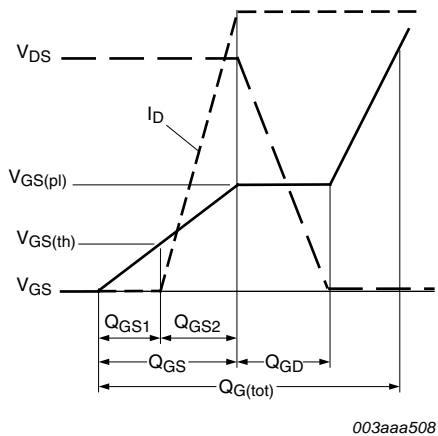


Fig 11. Gate charge waveform definitions

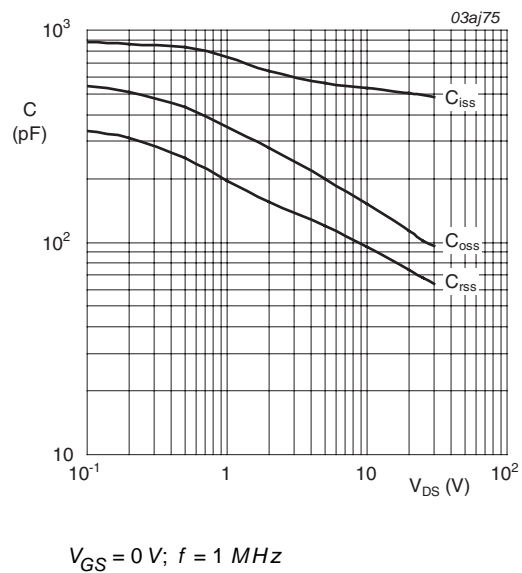


Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

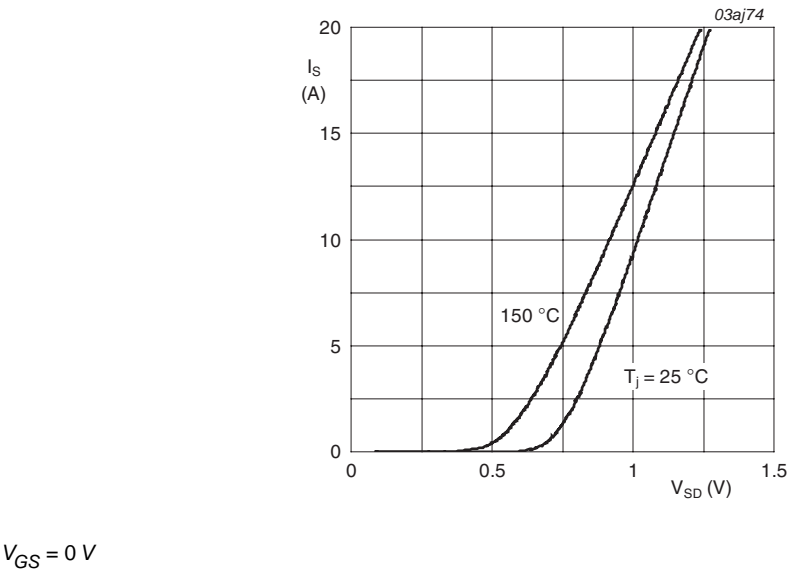


Fig 13. Source current as a function of source-drain voltage; typical values



7. Package outline

Plastic surface-mounted package (TSOP6); 6 leads

SOT457

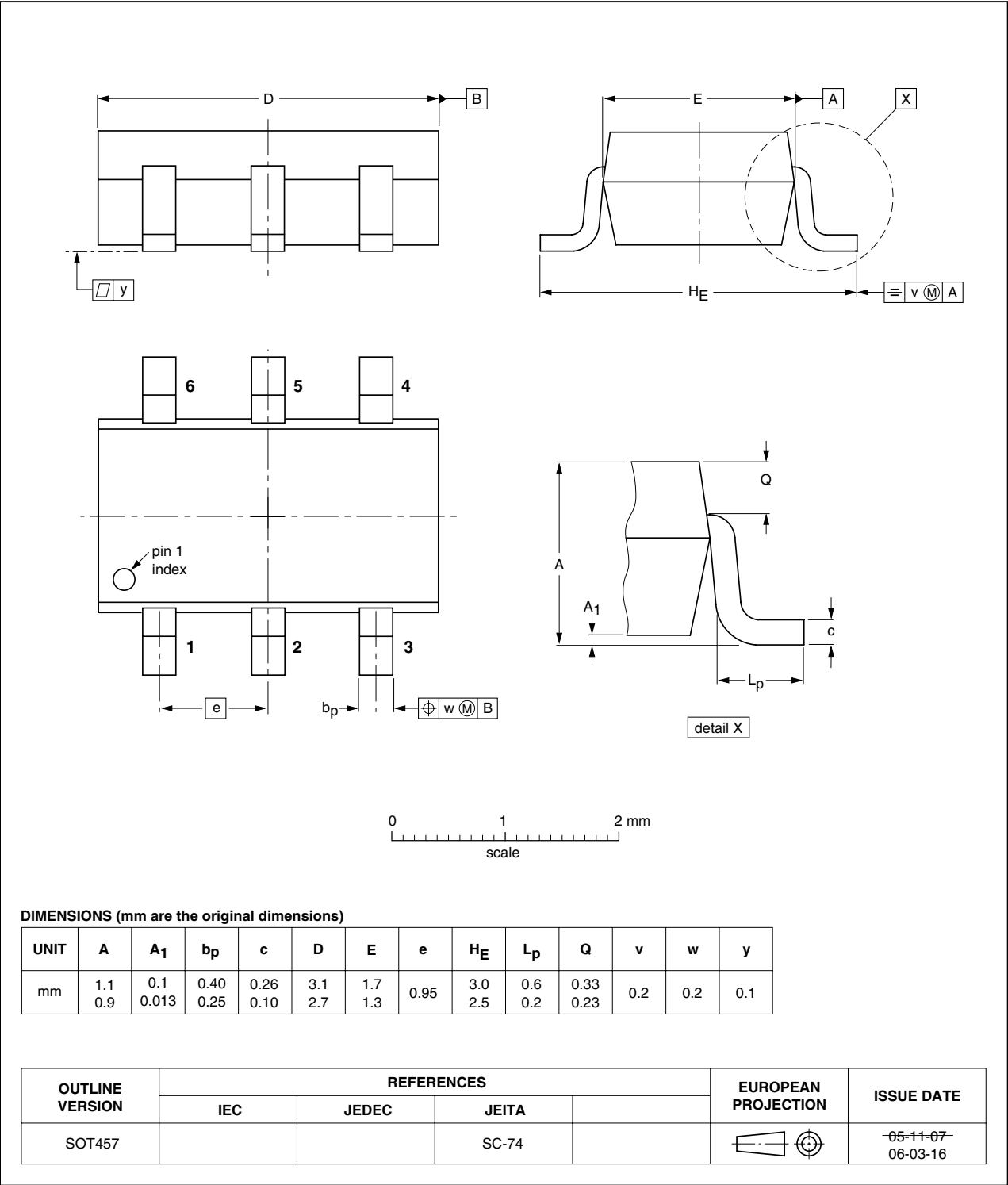


Fig 14. Package outline SOT457 (TSOP6)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMN38EN_2	20071003	Product data sheet	-	PMN38EN_1
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the company name where appropriate.</li></ul>			
PMN38EN_1	20060113	Product data sheet	-	-

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### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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