Low voltage IF I/Q transceiver — SA1638

DESCRIPTION

The SA1638 is a combined Rx and Tx IF I/Q circuit. The receive path contains an IF amplifier, a pair of quadrature down-mixers, and a pair of baseband filters and amplifiers. A second pair of mixers in the transmit path transposes a quadrature baseband input up to the IF frequency. An external VCO signal is divided down internally and buffered to provide quadrature local oscillator signals for the mixers. A further divider chain, reference divider and phase detector are provided to avoid the need for an external IF synthesizer. Rx or Tx path or the entire circuit may be powered down by logic inputs. On-board voltage regulators are provided to allow direct connection to a battery supply.

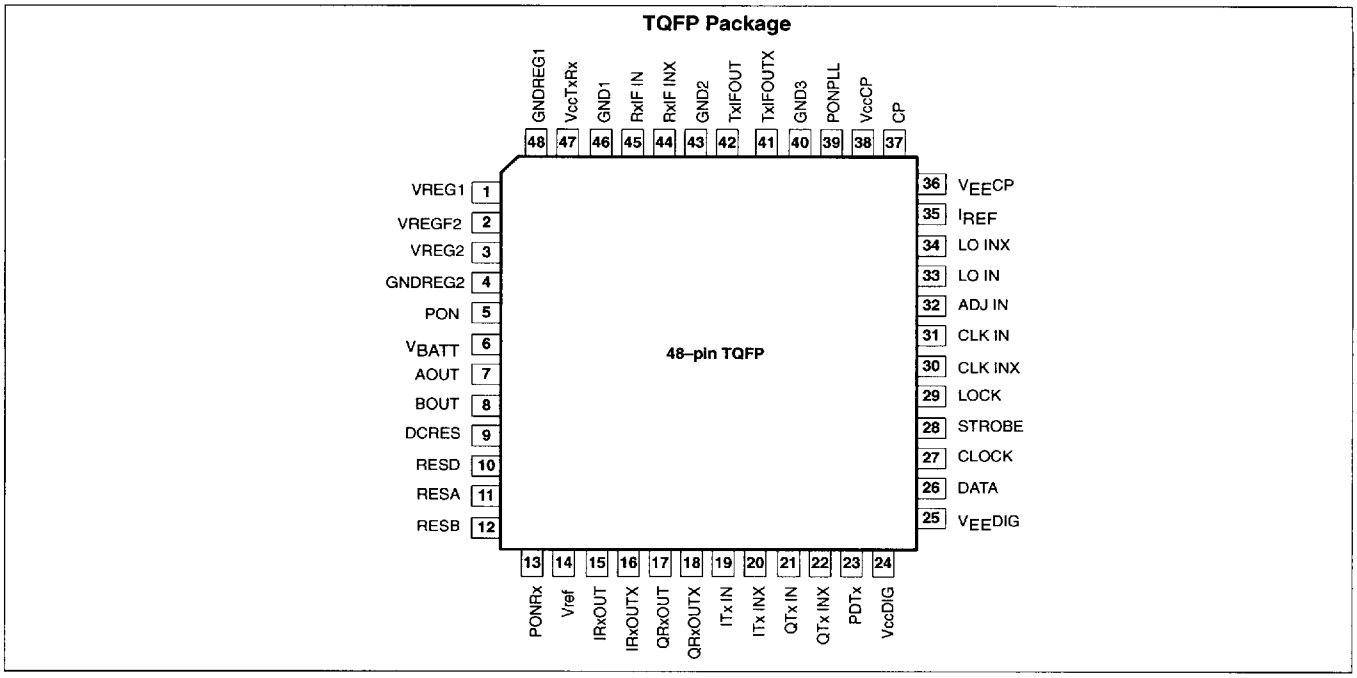
FEATURES

- Direct supply: 3.3V to 7.5V
- Two DC regulators giving 3.0V output
- Low current consumption: 14mA for Rx or 18mA for Tx
- Input/output IF frequency from 70-500MHz
- Internal IF PLL for synthesizing the local oscillator signal
- High performance on-board integrated receive filters with bandwidth tunable between 50kHz to 1MHz
- Switchable alternative bandwidth setting available to allow channel bandwidth flexibility in operation
- Designed for a widely used I and Q baseband GSM interface
- Control registers power up in a default state
- Optional DC offset trim capability to <200mV
- Only a standard reference input frequency required, choice of 13, 26, 39 or 52MHz
- Fully compatible with SA1620 GSM RF front-end

APPLICATIONS

- IF circuitry for GSM 900MHz hand-held units
- IF circuitry for PCN (DCS1800) hand-held units
- Quadrature up and down mixer stage

PIN CONFIGURATION



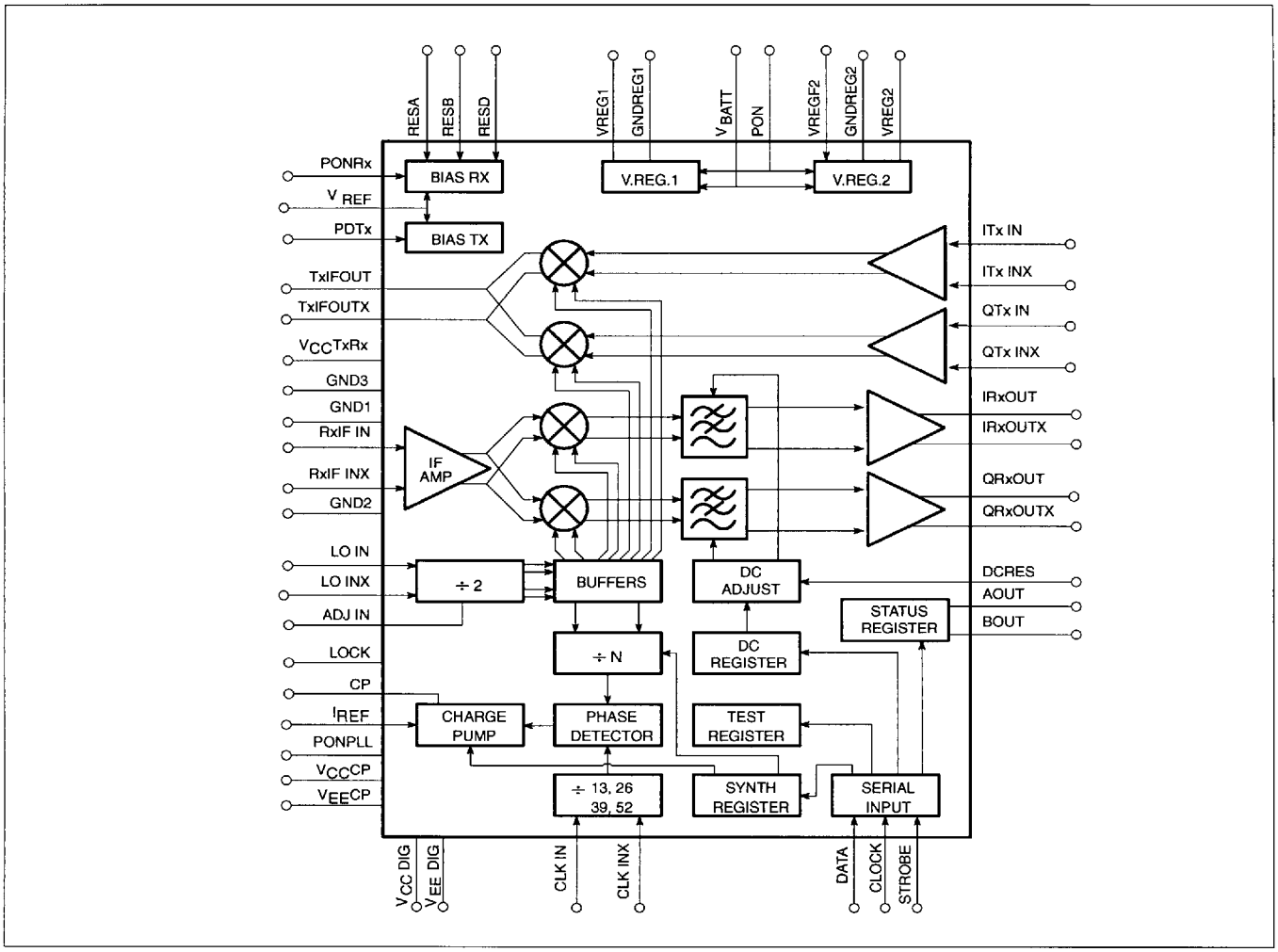
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (TQFP)	-40 to +85°C	SA1638BE	1706B

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXXX}	Supply voltages	2.7 to 5.5	V
$V_{CC}CP$	Charge pump supply voltage	2.9 to 5.5	V
V_{BATT}	Battery voltage	3.3 to 7.5	V
T_A	Operating ambient temperature range	-40 to +85	°C

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	VREG1	Output voltage of regulator 1
2	VREGF2	Feedback of regulator 2
3	VREG2	Output voltage of regulator 2
4	GNDREG2	Ground of regulator 2
5	PON	Power-on input for voltage regulators 1 and 2 (active high)
6	V_{BATT}	Input voltage for regulators 1 and 2
7	AOUT	Control output (for SA1620 attenuation select A pin)
8	BOUT	Control output (for SA1620 attenuation select B pin)
9	DCRES	Reference resistor for DC offset circuit
10	RESD	Additional external current defining resistor for filters
11	RESA	Principal external current defining resistor for filters
12	RESB	Principal external current defining resistor for filters
13	PONRx	Power-on input for Rx (active high)
14	V_{REF}	Reference voltage
15	IRxOUT	In-phase differential receive baseband output
16	IRxOUTX	In-phase differential receive baseband output
17	QRxOUT	Quadrature differential receive baseband output
18	QRxOUTX	Quadrature differential receive baseband output
19	ITx IN	In-phase differential transmit baseband input
20	ITx INX	In-phase differential transmit baseband input
21	QTx IN	Quadrature differential transmit baseband input
22	QTx INX	Quadrature differential transmit baseband input
23	PDTx	Power-on for transmitter (active low)
24	V_{CC}DIG	Digital circuit supply
25	V_{EE}DIG	Digital ground
26	DATA	Serial data input
27	CLOCK	Serial clock input
28	STROBE	Serial strobe input
29	LOCK	Test control/synthesizer lock indicator
30	CLK INX	Differential reference divider input
31	CLK IN	Differential reference divider input
32	ADJ IN	Used for test only
33	LO IN	Differential LO input
34	LO INX	Differential LO input
35	I_{REF}	Reference current for charge pump
36	V_{EE}CP	Charge pump ground
37	CP	Charge pump output
38	V_{CC}CP	Charge pump circuit supply
39	POnPLL	Power-on input for synthesizer circuits (active high)
40	Gnd3	Ground (internal connection to GND1 and GND2)
41	TxIFOUTX	Differential transmit IFoutput
42	TxIFOUT	Differential transmit IFoutput
43	GND2	Ground (internal connection to GND1 and GND3)
44	RxIF INX	Differential receive IF input
45	RxIF IN	Differential receive IF input
46	GND1	Ground (internal connection to GND2 and GND3)
47	V_{CC}TxRx	Transmit and receive circuits supply voltage (also feedback of Regulator 1)
48	GNDREG1	Ground of regulator 1
NOTE: There are no ESD protection diodes at Pins 41 and 42. Thus, open collector outputs may have increased DC voltage or higher AC peak voltage.		

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	-0.3 to +6.0	V
V_{BATT}	Battery voltage	-0.3 to +8.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CCXX}+0.3)	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	300	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}. 48-pin TQFP: θ_{JA} = 67°C/W.

Voltage Regulators

T_A = 25°C, P_{ON} = 3V, P_{ON}RX = 0V, PDTX = 3V, PDPLL = 0V, V_{BATT} = 3.3V, I_{LOAD} = 15mA, V_{REG}1 connected to V_{CC}TxRx, V_{REG}2 connected to V_{REG}F2; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
$V_{REG}1$, $V_{REG}2$	Nominal V_{OUT}		2.85		3.15	V
V_{BATT}			3.3		7.5	V
I_{LOAD}[1]	V_{REG}1 or V_{REG}2				30	mA
I_{BATT}		I_{LOAD} = 0mA		7		mA
$I_{BATT\ PD}$	P_{ON} = 0V	I_{LOAD} = 0mA			75	µA
$C_{REG}1$[2]	V_{REG}1 cap load		0.1		1000	µF
$C_{REG}2$[2]	V_{REG}2 cap load		0.1		500	µF
BW	Bandwidth		100			kHz
LINEREG	Line regulation	DC, V_{BATT} = 3.3V to 7.5V	–0.4		0.4	%
LOADREG	Load regulation	I_{LOAD} = 15mA to 30mA	–5		5	%

NOTES:
1. At $T_j \geq$ 150°C a thermal switch reduces the output current.
2. Recommended load capacitors: In every case $C_{REG}1$ = $C_{REG}2$ = 100nF to ground with series resistance ≤0.1Ω. Additional capacitor optional ≤1000µF with series resistance ≤5Ω.
3. Feedthrough attenuation from the logic input P_{ON} to the outputs V_{REG}1 and V_{REG}2: ≥40dB.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}XXX$ = PONRx = PONPLL = +3V; $V_{EE}XXX$ = GND1 = GND2 = GND3 = PDTx = 0V; T_A = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current					mA
	Rx and IF synthesizer active	PONRx = PONPLL = PDTx = Hi		14	17	
	Tx and IF synthesizer active	PONRx = PDTx = Low; PONPLL = Hi		18	21	
	Power-down mode	PONRx = PONPLL = Low; PDTx = Hi		.007		
V_{REF}	Reference voltage	Generated internally		1.5		V
IV_{REF}	V_{REF} I_{SINK} I_{SOURCE}				100 250	µA
Digital inputs (PDTx, P_{ON}Rx, P_{ON}PLL, P_{ON})						
V_{IH}	High level input voltage range		2.0		V_{CC}TxRx	V
V_{IL}	Low level input voltage range		0		0.8	V
Digital inputs (Clock, Data, Strobe)						
V_{IH}	High level input voltage range		0.7 × V_{CC}DIG		V_{CC}Dig	V
V_{IL}	Low level input voltage range		0		0.3 × V_{CC}DIG	V
Digital outputs (LOCK, AOUT, BOUT)						
V_{OH}	Output voltage HIGH	I_O = -2mA	V_{CC}DIG – 0.4			V
V_{OL}	Output voltage LOW	I_O = 2mA			0.4	V

AC ELECTRICAL CHARACTERISTICS

$V_{CC}XXX$ = P_{ON}Rx = P_{ON}PLL =+3V; $V_{EE}XXX$ = GND1 = GND2 = GND3 = PDTx = 0V; f_{LO} = 800MHz; T_A = 25°C unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
IF Transmit Modulator						
BW	Input modulation bandwidth	200Ω source impedance		2		MHz
	Input signal amplitude	Centered on V_{REF} (V)		V_{REF}/2	V_{REF}/1.75	V_{PK}
THD	Total harmonic distortion[1]	I ITxIn I = I ITxInX I = I QTxIn I = I QTxInX I = ±V_{REF}/2		-50		dBc
R_{INTx}	Input resistance	Between pins: ITxIn and ITxInX or QTxIn and QTxInX	10			kΩ
C_{INTx}	Input capacitance	At ITxIn, ITxInX, QTxIn, QTxInX			10	pF
	Output saturation limit				V_{CC}TxRx-0.3	V
	DC output current	At pins TxIFOUT and TxIFOUTX		2.0		mA
	Offset between DC output currents	At pins TxIFOUT and TxIFOUTX		tbd		µA
	Output current	I ITxIn I = I ITxInX I = I QTxIn I = I QTxInX I = ±V_{REF}/2		0.25		mA_{RMS}
S_{LO}	LO suppression	I ITxIn I = I ITxInX I = I QTxIn I = I QTxInX I = ±V_{REF}/2		-36		dB
SSB	Sideband suppression	I ITxIn I = I ITxInX I = I QTxIn I = I QTxInX I = ±V_{REF}/2		-42		dB
	Equivalent input noise	at 10kHz		tbd		nV/√Hz
t_{ON}	Turn ON time			5		µs
t_{OFF}	Turn OFF time			5		µs

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
IF Receiver						
RInRx	Differential input impedance	f_{IN} = 400MHz		5		kΩ
ROutRx	Output impedance			1		kΩ
	Output common mode voltage			V_{REF}		V
f3dB	Low pass filter -3dB bandwidth	68kΩ resistor between pins RESA and RESB	72	80	88	kHz
	Low pass filter attenuation: 200kHz 400kHz 600kHz 6.5MHz 13.0MHz	68kΩ external resistor between RESA and RESB		 34 64 80 >80 >80		dB
VG	Voltage gain	Differential output PD into GSM baseband relative to 1200Ω source EMF	43	50	58	dB
NF	Noise figure at minimum gain	1200Ω source and external matching resistor and inductor		5.8		dB
	Channel matching: Gain Phase			 1.0 5.0		 dB degrees
	Output DC offset[2]	Differential		200		mV
P_{-1dB}	Input 1dB compression point: In band 200kHz 400kHz 600kHz	1200Ω source EMF		 -52 -41 -41 -41		dBV
t_{ON}	Turn-On time	POnRx = V_{EE}		5		µs
t_{OFF}	Turn-off time	POnRx = V_{EE}		5		µs
IF Synthesizer						
f_{LO}	Local oscillator input frequency range		140		1000	MHz
Z_{LOIN}	Differential input impedance	Between pins LO_{IN} and $LO_{IN}X$		tbd		Ω ll pF
	LO input range	Referred to 50Ω	300		550	mV_{P-P}
	Programmable divider: Division range Step size		64	 1	511	
f_{CLK}	Reference clock input frequency			13, 26, 39 or 52		MHz
Z_{CLKIN}	Differential input impedance	Between pins ClkIn and ClkInX		10 ll 1.0		kΩ ll pF
	CLK input sensitivity	Referred to 50Ω		200		mV_{P-P}
I_{REF}	Charge pump input reference current			31.2		µA
$\lvert I_{CP} \rvert$	Charge pump output current: C0...C2 = 000 C0...C2 = 111 Step size	I_{REF} =31.2µA, $V_{CP} = V_{CC}CP/2$		 0.5 1.0 0.071		mA
$\frac{\Delta I_{CP}}{I_{CP}}$	Relative output current variation[3]	I_{REF} =31.2µA			±10	%
ΔI_{CP_M}	Output current matching[4]	I_{REF} =31.2µA, $V_{CP} = V_{CC}CP/2$			±50	µA

NOTES:

1. Parameter measured relative to modulation sideband amplitude.
2. After programming the DC offset register for minimum offset.
3. The relative output current variation is defined thus: $\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{\lvert(I_2 + I_1)\rvert}$; with V_1 = 0.3V, $V_2 = V_{CC}CP - 0.3V$ (see Figure 1).
4. The output current matching is measured when both (positive current and negative current) sections of the output charge pumps are on.

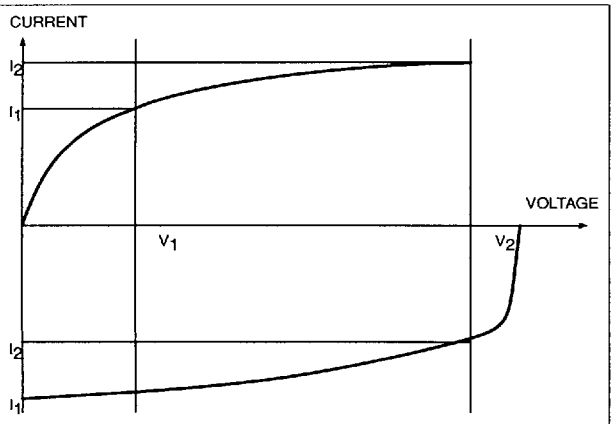


Figure 1. Relative Output Current Variation

FUNCTIONAL DESCRIPTION

Serial Programming Input

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program the counter ratios, charge pump current, status- and DC-offset register, mode select and test register. The programming data is structured into two 21-bit words; each word includes 4 chip address bits and 1 subaddress bit. Figure 2 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the value of the subaddress bit the data is latched into different working registers. Table 1 shows the contents of each word.

Default States

Upon power up (V_{CC}DIG is applied) a reset signal is generated, which sets all registers to a default state. These default states are shown in Table 1.

Reference Divider

The reference divider can be programmed to four different division ratios (:13, :26, :39, :52), see registers r0, r1; default setting: divide by 13.

Main Divider

The external VCO signal, applied to the LO_{IN} and $LO_{IN}X$ inputs, is divided by two and then fed to the main divider (:N). The main divider is a programmable 9 bit divider, the minimum division ratio is divide by 64. The division ratio is binary coded and set in the registers n0 to n8. The default setting is a divide by 400.

At the completion of a main divider cycle, a main divider output is generated which will drive the phase detector.

Phase Detector

The phase detector is a D-type flip-flop phase and frequency detector shown in Figure 3. The flip-flops are set by the negative edges of the output signals of the dividers. The rising edge of the signal L will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps.

A source current from the charge pump indicates the VCO frequency will be increased; a sink current indicates the VCO frequency will be decreased.

Current Setting

The charge pump current is defined by the current set between the pin I_{REF} and V_{SS}. The current value to be set there is 31.2µA. This current can be set by an external resistor to be connected between the pin I_{REF} and V_{SS}. The typical value R_{EXT} (current setting resistor) can be calculated with the formula

$$R_{EXT} = \frac{V_{CC}CP - 1.4V}{31.2\mu A}$$

The current can be set to zero by connecting the pin I_{REF} to V_{CC}CP.

Charge Pumps

The charge pumps at pin CP are driven by the phase dectector and the current value is determined by the binary value of the charge pumps register CN = c0, c1, c2, default 1mA. The active charge pump current is typically:

$$|I_{CP}| = CN \cdot 71\mu A + 500\mu A$$

Lock Detect

The output LOCK is H when the phase detector indicates a lock condition. This condition is defined as a phase difference of less than ±1 cycle on the reference input CLK_{IN}, $CLK_{IN}X$.

Test Modes

The LOCK output is selectable as a test output. Bits x0, x1 control the selection, the default setting is normal lock output as described in the Lock detect section. The selection of a Bit x0, x1 combination has a twofold effect: First it routes a divider output signal to the LOCK pin, second it disables mixer stages in the transmit path:

x0	x1	signal at LOCK pin	Transmit Mixer	
			I-mixer	Q-mixer
0	0	normal lock detect	on	on
1	0	CLK_{IN} divided by reference divider ratio	off	on
0	1	LOIN divided by 2 * (main divider ratio)	on	off
1	1	main divider output, that goes to the phase detector	off	off

Power Down Modes

There are 4 power-on pins in the SA1638: P_{ON}, P_{ON}Rx, P_{ON}Tx, P_{ON}PLL.

P_{ON} = H powers up both voltage regulators $V_{REG}1$ and $V_{REG}2$. P_{ON} should be set to L, if these internal voltage regulators are not to be used.

P_{ON}Rx = H powers up the receiver part.

P_{ON}Tx = L powers up the transmitter part.

P_{ON}PLL = H powers up the synthesizer part. As it also powers up the first divide by 2 stage for generating the 0/90 degree phase shifted signals for the transmit and receive mixers, it also has to be set H if either the transmit part or the receive part is used. P_{ON}PLL = L powers down the dividers, resets the phase detector and disconnects the current setting pin I_{REF}. In P_{ON}PLL = L mode, the values in the serial input registers are still kept and the part still can be reprogrammed.

Table 1. Definition of SA1638 Serial Registers

First data word: (shown with default values)

Address SA1638				Sub Adr	N-Divider									Ref ÷ Reg		Charge-Pump			Synth Test	
MSB																				LSB
a0	a1	a2	a3	sa	n0	n1	n2	n3	n4	n5	n6	n7	n8	r0	r1	c0	c1	c2	x0	x1
1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	1	1	1	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 0 for first data word
N-Divider:	9 bits, n0...n8, values 64 (00100 0000) to 511 (111111111) allowed for IF-choice, default 400
Reference Divider Register:	2 bits, r0...r1, 00 = ÷13, 01 = ÷26, 10 = ÷39, 11 = ÷52. Default: 00
Charge-Pump Register:	3 bits, c0...c2, Binary current setting factor for charge pumps, values 000 = minimum current to 111 = maximum current, default maximum charge pump current
Synthesizer-Test Register:	2 bits, x0...x1, default 00 00 lock detect at LOCK pin 10 reference signal divided by the reference divider ratio at LOCK pin 01 main input signal divided by 2 × (main divider ratio) at LOCK pin 11 main divider output signal going to the phase detector at LOCK pin

Second data word: (shown with default values)

Address SA1638				Sub Adr	Status Reg	DC Offset Register								Mode Select Register						
						I-Channel					Q-Channel									
MSB																				LSB
a0	a1	a2	a3	sa	s0	s1	i0	i1	i2	i3	q0	q1	q2	q3	t0	t1	t2	t3	t4	t5
1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 1 for second data word
Status Register:	2 bits, s0...s1, controls gain/attenuation settings of SA1620 data sheet, see Table 4, Gain Control Logic for LNA1 and LNA2 of the SA1620 data sheet.
DC Offset Register:	4 bits per channel, i0...i3 and q0...q3, no correction as default i0 and q0 switches offset polarity, 0 to lower voltage, 1 to higher voltage il...i3 and q1...q3, 000 no correction to 111 max. correction enabled
Mode Select Register:	6 bits, t0...t5, 000000 = normal GSM-Operation as default 0xxxxx = Rx internal path AC coupled 1xxxxx = Rx internal path DC coupled x0xxxx = Rx LO input applied x1xxxx = Rx LO input replaced by DC offset xx00xx = LLL on xx01xx = LLL on with medium external tune (ADJ IN) xx10xx = LLL off xx11xx = LLL on with fine external tune (ADJ IN) xxxx00 = Rx LP filter 3dB BW = 80kHz (GSM) xxxx11 = Rx LP filter 3dB BW = 580kHz

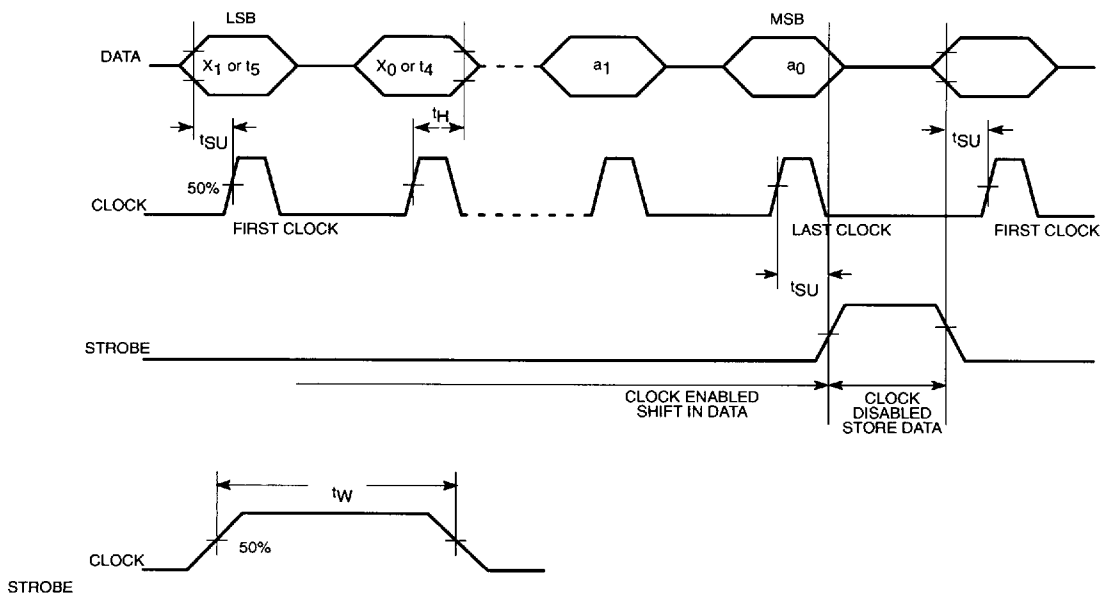


Figure 2. Serial Input Timing Sequence

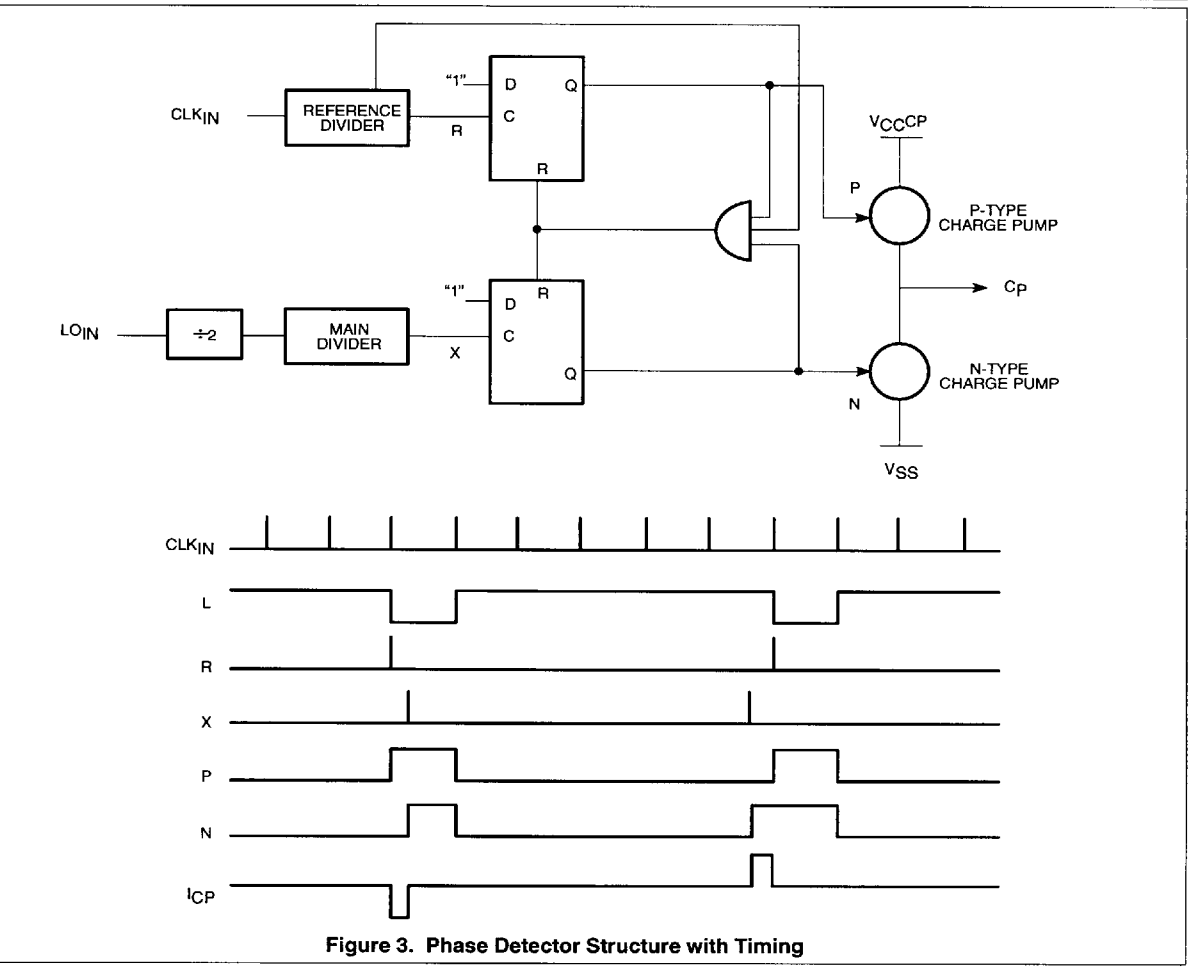
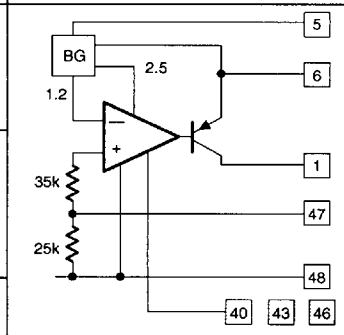
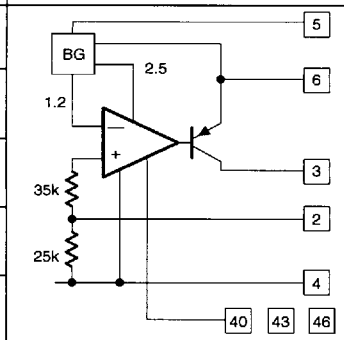
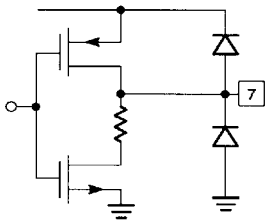
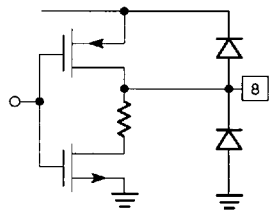
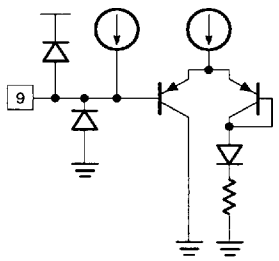
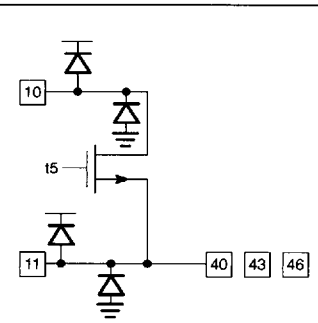
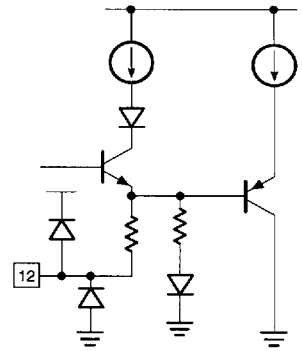
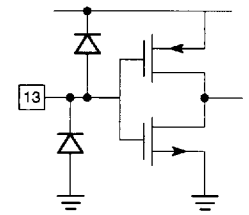
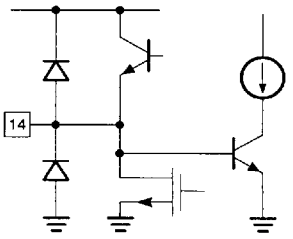
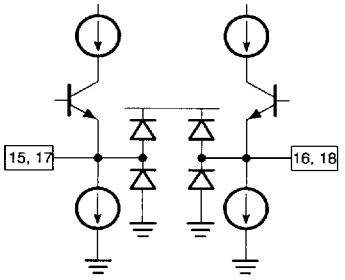


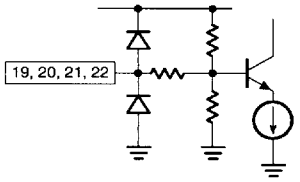
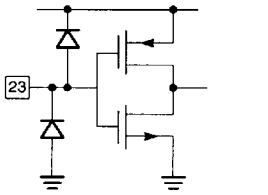
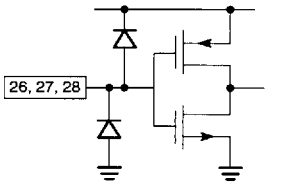
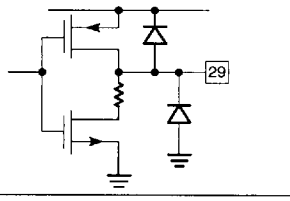
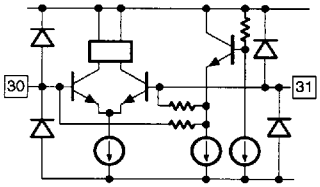
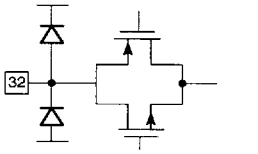
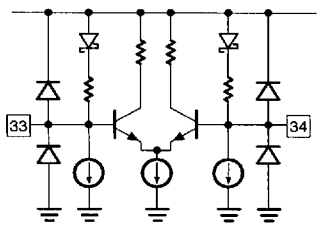
Figure 3. Phase Detector Structure with Timing

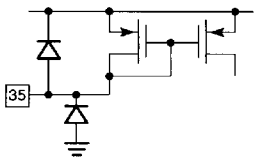
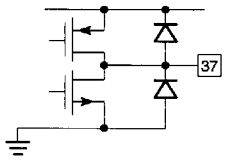
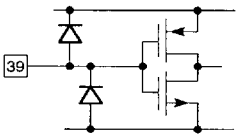
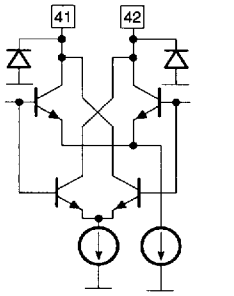
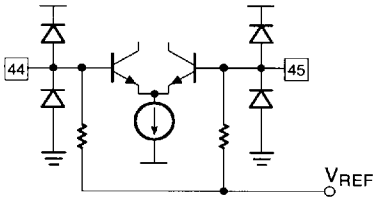
PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
47	$V_{CC}TxRx$	3.0	
48	$GND_{REG}1$	0.0	
1	$V_{REG}1$	3.0	
2	$V_{REG}F2$	3.0	
3	$V_{REG}2$	3.0	
4	$GND_{REG}2$	0.0	
5	P_{ON}	3.3	
6	V_{BATT}	3.3	
7	A_{OUT}	3.0	
8	B_{OUT}	3.0	
9	DC_{RES}	1.6	

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
10	RES_D	0.05	
11	RES_A	0.00	
12	RES_B	0.05	
13	$P_{ON}Rx$	3.0	
14	V_{REF}	1.5	
15	IRX_{OUT}	1.5	
16	$IRX_{OUT}X$	1.5	
17	QRX_{OUT}	1.5	
18	$QRX_{OUT}X$	1.5	

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
19	ITX_{IN}	1.5	
20	$ITX_{IN}X$	1.5	
21	QTX_{IN}	1.5	
22	$QTX_{IN}X$	1.5	
23	PdTx	0.0	
24	$V_{CC}DIG$	3.0	
25	$V_{EE}DIG$	3.0	
26	DATA		
27	CLOCK		
28	STROBE		
29	LOCK		
30	CLK_{IN}	2.0	
31	$CLK_{IN}X$	2.0	
32	ADJ_{IN}	2.0	
33	LO_{IN}	2.0	
34	$LO_{IN}X$	2.0	

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
35	I_{REF}	1.6	
36	$V_{EE}CP$	0.0	
37	CP		
38	$V_{CC}CP$	3.0	
39	$P_{ON}PLL$	3.0	
40	GND3	0.0	
41	$TXIF_{OUT}X$	OPEN COLLECTOR	
42	$TXIF_{OUT}X$	OPEN COLLECTOR	
43	GND2	0.0	
44	$RxIF_{IN}X$	1.5	
45	$RxIF_{IN}$	1.5	
46	GND1	0.0	
47	$V_{CC}TxRx$	3.0	
48	$GND_{REG}1$	0.0	

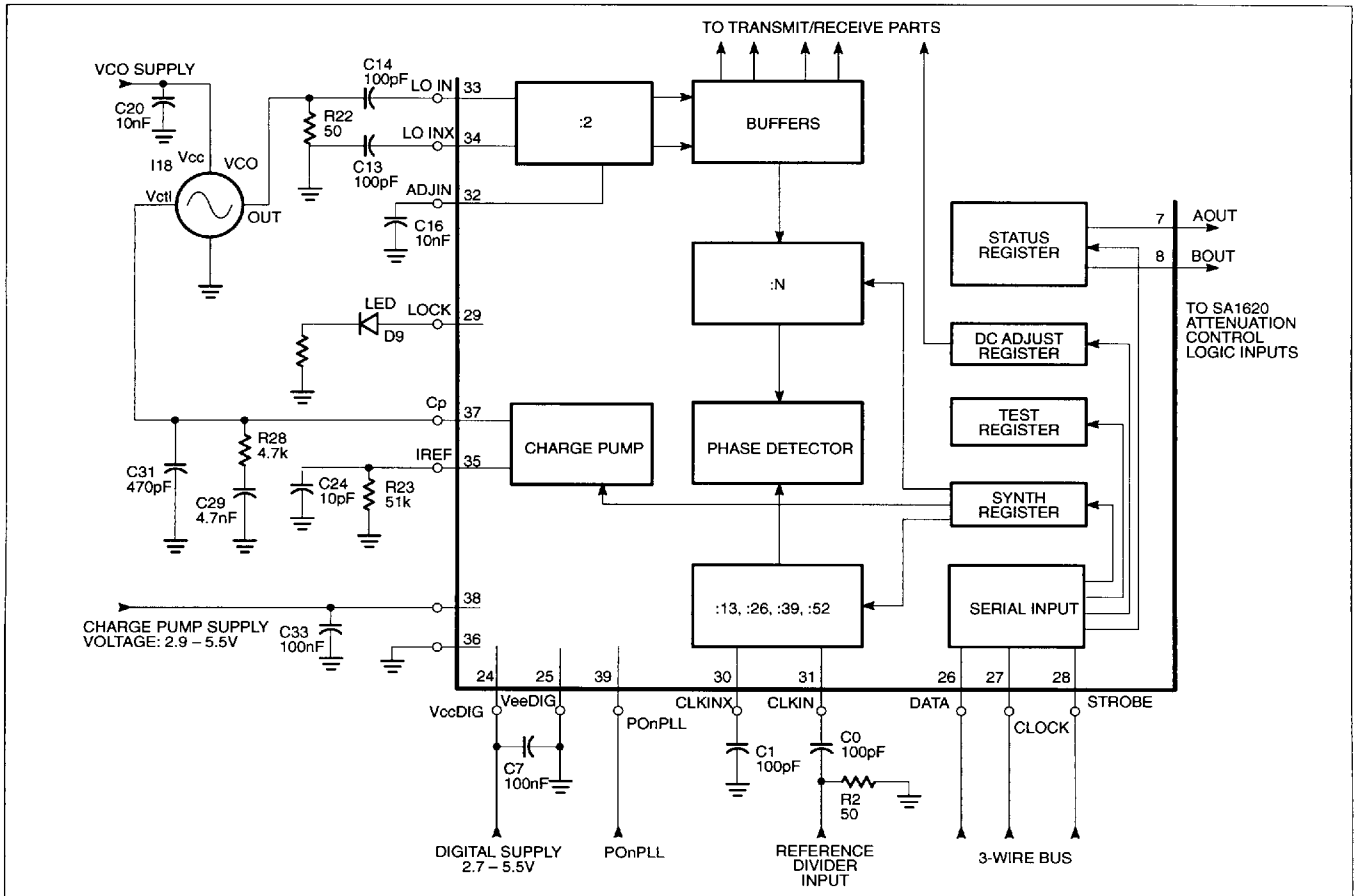


Figure 4. Recommended Application of the Synthesizer Part of SA1638

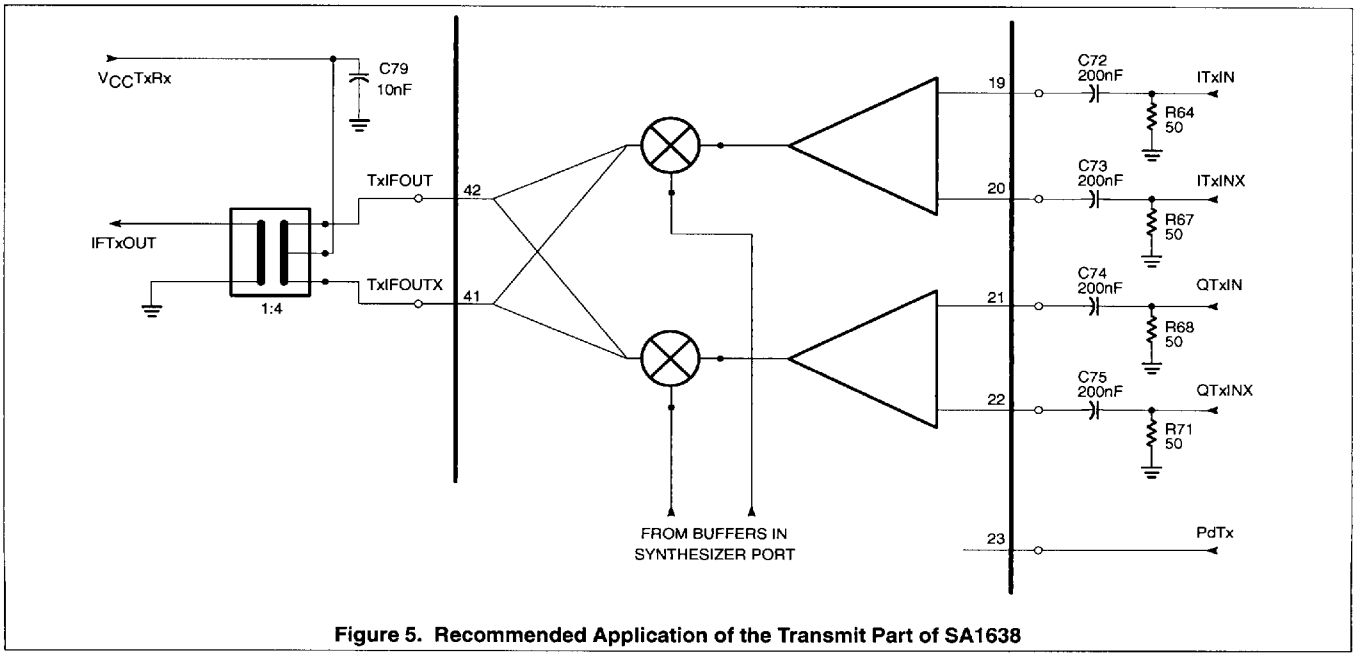


Figure 5. Recommended Application of the Transmit Part of SA1638

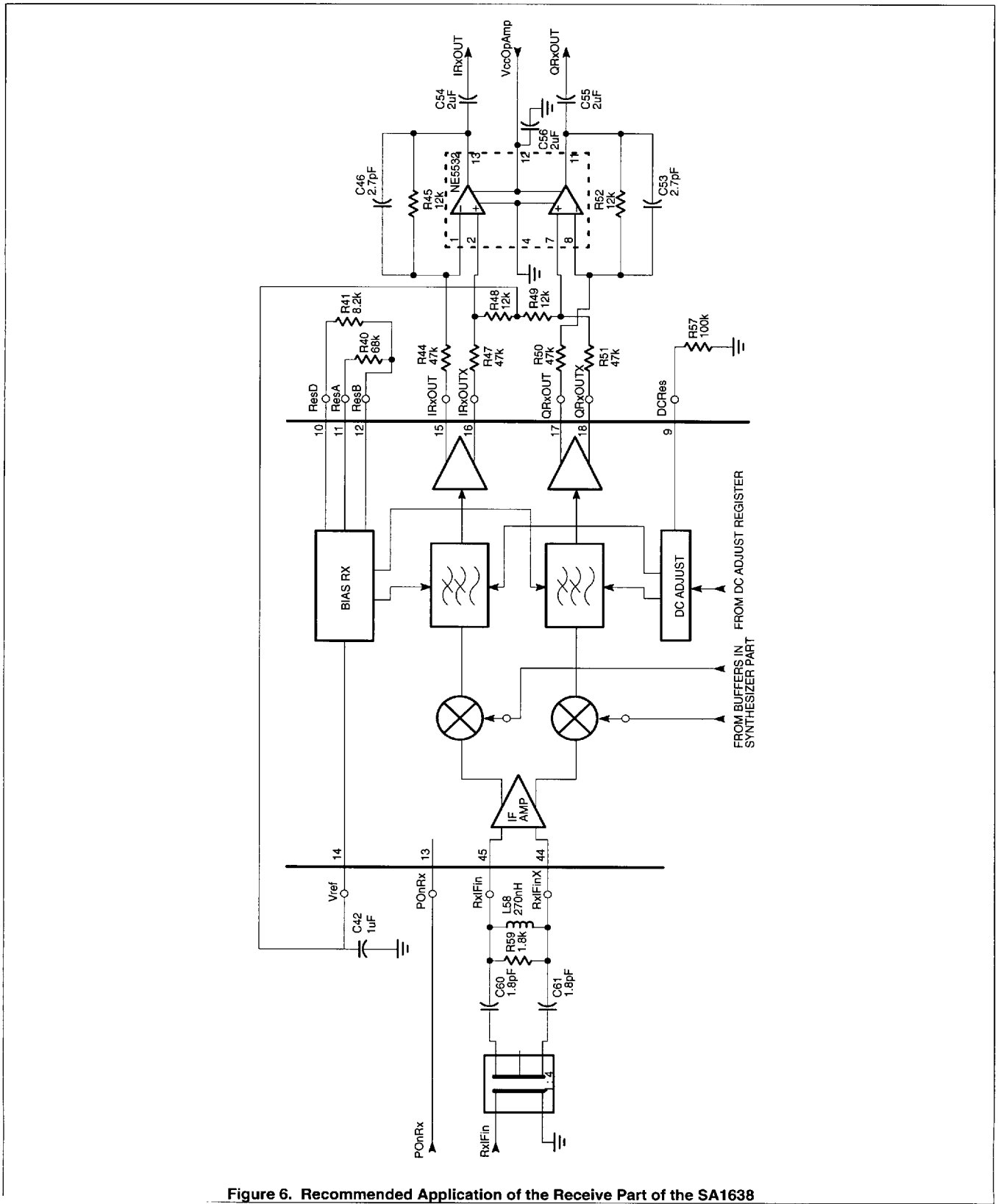
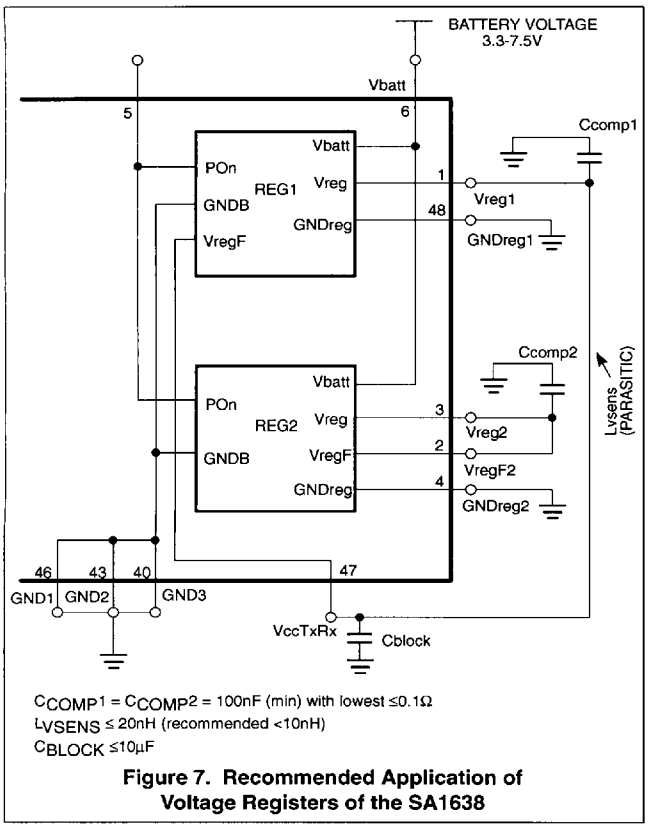


Figure 6. Recommended Application of the Receive Part of the SA1638



$C_{COMP1} = C_{COMP2}$ = 100nF (min) with lowest ≤0.1Ω
L_{VSENS} ≤ 20nH (recommended <10nH)
C_{BLOCK} ≤10µF

Figure 7. Recommended Application of Voltage Registers of the SA1638

Overview of Dual GSM/PCN Architecture

The SA1620 RF front-end and SA1638 IF transceivers form a dual conversion architecture which uses a common IF and standard I/Q baseband interface for both transmit and receive paths. This approach avoids the screening difficulties of direct modulation in the transmit direction and the mass production and practical performance issues related to direct conversion in the receive direction. The time division multiplex nature of the GSM system permits integration of the transmit and receive functions together on the one RF and one IF chips. This simplifies the distribution of local oscillator signals, maximizes circuitry commonality, and reduces power consumption.

The SA1620 and SA1638 allow considerable flexibility to optimize the transceiver design for particular price/size/performance requirements, through choice of appropriate RF and IF filters. The IF may be chosen freely in the range 70–500MHz. The same IF can be used in the transmit and receive directions. Alternately, different IFs can be used if the SA1638 synthesizer frequency is switched between transmit and receive timeslots. The comparison frequency of the SA1638 PLL is high in order to provide fast switching time.

With suitable choice of the IF, an identical SA1638 IF receiver design can be used for both 900MHz GSM and 1800MHz PCN (DCS1800) equipment.

General Benefits/Advantages

- 2.7V operation. Compatible with 3V digital technology and portable applications. (Higher voltage operation also possible, if desired.)
- Excellent dynamic range. The availability of two LNAs in the SA1620 allows flexibility in receiver dynamic design for portable and mobile GSM spec. applications with appropriate filters. If for a particular application a GaAs or discrete front-end is desired, one of the LNAs can be left unpowered. Placing the AGC gain switches at the front results in some attenuation most of the time, further increasing typical dynamic performance beyond that specified by GSM.
- High power transmit output driver, delivering +7.5dBm output. This is sufficient to drive a filter and power amplifier input, without a driver amplifier. To avoid unnecessary current consumption, the output power can be reduced to an appropriate level by choice of an external resistor.
- DC offsets generated in the receive channel are independent of the AGC setting, and correctable by software to prevent erosion of signal handling dynamic range by DC offsets. Independence of DC from AGC setting is achieved by putting the gain switches in the RF front-end.
- Minimal high-quality filter requirements. As a result of the integration in the SA1638 of high quality channel selectivity filters, only sufficient filtering is needed in the receive path to provide blocking protection for the second mixers. This reduces receiver cost and size.
- Operation at a high IF allows RF image reject filter requirements to be relaxed. For example, at a 400MHz IF, the natural gain roll-off in the SA1620 LNAs and mixer suppresses the image signal in the 1800MHz band by typically 28dB below the desired 900MHz band signal.

DC Offset Correction

DC offset correction is provided by two DACs each feeding into one of the two Rx channels. The step size of both DACs is set by the value of the external resistor between DCRES and ground. With a resistor value of 120kΩ, the step size is 200mV. The actual offset of each DAC is controlled independently by 4 bits within a DC register. For each DAC 1 bit controls the polarity of the offset and the other 3 bits control the magnitude of the offset. Thus any original offset less than 1.5V magnitude in either channel can be reduced to the specified level by selecting the appropriate DAC setting via the serial interface.

Integrated Receive Filters

The low-pass characteristics of the Rx channel are determined by two low-pass responses. The first of these is the output of the quadrature mixers and the second is the low-pass filters which follow the post-mixer amplifiers. These specifications refer only to the response of the default state, but this may be switched by the control register to an alternative setting with a nominal 3dB point of 792kHz. In this alternative bandwidth setting, the performance of the circuit is not specified.

The corner frequency of the low pass filters can be adjusted over a wide range by varying the value of the external resistor between RESA and RESB. The range of feasible corner frequencies extends at least between 50kHz and 500kHz. As with the alternative bandwidth setting on the mixer outputs, the performance of the circuit is not specified when the alternative low-pass filter bandwidth is active.

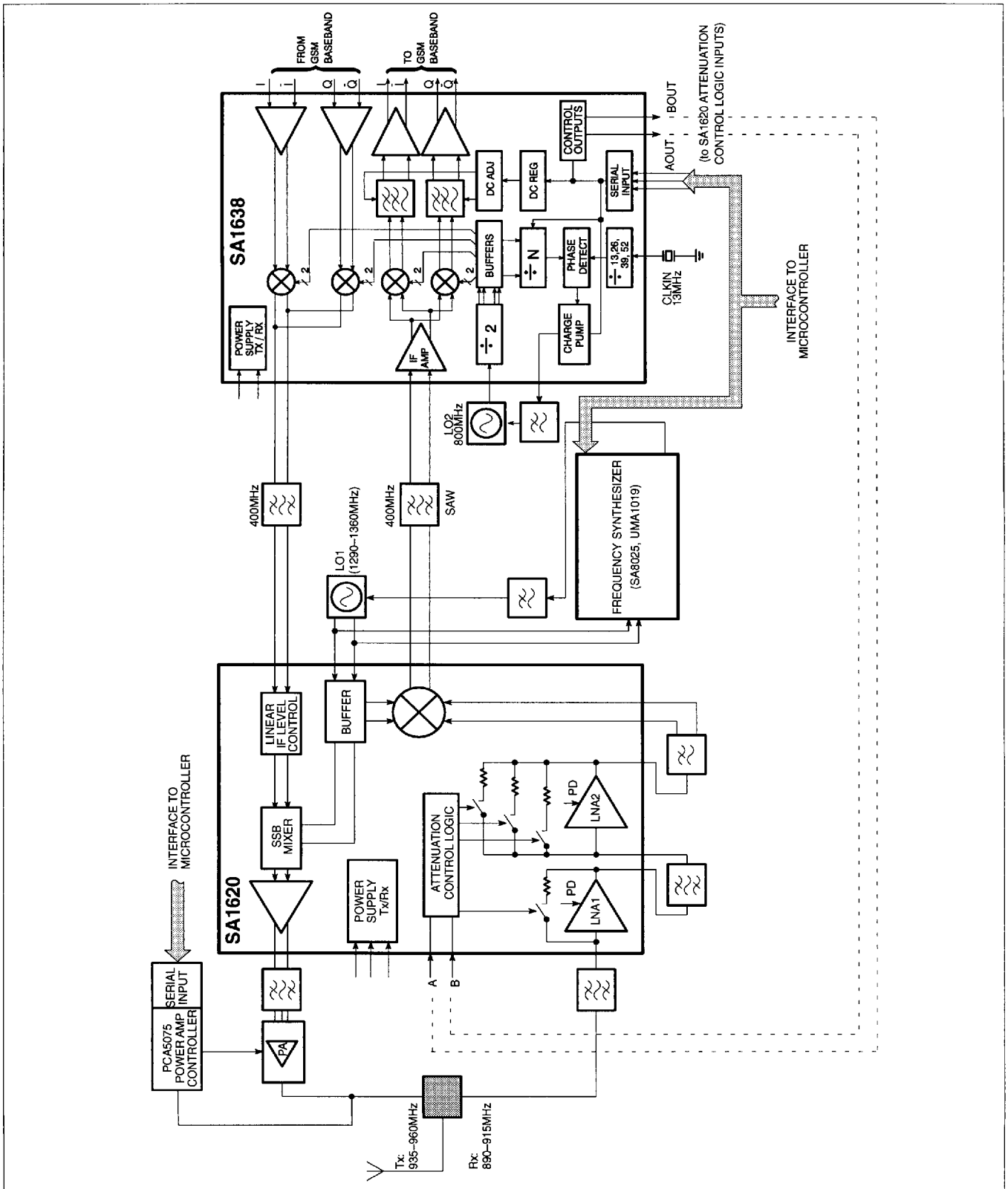


Figure 8.