



## FUNCTIONAL DESCRIPTION

The ICS843207-350 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A 14MHz fundamental crystal is used as the input to the on chip oscillator. The output of the oscillator is fed into the pre-divider. In frequency margining mode, the 14MHz crystal frequency is divided by 2 and a 7MHz reference frequency is applied to the phase detector. The VCO of the PLL operates over a range of 620MHz to 750MHz. The output of the M divider is also applied to the phase detector. The default mode for the ICS843207-350 is a nominal VCO frequency of 700MHz with each output configurable to divide by 2, 4 or 8. The nominal output frequency can be changed by placing the device into the margining mode using the mode pin

and using the margin pin to change the M feedback divider. Frequency margining mode operation occurs when the MODE input is HIGH. The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. The output of the VCO is scaled by an output divider prior to being sent to the LVPECL output buffer. The divider provides a 50% output duty cycle. The relationship between the crystal input frequency, the M divider, the VCO frequency and the output frequency is provided in Table 1A. When changing back from frequency margining mode to nominal mode, the device will return to the default nominal configuration described above.

**TABLE 1A. FREQUENCY SELECT FUNCTION TABLE**

| XTAL (MHz) | SELx | SELx-1 | VCO (MHz) | Output Divider | Output Frequency (MHz) |
|------------|------|--------|-----------|----------------|------------------------|
| 14         | 0    | 0      | 700       | N/A            | HiZ                    |
| 14         | 0    | 1      | 700       | 2              | 350                    |
| 14         | 1    | 0      | 700       | 8              | 87.5                   |
| 14         | 1    | 1      | 700       | 4              | 175                    |

**TABLE 1B. FREQUENCY MARGIN FUNCTION TABLE**

| MODE | MARGIN | XTAL (MHz) | Pre-Divider (P) | Feedback Divider | VCO (MHz) | % Change  |
|------|--------|------------|-----------------|------------------|-----------|-----------|
| 1    | 0      | 14         | 2               | 95               | 665       | -5.0      |
| 0    | X      | 14         | 1               | 50               | 700       | Nom. Mode |
| 1    | 1      | 14         | 2               | 105              | 735       | +5.0      |

TABLE 2. PIN DESCRIPTIONS

| Number                                                                   | Name                                                                                                     | Type   |          | Description                                                                                                                                                                                                                                             |
|--------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 7, 12,<br>25, 30, 34                                                  | V <sub>CCO</sub>                                                                                         | Power  |          | Output supply pins.                                                                                                                                                                                                                                     |
| 2, 3                                                                     | Q0, nQ0                                                                                                  | Output |          | Differential output pair. LVPECL interface levels.                                                                                                                                                                                                      |
| 4, 5                                                                     | Q1, nQ1                                                                                                  | Output |          | Differential output pair. LVPECL interface levels.                                                                                                                                                                                                      |
| 6, 16, 31                                                                | V <sub>EE</sub>                                                                                          | Power  |          | Negative supply pins.                                                                                                                                                                                                                                   |
| 8, 9                                                                     | Q2, nQ2                                                                                                  | Output |          | Differential output pair. LVPECL interface levels.                                                                                                                                                                                                      |
| 10, 11                                                                   | Q3, nQ3                                                                                                  | Output |          | Differential output pair. LVPECL interface levels.                                                                                                                                                                                                      |
| 13                                                                       | MODE                                                                                                     | Input  | Pulldown | MODE pin. LOW = default mode. HIGH = frequency margining mode. See Table 4B. LVCMOS/LVTTL interface levels.                                                                                                                                             |
| 14                                                                       | Margin                                                                                                   | Input  | Pulldown | Sets the frequency to ±5% in frequency margining mode. See Table 1B. LVCMOS/LVTTL interface levels.                                                                                                                                                     |
| 15                                                                       | MR                                                                                                       | Input  | Pulldown | Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go LOW and inverted outputs nQx to go HIGH. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 17                                                                       | REF_CLK                                                                                                  | Input  | Pulldown | Reference input clock. LVCMOS/LVTTL interface levels.                                                                                                                                                                                                   |
| 18                                                                       | nXTAL_SEL                                                                                                | Input  | Pulldown | Crystal select pin. Selects between the crystal and the reference clock inputs. LVCMOS/LVTTL interface levels.                                                                                                                                          |
| 19, 20                                                                   | XTAL_OUT,<br>XTAL_IN                                                                                     | Input  |          | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.                                                                                                                                                                      |
| 21, 35                                                                   | V <sub>CC</sub>                                                                                          | Power  |          | Core supply pins.                                                                                                                                                                                                                                       |
| 22                                                                       | nPLL_SEL                                                                                                 | Input  | Pulldown | PLL select pin. When HIGH, PLL is bypassed and input is fed directly to the output dividers. When LOW, PLL is enabled. LVCMOS/LVTTL interface levels.                                                                                                   |
| 23, 24,<br>37, 38,<br>39, 40,<br>41, 42,<br>43, 44,<br>45, 46,<br>47, 48 | SEL0, SEL1,<br>SEL2, SEL3,<br>SEL4, SEL5,<br>SEL6, SEL7,<br>SEL8, SEL9,<br>SEL10, SEL11,<br>SEL12, SEL13 | Input  | Pullup   | Output divider select pins. See Table 1A. LVCMOS/LVTTL interface levels.                                                                                                                                                                                |
| 26, 27                                                                   | Q4, nQ4                                                                                                  | Output |          | Differential output pair. LVPECL interface levels.                                                                                                                                                                                                      |
| 28, 29                                                                   | Q5, nQ5                                                                                                  | Output |          | Differential output pair. LVPECL interface levels.                                                                                                                                                                                                      |
| 32, 33                                                                   | Q6, nQ6                                                                                                  | Output |          | Differential output pair. LVPECL interface levels.                                                                                                                                                                                                      |
| 36                                                                       | V <sub>CCA</sub>                                                                                         | Power  |          | Analog supply pin.                                                                                                                                                                                                                                      |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 3. PIN CHARACTERISTICS

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 4       |         | pF    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | kΩ    |

TABLE 4A. nXTAL\_SEL CONTROL INPUT FUNCTION TABLE

| Input     |                   |
|-----------|-------------------|
| nXTAL_SEL | Selected Source   |
| 0         | XTAL_IN, XTAL_OUT |
| 1         | REF_CLK           |

TABLE 4B. MODE CONTROL INPUT FUNCTION TABLE

| Input | Condition                |
|-------|--------------------------|
| MODE  | Q0:Q6, nQ0:nQ6           |
| 0     | Default Mode             |
| 1     | Frequency Margining Mode |

## ABSOLUTE MAXIMUM RATINGS

|                                          |                          |
|------------------------------------------|--------------------------|
| Supply Voltage, $V_{CC}$                 | 4.6V                     |
| Inputs, $V_I$                            | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, $I_O$                           |                          |
| Continuous Current                       | 50mA                     |
| Surge Current                            | 100mA                    |
| Package Thermal Impedance, $\theta_{JA}$ | 65.7°C/W (0 mps)         |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C           |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 5A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{CCO} = V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$ 

| Symbol    | Parameter             | Test Conditions | Minimum         | Typical | Maximum  | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| $V_{CC}$  | Core Supply Voltage   |                 | 3.135           | 3.3     | 3.465    | V     |
| $V_{CCA}$ | Analog Supply Voltage |                 | $V_{CC} - 0.13$ | 3.3     | $V_{CC}$ | V     |
| $V_{CCO}$ | Output Supply Voltage |                 | 3.135           | 3.3     | 3.465    | V     |
| $I_{EE}$  | Power Supply Current  |                 |                 |         | 210      | mA    |
| $I_{CCA}$ | Analog Supply Current |                 |                 |         | 13       | mA    |

TABLE 5B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$ 

| Symbol              | Parameter                       | Test Conditions                                                                        | Minimum | Typical | Maximum        | Units   |
|---------------------|---------------------------------|----------------------------------------------------------------------------------------|---------|---------|----------------|---------|
| $V_{IH}$            | Input High Voltage              | $V_{CC} = 3.3V$                                                                        | 2       |         | $V_{CC} + 0.3$ | V       |
| $V_{IL}$            | Input Low Voltage               | $V_{CC} = 3.3V$                                                                        | -0.3    |         | 0.8            | V       |
| $I_{IH}$            | Input High Current              | REF_CLK, MARGIN, MODE, nPLL_SEL, MR, nXTAL_SEL<br>$V_{CC} = V_{IN} = 3.465$            |         |         | 150            | $\mu A$ |
|                     |                                 | SEL[0:13]<br>$V_{CC} = V_{IN} = 3.465$                                                 |         |         | 5              | $\mu A$ |
| $I_{IL}$            | Input Low Current               | REF_CLK, MARGIN, MODE, nPLL_SEL, MR, nXTAL_SEL<br>$V_{CC} = 3.465V$ ,<br>$V_{IN} = 0V$ | -5      |         |                | $\mu A$ |
|                     |                                 | SEL[0:13]<br>$V_{CC} = 3.465V$ ,<br>$V_{IN} = 0V$                                      | -150    |         |                | $\mu A$ |
| $\Delta t/\Delta v$ | Input Transition Rise/Fall Rate | SEL[0:13], MODE                                                                        |         |         | 20             | ns/V    |

**TABLE 5C. LVPECL DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol      | Parameter                         | Test Conditions | Minimum         | Typical | Maximum         | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CCO} - 1.4$ |         | $V_{CCO} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CCO} - 2.0$ |         | $V_{CCO} - 1.7$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.6             |         | 1.0             | V     |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ .**TABLE 6. CRYSTAL CHARACTERISTICS**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 | 12.4        | 14      | 15      | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 40      | $\Omega$ |
| Shunt Capacitance                  |                 |             |         | 7       | pF       |
| Drive Level                        |                 |             |         | 300     | $\mu W$  |

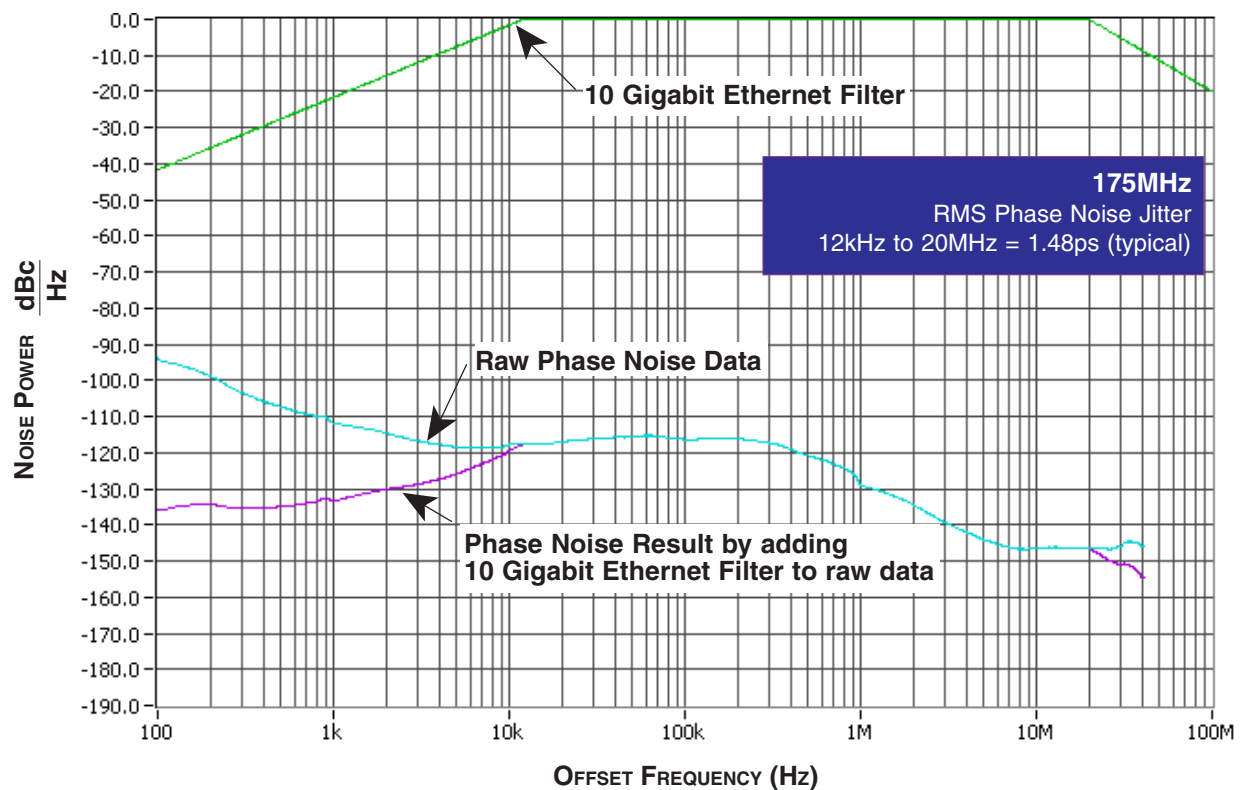
NOTE: Characterized using an 18pF parallel resonant crystal.

**TABLE 7. AC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

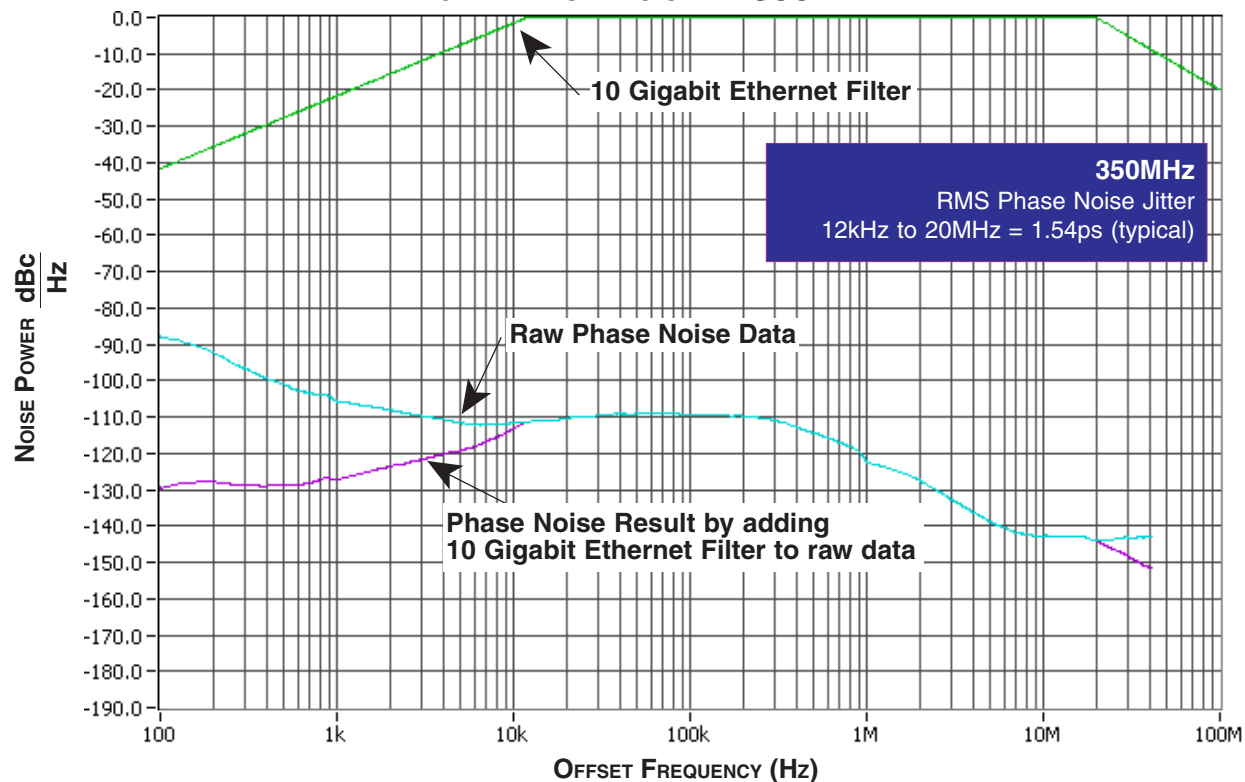
| Symbol               | Parameter                        | Test Conditions                        | Minimum | Typical | Maximum | Units |
|----------------------|----------------------------------|----------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency                 | $N = \div 2$                           | 310     | 350     | 375     | MHz   |
|                      |                                  | $N = \div 4$                           | 155     | 175     | 187.5   | MHz   |
|                      |                                  | $N = \div 8$                           | 77.5    | 87.5    | 93.75   | MHz   |
| $f_{IN}$             | Input Frequency                  | REF_CLK                                | 12.4    | 14      | 15      | MHz   |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, Random; NOTE 1 | Mode = LOW<br>350MHz, (12kHz - 20MHz)  |         | 1.54    |         | ps    |
|                      |                                  | Mode = LOW<br>175MHz, (12kHz - 20MHz)  |         | 1.48    |         | ps    |
|                      |                                  | Mode = LOW<br>87.5MHz, (12kHz - 20MHz) |         | 1.61    |         | ps    |
| $t_R / t_F$          | Output Rise/Fall Time            | 20% to 80%                             | 300     |         | 600     | ps    |
| odc                  | Output Duty Cycle                | Output Divider = $\div 2$              | 42      |         | 58      | %     |
|                      |                                  | Output Divider = $\neq 2$              | 46      |         | 64      | %     |

NOTE 1: Characterized using a 14MHz crystal.

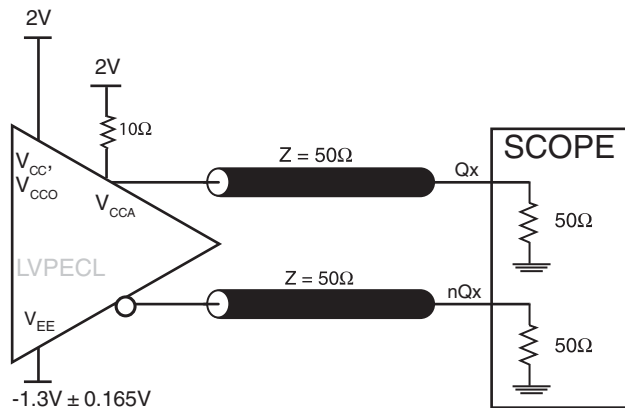
## TYPICAL PHASE NOISE AT 175MHz



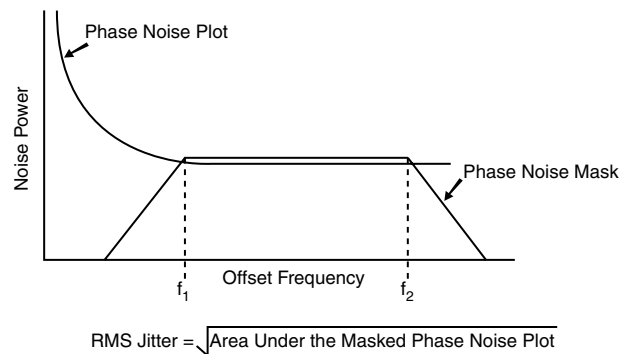
## TYPICAL PHASE NOISE AT 350MHz



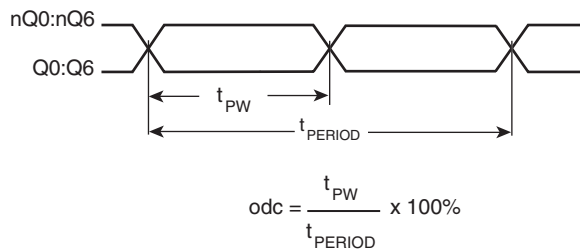
## PARAMETER MEASUREMENT INFORMATION



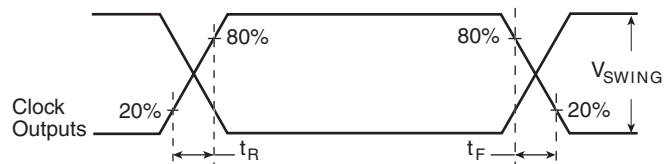
**3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT**



**RMS PHASE JITTER**



**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



**OUTPUT RISE/FALL TIME**

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843207-350 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$  and  $V_{CCO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{CC}$  pin and also shows that  $V_{CCA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{CCA}$  pin.

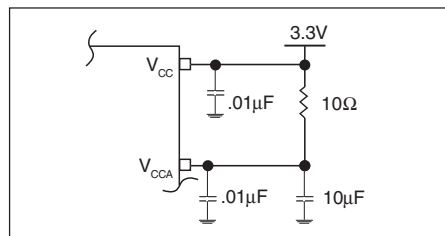


FIGURE 1. POWER SUPPLY FILTERING

### CRYSTAL INPUT INTERFACE

The ICS843207-350 has been characterized with  $18\text{pF}$  parallel resonant crystals. The capacitor values shown in

*Figure 2* below were determined using a  $14\text{MHz}$ ,  $18\text{pF}$  parallel resonant crystal and were chosen to minimize the ppm error.

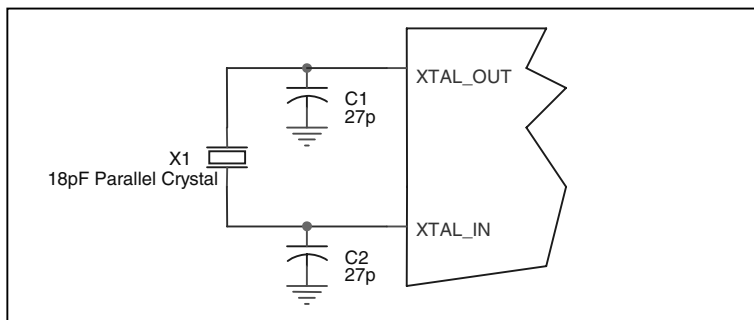


FIGURE 2. CRYSTAL INPUT INTERFACE



## LVC MOS TO XTAL INTERFACE

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3*. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω.

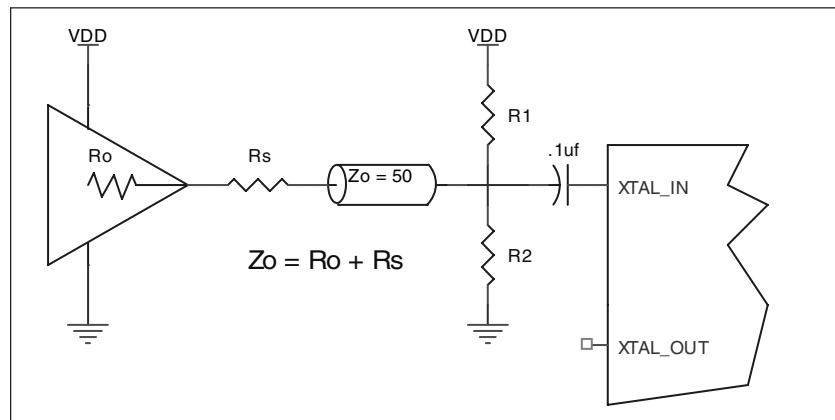


FIGURE 3. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

## RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### INPUTS:

#### CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL\_IN to ground.

#### REF\_CLK INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF\_CLK to ground.

#### LVC MOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### OUTPUTS:

#### LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

### TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are

designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

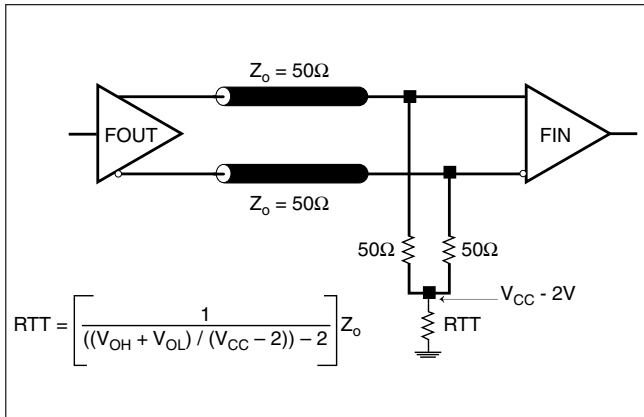


FIGURE 4A. LVPECL OUTPUT TERMINATION

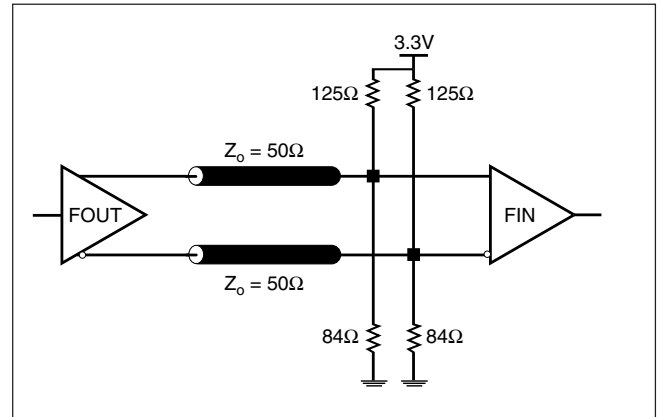


FIGURE 4B. LVPECL OUTPUT TERMINATION

## SCHEMATIC EXAMPLE

Figure 5 shows an example of ICS843207-350 application schematic. In this example, the device is operated at  $V_{CC} = V_{CCO} = 3.3V$ . The 18pF parallel resonant 14MHz crystal is used. The  $C1 = 27pF$  and  $C2 = 27pF$  are recommended for frequency accuracy. For different board layout, the  $C1$

and  $C2$  may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL terminations are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

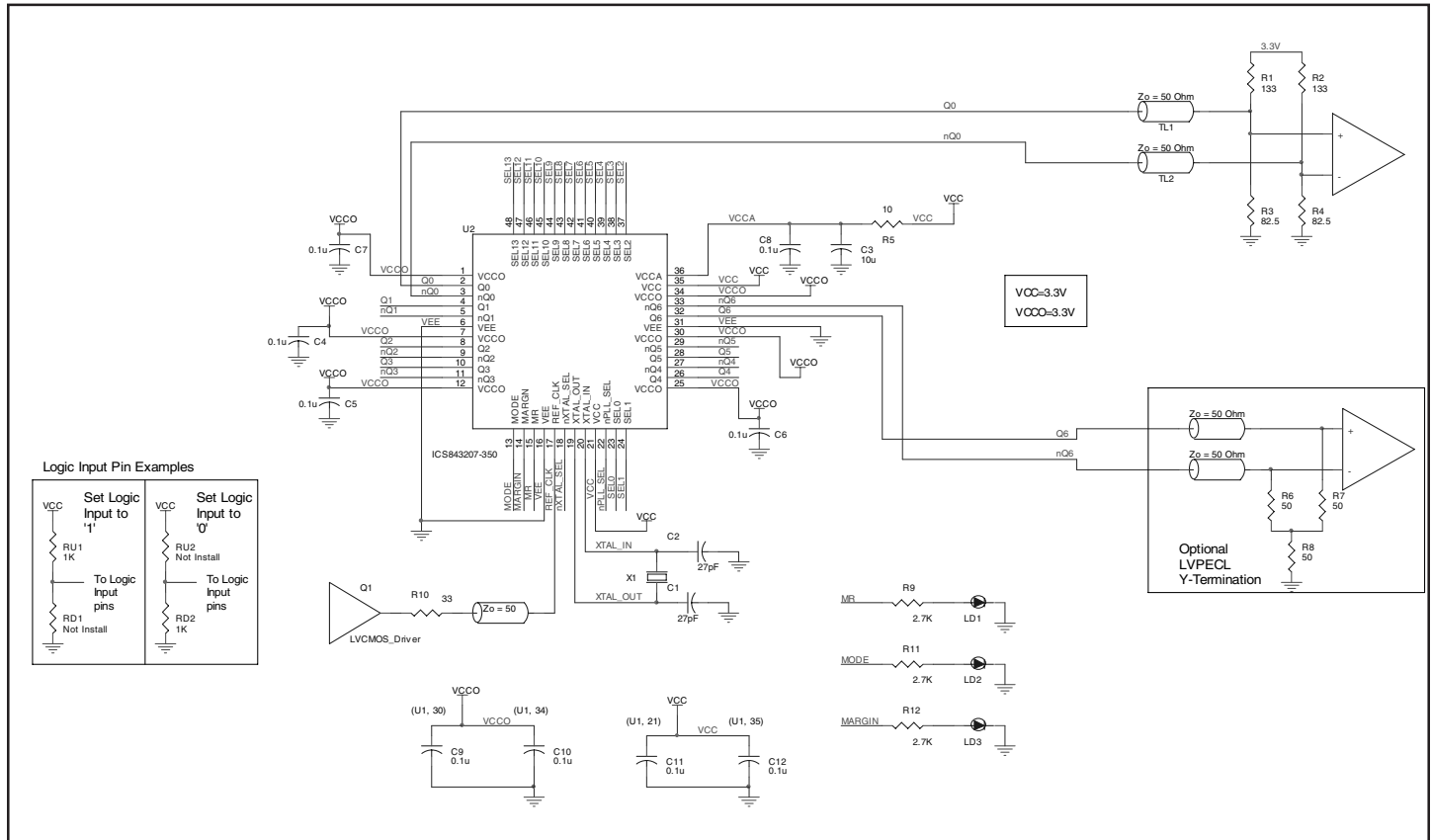


FIGURE 5. ICS843207-350 SCHEMATIC LAYOUT

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843207-350. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS843207-350 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 210mA = 727.65mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $7 * 30mW = 210mW$

$$\text{Total Power}_{MAX} (3.63V, \text{ with all outputs switching}) = 727.65mW + 210mW = 937.65mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming air flow at 1 meter per second and a multi-layer board, the appropriate value is 55.9°C/W per Table 8 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:  
 $70^\circ C + 0.938W * 55.9^\circ C/W = 122.4^\circ C$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

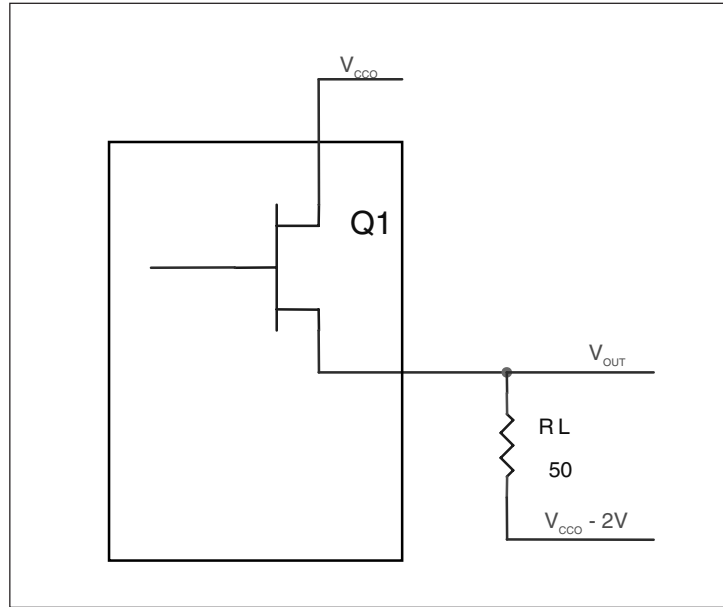
**TABLE 8. THERMAL RESISTANCE  $\theta_{JA}$  FOR 48-PIN LQFP, FORCED CONVECTION**

| $\theta_{JA}$ by Velocity (Meters per Second) |          |          |          |
|-----------------------------------------------|----------|----------|----------|
|                                               | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards   | 65.7°C/W | 55.9°C/W | 52.4°C/W |

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*.



**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.9V$

$$(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.9V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$

$$(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30mW$$

## RELIABILITY INFORMATION

**TABLE 9.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 48 LEAD LQFP**

| $\theta_{JA}$ by Velocity (Meters per Second) |          |          |          |
|-----------------------------------------------|----------|----------|----------|
|                                               | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards   | 65.7°C/W | 55.9°C/W | 52.4°C/W |

### TRANSISTOR COUNT

The transistor count for ICS843207-350 is: 4380

## PACKAGE OUTLINE - Y SUFFIX FOR 48 LEAD LQFP

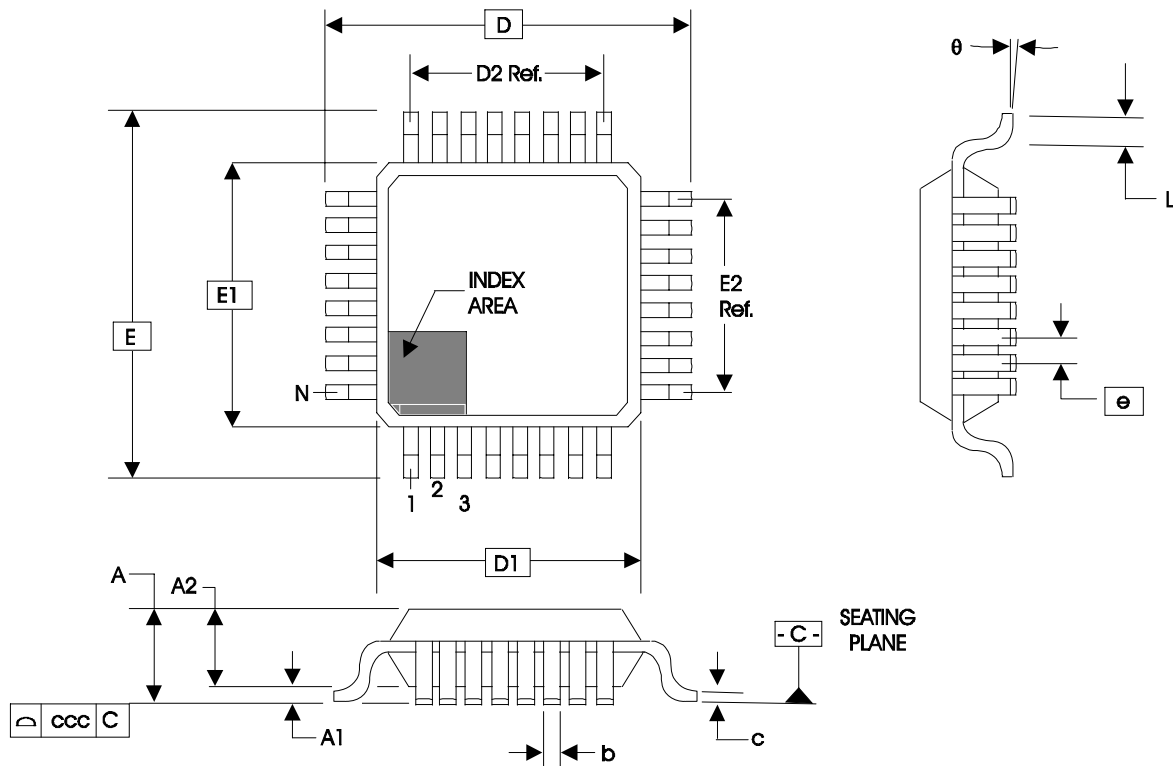


TABLE 10. PACKAGE DIMENSIONS

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |            |         |         |
|--------------------------------------------------|------------|---------|---------|
| SYMBOL                                           | BBC        |         |         |
|                                                  | MINIMUM    | NOMINAL | MAXIMUM |
| N                                                | 48         |         |         |
| A                                                | --         | --      | 1.60    |
| A1                                               | 0.05       | --      | 0.15    |
| A2                                               | 1.35       | 1.40    | 1.45    |
| b                                                | 0.17       | 0.22    | 0.27    |
| c                                                | 0.09       | --      | 0.20    |
| D                                                | 9.00 BASIC |         |         |
| D1                                               | 7.00 BASIC |         |         |
| D2                                               | 5.50 Ref.  |         |         |
| E                                                | 9.00 BASIC |         |         |
| E1                                               | 7.00 BASIC |         |         |
| E2                                               | 5.50 Ref.  |         |         |
| e                                                | 0.50 BASIC |         |         |
| L                                                | 0.45       | 0.60    | 0.75    |
| θ                                                | 0°         | --      | 7°      |
| ccc                                              | --         | --      | 0.08    |

Reference Document: JEDEC Publication 95, MS-026

TABLE 11. ORDERING INFORMATION

| Part/Order Number | Marking   | Package                  | Shipping Packaging | Temperature |
|-------------------|-----------|--------------------------|--------------------|-------------|
| 843207CY-350      | 43207C350 | 48 Lead LQFP             | tray               | 0°C to 70°C |
| 843207CY-350T     | 43207C350 | 48 Lead LQFP             | 1000 tape & reel   | 0°C to 70°C |
| 843207CY-350LF    | 3207C350L | 48 Lead "Lead-Free" LQFP | tray               | 0°C to 70°C |
| 843207CY-350LFT   | 3207C350L | 48 Lead "Lead-Free" LQFP | 1000 tape & reel   | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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## REVISION HISTORY SHEET

| Rev | Table | Page | Description of Change    | Date    |
|-----|-------|------|--------------------------|---------|
| A   |       | 11   | Added Schematic Example. | 1/16/08 |
|     |       |      |                          |         |
|     |       |      |                          |         |

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