WM8312

Processor Power Management Subsystem

DESCRIPTION

WM8312 is an integrated power-management subsystem which provides a cost-effective, flexible, single-chip solution for power management, specifically targeted at the requirements of a range of low-power portable applications. WM8312 is specifically designed to operate as a system PMIC supporting a variety of industry standard processors and accessories in a wide range of applications.

The start-up behaviour and configuration is fully programmable in an integrated One Time Programmable (OTP) Non-Volatile Memory (NVM). This highly flexible solution helps reduce time-to-market, as changing application requirements can be very easily accommodated.

The WM8312 power management subsystem comprises of four programmable DC-DC converters, eleven LDO regulators (four of which are low-noise for supplying sensitive analogue subsystems). The integrated OTP bootstrap circuitry controls the start-up sequencing and voltages of the converters and regulators as well as the sequencing of system clocks.

WM8312 can be powered from a battery, a wall adaptor or from a USB power source. An on-chip regulator provides power for always-on PMIC functions such as register map and the RTC. The device provides autonomous backup battery switchover. A low-power LDO is included to support 'alive' processor power domains external to the WM8312.

A linear on-chip battery charger supports trickle charging and constant current/constant voltage charging of single-cell lithium-ion/lithium-polymer batteries. The charge current, termination voltage, and charger time-out are programmable. WM8312 detects and handles battery fault conditions with a minimum of system software involvement.

A 12-bit Auxiliary ADC supports a wide range of applications for internal as well as external analogue sampling, such as voltage detection and temperature measurement. The Touch Panel controller uses the same ADC on an interleaved basis.

WM8312 includes a crystal oscillator, an internal RC oscillator and Frequency Locked Loop (FLL) to generate all clock signals for autonomous system start-up and processor clocking. A Secure Real-Time Clock (S-RTC) and alarm function is included, capable of waking up the system from low-power modes. A watchdog function is provided to ensure system integrity.

To maximise battery life, highly-granular power management enables each function in the WM8312 subsystem to be independently powered down through a control interface or alternatively through register and OTP-configurable GPIOs. The device offers a standby power consumption of <10µA, making it particularly suitable for portable applications.

The WM8312 is supplied in a 7x7mm 169-ball BGA package, ideal for use in portable systems. The WM8312 forms part of the Wolfson series of audio and power management solutions.

FEATURES

Power Management

- 2 x DC-DC synch. buck converter (0.6V - 1.8V, 1.2A, DVS)
- 1 x DC-DC synch. buck converter (0.85V - 3.4V, 1A)
- 1 x DC-DC boost converter (up to 30V, up to 90mA)
- 1 x LDO regulator (0.9V - 3.3V, 300mA, 1Ω)
- 2 x LDO regulators (0.9V - 3.3V, 200mA, 1Ω)
- 3 x LDO regulators (0.9V - 3.3V, 100mA, 2Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 200mA, 1Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 150mA, 2Ω)
- 1 x 'alive' regulator (0.8V – 1.55V, up to 10mA)

Backlight LED Current Sinks

- 2 x programmable constant current sinks, suitable for multi-LED display backlight control

Battery Charger

- Programmable single-cell lithium-ion / lithium-polymer battery charger (1A max charge current)
- Battery monitoring for temperature and voltage
- Autonomous backup battery charging and switching

System Control

- I^2C or SPI compatible primary control interface
- Interrupt-based feedback communication scheme
- Watchdog timer and system reset control
- Autonomous power sequencing and fault detection
- Intelligent power path and power source selection
- OTP memory bootstrap configuration function

Additional Features

- Auxiliary ADC for multi-function analogue measurement
- Touch Panel interface controller (4-wire and 5-wire)
- 128-bit pseudo-random unique ID
- Secure Real-Time Clock with wake-up alarm
- 16 x configurable multi-function (GPIO) pins
- Comprehensive clocking scheme: low-power 32kHz RTC crystal oscillator, Frequency Locked Loop, GPIO clock output and 4MHz RC clock for power management
- System LED outputs indicating power state, battery charger or fault status
- Selectable USB current limiting up to 1.8A (in accordance with USB Battery Charging specification Rev 1.1)

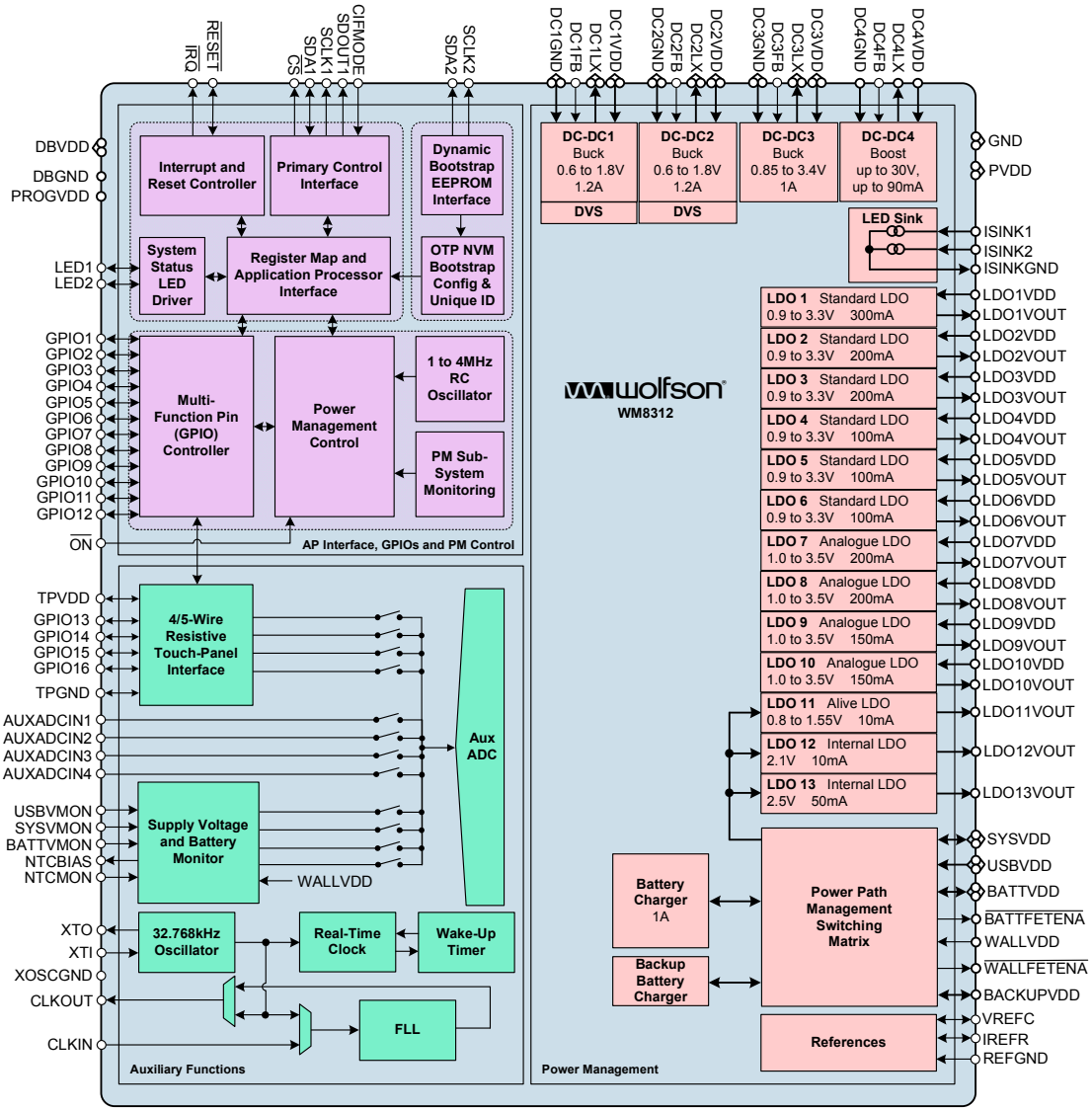
Package Options

- 7x7mm, 169-ball BGA package, 0.5mm ball pitch

APPLICATIONS

- Portable Media Players
- Portable Navigation Devices
- Cellular Handsets
- Electronic Books
- Electronic Gaming Devices

BLOCK DIAGRAM



TYPICAL APPLICATIONS

The WM8312 is designed as a system PMIC device that manages multiple power supply paths (wall adapter, USB, battery) and generates configurable DC supplies to power processors and associated peripherals within a system. The WM8312 provides three step-down DC-DC converters and one step-up DC-DC converter. Eleven LDO regulators provide a high degree of flexibility to provide power to multiple devices, with the capability to power-up and power-down different circuits independently.

Two of the DC-DC step-down converters are specifically designed to handle rapid changes in load current, as required by modern application processors; selectable operating modes allow the converters to be optimally configured for light, heavy or transient load conditions; they can also be tailored for minimum PCB area, maximum performance, or for maximum efficiency. The analogue LDOs provide low-noise outputs suitable for powering sensitive circuits such as RF / Wi-Fi / bluetooth radio applications.

The WM8312 powers up the converters and LDOs according to a programmable sequence. A configurable 'SLEEP' state is also available, providing support for an alternate configuration, typically for low-power/standby operation. The power control sequences and many other parameters can be stored in an integrated user-programmable OTP memory or may be loaded from an external memory. The WM8312 supports autonomous programming and verification of the integrated OTP memory.

The WM8312 provides power path management which seamlessly switches between wall adapter, USB and battery power sources according to the prevailing conditions. A backup battery supply is also supported in order to maintain the Real Time Clock (RTC) in the absence of any other supplies. The WM8312 provides a battery charger for the main battery as well as the backup battery; these can be powered from either the wall adapter or USB supplies.

Programmable GPIO pins may be configured as hardware inputs for general use or for selecting different power management configurations. As outputs, the GPIOs can provide indications of the device status, or may be used as control signals for other power management circuits. The WM8312 also provides two LED drivers, which can be controlled manually or configured as status indicators for the OTP memory programmer, operating power state or battery charger.

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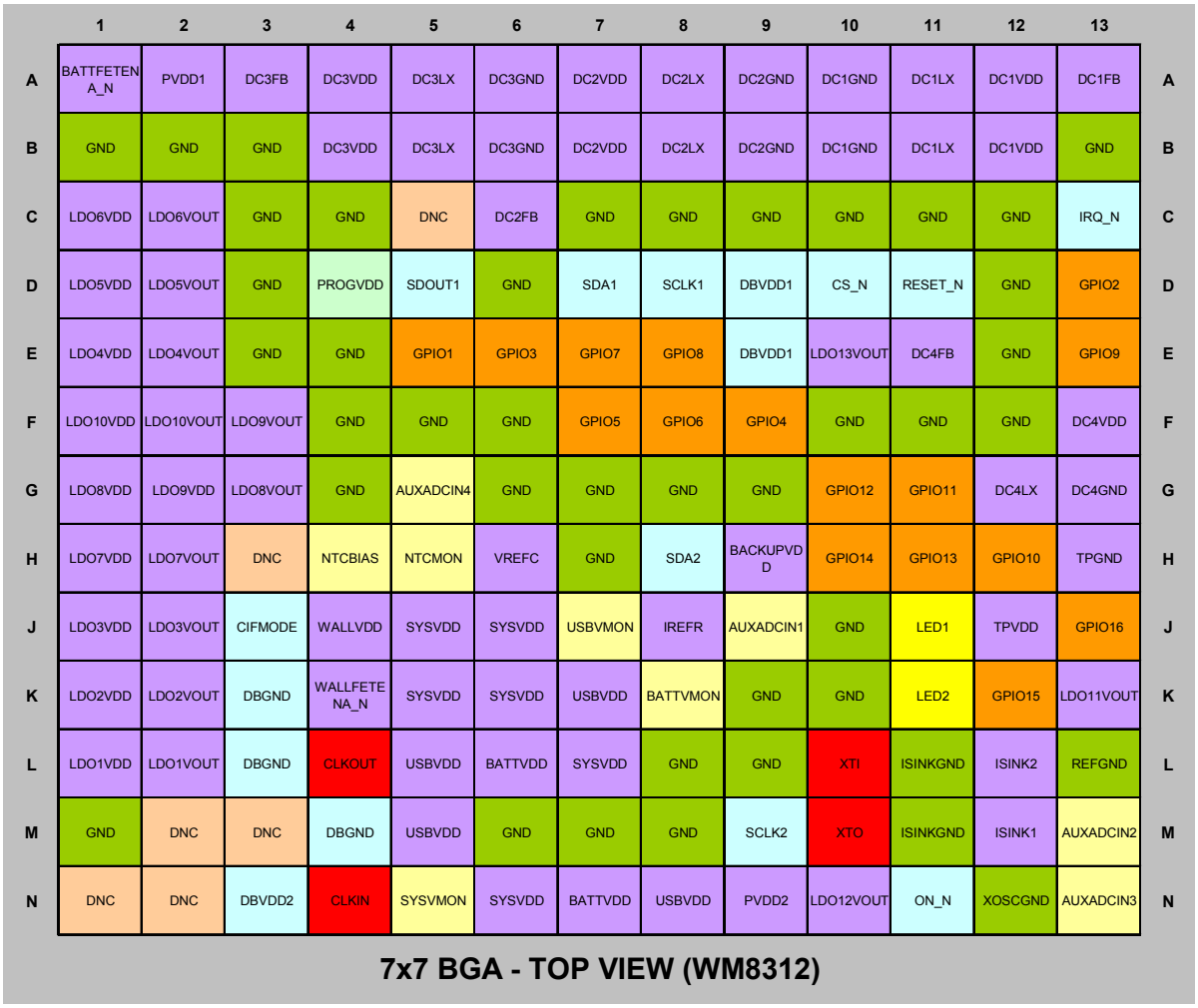
PIN CONFIGURATION



	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	BATTFETENA_N	PVDD1	DC3FB	DC3VDD	DC3LX	DC3GND	DC2VDD	DC2LX	DC2GND	DC1GND	DC1LX	DC1VDD	DC1FB	A
B	GND	GND	GND	DC3VDD	DC3LX	DC3GND	DC2VDD	DC2LX	DC2GND	DC1GND	DC1LX	DC1VDD	GND	B
C	LDO6VDD	LDO6VOUT	GND	GND	DNC	DC2FB	GND	GND	GND	GND	GND	GND	IRQ_N	C
D	LDO5VDD	LDO5VOUT	GND	PROGVDD	SDOUT1	GND	SDA1	SCLK1	DBVDD1	CS_N	RESET_N	GND	GPIO2	D
E	LDO4VDD	LDO4VOUT	GND	GND	GPIO1	GPIO3	GPIO7	GPIO8	DBVDD1	LDO13VOUT	DC4FB	GND	GPIO9	E
F	LDO10VDD	LDO10VOUT	LDO9VOUT	GND	GND	GND	GPIO5	GPIO6	GPIO4	GND	GND	GND	DC4VDD	F
G	LDO8VDD	LDO9VDD	LDO8VOUT	GND	AUXADCIN4	GND	GND	GND	GND	GPIO12	GPIO11	DC4LX	DC4GND	G
H	LDO7VDD	LDO7VOUT	DNC	NTCBIAS	NTCMON	VREFC	GND	SDA2	BACKUPVDD	GPIO14	GPIO13	GPIO10	TPGND	H
J	LDO3VDD	LDO3VOUT	CIFMODE	WALLVDD	SYSVDD	SYSVDD	USBVMON	IREFR	AUXADCIN1	GND	LED1	TPVDD	GPIO16	J
K	LDO2VDD	LDO2VOUT	DBGND	WALLFETENA_N	SYSVDD	SYSVDD	USBVDD	BATTVMON	GND	GND	LED2	GPIO15	LDO11VOUT	K
L	LDO1VDD	LDO1VOUT	DBGND	CLKOUT	USBVDD	BATTVDD	SYSVDD	GND	GND	XTI	ISINKGND	ISINK2	REFGND	L
M	GND	DNC	DNC	DBGND	USBVDD	GND	GND	GND	SCLK2	XTO	ISINKGND	ISINK1	AUXADCIN2	M
N	DNC	DNC	DBVDD2	CLKIN	SYSVMON	SYSVDD	BATTVDD	USBVDD	PVDD2	LDO12VOUT	ON_N	XOSCGND	AUXADCIN3	N

7x7 BGA - TOP VIEW (WM8312)

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE (T_A)	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8312GEB/V	-40°C to +85°C	169-ball (7 x 7mm) (Pb-free)	MSL3	260°C
WM8312GEB/RV	-40°C to +85°C	169-ball (7 x 7mm) (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 2200

PIN DESCRIPTION

Notes:

1. Pins are sorted by functional groups.
2. The power domain associated with each pin is noted; VPMIC is the domain powered by LDO12 for the 'always-on' functions internal to the WM8312.

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
Touch Panel and Auxiliary ADC				
J7	USBVMON	Analogue Input	USBVDD	USBVDD Supply Voltage Monitor
N5	SYSVMON	Analogue Input	SYSVDD	SYSVDD Supply Voltage Monitor
K8	BATTVMON	Analogue Input	BATTVDD	BATTVDD Supply Voltage Monitor
J9	AUXADCIN1	Analogue Input/Output	SYSVDD	Auxiliary Analogue Input 1 / Battery Charge Current Monitor Output
M13	AUXADCIN2	Analogue Input		Auxiliary Analogue Input 2
N13	AUXADCIN3	Analogue Input		Auxiliary Analogue Input 3
G5	AUXADCIN4	Analogue Input	TPVDD	Auxiliary Analogue Input 4
J12	TPVDD	Supply		Touch panel VDD supply
H13	TPGND	Supply		Touch panel Power Ground
Clocking and Real Time Clock				
M10	XTO	Analogue Output	VPMIC	Crystal Drive Output
L10	XTI	Analogue Input		Crystal Drive Input or 32.768kHz CMOS Clock Input
N12	XOSCGND	Supply		Crystal Oscillator Ground
L4	CLKOUT	Digital Output	DBVDD2	CMOS Clock Output
N4	CLKIN	Digital Input		CMOS FLL Clock Input
General Purpose Input / Output				
E5	GPIO1	Digital I/O	DBVDD1 or VPMIC	GPIO Pin 1
D13	GPIO2	Digital I/O		GPIO Pin 2
E6	GPIO3	Digital I/O		GPIO Pin 3
F9	GPIO4	Digital I/O	DBVDD1 or SYSVDD	GPIO Pin 4
F7	GPIO5	Digital I/O		GPIO Pin 5
F8	GPIO6	Digital I/O		GPIO Pin 6
E7	GPIO7	Digital I/O	DBVDD1 or VPMIC	GPIO Pin 7
E8	GPIO8	Digital I/O		GPIO Pin 8
E13	GPIO9	Digital I/O		GPIO Pin 9
H12	GPIO10	Digital I/O	DBVDD1 or SYSVDD	GPIO Pin 10
G11	GPIO11	Digital I/O		GPIO Pin 11
G10	GPIO12	Digital I/O		GPIO Pin 12
H11	GPIO13	Digital I/O	TPVDD	GPIO Pin 13 / Touch panel interface
H10	GPIO14	Digital I/O		GPIO Pin 14 / Touch panel interface
K12	GPIO15	Digital I/O		GPIO Pin 15 / Touch panel interface
J13	GPIO16	Digital I/O		GPIO Pin 16 / Touch panel interface
Processor Interface and IC Control				
N11	$\overline{ON}$	Digital Input	VPMIC	ON Request Pin (Internal pull-up)
D11	$\overline{RESET}$	Digital I/O	DBVDD1	System Reset Input and Open Drain Output. (Internal pull-up)
C13	$\overline{IRQ}$	Digital Output	DBVDD1	PMIC Interrupt Flag Output. Configurable Open Drain / CMOS mode. (Internal pull-up in Open Drain mode.)

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION	
J3	CIFMODE	Digital Input	DBVDD2	Primary Control Interface Mode Select: 0 = I²C Compatible Control Interface Mode 1 = SPI Compatible Control Interface Mode	
				SPI Compatible Control Interface Mode	*I²C Compatible Control Interface Mode*
D5	SDOUT1	Digital Output	DBVDD1	Control Interface Serial Data Out	No Function
D8	SCLK1	Digital Input		Control Interface Serial Clock	Control Interface Serial Clock
D7	SDA1	Digital I/O		Control Interface Serial Data In	Control Interface Serial Data Input and Open Drain Output. (Output can extend above DBVDD1 domain.)
D10	$\overline{CS}$	Digital Input		Control Interface Chip Select	I²C Address Select: 0 = 0x68h 1 = 0x6Ch
M9	SCLK2	Digital I/O	VPMIC	Control Interface Serial Clock for external DBE EEPROM (Internal pull-down)	
H8	SDA2	Digital I/O		Control Interface Serial Data to/from external DBE EEPROM (Internal pull-down)	
D9, E9	DBVDD1	Supply		Digital Buffer Supply	
N3	DBVDD2	Supply		Digital Buffer Supply	
K3, L3, M4	DBGND	Supply		Digital Buffer Ground	
OTP Memory					
D4	PROGVDD	Supply		High-voltage input for OTP programming.	
DC-DC Converters and LDO Regulators					
B1, B2, B3, B13, C3, C4, C7, C8, C9, C10, C11, C12, D3, D6, D12, E3, E4, E12, F4, F5, F6, F10, F11, F12, G4, G6, G7, G8, G9, H7, J10, K9, K10, L8, L9, M1, M6, M7, M8	GND1	Supply		Ground	
A2	PVDD1	Supply		Internal VDD supply; Connect to SYSVDD	
N9	PVDD2	Supply			
A10, B10	DC1GND	Supply		DC-DC1 Power Ground	
A13	DC1FB	Analogue Input	DC1VDD	DC-DC1 Feedback Pin	
A11, B11	DC1LX	Analogue I/O		DC-DC1 Inductor Connection	
A12, B12	DC1VDD	Supply		DC-DC1 Power Input	
A9, B9	DC2GND	Supply		DC-DC2 Power Ground	
C6	DC2FB	Analogue Input	DC2VDD	DC-DC2 Feedback Pin	

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
A8, B8	DC2LX	Analogue I/O		DC-DC2 Inductor Connection
A7, B7	DC2VDD	Supply		DC-DC2 Power Input
A6, B6	DC3GND	Supply		DC-DC3 Power Ground
A3	DC3FB	Analogue Input	DC3VDD	DC-DC3 Feedback Pin
A5, B5	DC3LX	Analogue I/O		DC-DC3 Inductor Connection
A4, B4	DC3VDD	Supply		DC-DC3 Power Input
G13	DC4GND	Supply		DC-DC4 Power Ground
E11	DC4FB	Analogue Input	DC4VDD	DC-DC4 Feedback Connection
G12	DC4LX	Analogue I/O		DC-DC4 Inductor Connection
F13	DC4VDD	Supply		DC-DC4 Power Input
L1	LDO1VDD	Supply		LDO1 Power Input
L2	LDO1VOUT	Analogue Output	LDO1VDD	LDO1 Power Output
K1	LDO2VDD	Supply		LDO2 Power Input
K2	LDO2VOUT	Analogue Output	LDO2VDD	LDO2 Power Output
J1	LDO3VDD	Supply		LDO3 Power Input
J2	LDO3VOUT	Analogue Output	LDO3VDD	LDO3 Power Output
E1	LDO4VDD	Supply		LDO4 Power Input
E2	LDO4VOUT	Analogue Output	LDO4VDD	LDO4 Power Output
D1	LDO5VDD	Supply		LDO5 Power Input
D2	LDO5VOUT	Analogue Output	LDO5VDD	LDO5 Power Output
C1	LDO6VDD	Supply		LDO6 Power Input
C2	LDO6VOUT	Analogue Output	LDO6VDD	LDO6 Power Output
H1	LDO7VDD	Supply		LDO7 Power Input
H2	LDO7VOUT	Analogue Output	LDO7VDD	LDO7 Power Output
G1	LDO8VDD	Supply		LDO8 Power Input
G3	LDO8VOUT	Analogue Output	LDO8VDD	LDO8 Power Output
G2	LDO9VDD	Supply		LDO9 Power Input
F3	LDO9VOUT	Analogue Output	LDO9VDD	LDO9 Power Output
F1	LDO10VDD	Supply		LDO10 Power Input
F2	LDO10VOUT	Analogue Output	LDO10VDD	LDO10 Power Output
K13	LDO11VOUT	Analogue Output		LDO11 (Alive) Power Output
N10	LDO12VOUT	Analogue I/O		LDO12 (Internal VPMIC) Output; not for general use
E10	LDO13VOUT	Analogue I/O	PVDD2	LDO13 (Internal INTVDD) Output; not for general use
Current Sinks				
M12	ISINK1	Analogue Output	SYSVDD	LED String Current Sink 1
L12	ISINK2	Analogue Output		LED String Current Sink 2
L11, M11	ISINKGND	Supply		LED String Current Sink Ground
Voltage and Current References				
H6	VREFC	Analogue I/O	VPMIC	Voltage Reference capacitor connection point
J8	IREFR	Analogue I/O		Current Reference resistor connection point
L13	REFGND	Supply		Reference Ground
Power Path Management				
J5, J6, K5, K6, L7, N6	SYSVDD	Supply		System VDD Supply
K7, L5, M5, N8	USBVDD	Supply		USB VDD Supply
L6, N7	BATTVDD	Supply		Primary Battery Supply
A1	BATTFETENA	Digital Output	PVDD1	External Battery FET Driver
J4	WALLVDD	Supply		Wall VDD Supply/Sense

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
K4	WALLFETENA	Digital Output	highest VDD supply	External Wall FET Driver. Power domain is the highest out of WALLVDD, USBVDD or BATTVDD.
H4	NTCBIAS	Analogue Output	VPMIC	Battery NTC Temperature Monitor Supply
H5	NTCMON	Analogue Input		Battery NTC Temperature Monitor Voltage Sense Input
H9	BACKUPVDD	Supply		Secondary (Backup) Battery Supply
System LED Drivers				
J11	LED1	Digital Output	SYSVDD	Status LED Driver 1. Open Drain Output
K11	LED2	Digital Output		Status LED Driver 2. Open Drain Output
Do Not Connect				
C5, H3, M2, M3, N1, N2	DNC			Do Not Connect

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The WM8312 has been classified as MSL3.

CONDITION	MIN	MAX
OTP Programming Supply (PROGVDD)	-0.3V	7.0V
BATTVDD, WALLVDD and USBVDD supplies	-0.3V	7.0V
Input voltage for LDO regulators	-0.3V	7.0V
Input voltage for DC-DC converters	-0.3V	7.0V
Digital buffer supply (DBVDD1, DBVDD2)	-0.3V	4.5V
Voltage range for digital inputs	-0.3V	DBVDD + 0.3V
Operating Temperature Range, T_A	-40°C	+85°C
Junction Temperature, T_J	-40°C	+125°C
Thermal Impedance Junction to Ambient, θ_{JA}		45°C/W
Storage temperature prior to soldering	30°C max / 60% RH max	
Storage temperature after soldering	-65°C	+150°C
Soldering temperature (10 seconds)		+260°C
Note: These ratings assume that all ground pins are at 0V.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Wall Input power source	WALLVDD	4.3		5.5	V
Battery Input power source	BATTVDD	2.7		5.5	V
USB Input power source	USBVDD	4.3		5.5	V
Backup Battery power source	BACKUPVDD			3.6	V
Digital buffer supply	DBVDD1, DBVDD2	1.71		3.6	V
Touch Panel supply (see note 1)	TPVDD	1.71	2.5	3.6	V
OTP Programming Supply (see note2)	PROGVDD	6.25	6.5	6.75	V
Ground	GND, DBGND, TPGND, XOSCGND, REFGND		0		V

Notes:

1. When the Touch Panel Controller is enabled, then TPVDD must be connected to LDO13VOUT (2.5V). The min/max TPVDD conditions noted above do not apply when the Touch Panel Controller is enabled. (Note that, when the Touch Panel is not enabled, TPVDD is the power domain for GPIO pins 13-16.)

2. The OTP Programming Supply PROGVDD should only be present when programming the OTP. At other times, this pin should be left unconnected.

FEATURES OVERVIEW

POWER MANAGEMENT FUNCTIONS

REGULATOR (TYPE)	INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT	EXTERNAL COMPONENTS	FEATURES
DCDC1,2 (Buckwise™ Step-down)	SYSVDD	0.6V to 1.8V (12.5mV steps)	Up to1.2A	4.7µF to 47µF Output Capacitor 0.5µH to 2.2µH Inductor	- Best in class transient performance - Dynamic Voltage Scaling - Up to 91% efficiency - Selectable 2/4MHz Switching Frequency - FCCM, Auto and Hysteretic switching modes - Low Iq LDO mode
DCDC3 (Step-down)	SYSVDD	0.85V to 3.4V (25mV steps)	Up to 1.0A	10µF to 47µF Output Capacitor 2.2µH Inductor	- Up to 93% efficiency - 2MHz Switching Frequency - FCCM, Auto, Hysteretic switching modes - Low Iq LDO mode
DCDC4 (Step-up)	SYSVDD	7V to 30V	90mA@8V 40mA@20V 25mA@30V	N-FET+Schottky Diode, 1µF Output Capacitor,10µH Inductor, Resistor divider	- Output current regulation using ISINKn pins - Over voltage protection
ISINK1,2 (Current sink)	SYSVDD	0.5V to SYSVDD	2uA to 28mA		- Logarithmic scale for linear LED brightness change - Programable ramp up/down
LDO1	1.5V to SYSVDD	0.9V to 3.3V (50-100mV steps)	Up to 300mA	2.2µF Output Capacitor	- 5µA low Iq mode - Current limited Switch mode.
LDO2,3	1.5V to SYSVDD	0.9V to 3.3V (50-100mV steps)	Up to 200mA	2.2µF Output Capacitor	- 5µA low Iq mode - Current limited switch mode.
LDO4,5,6	1.5V to SYSVDD	0.9V to 3.3V (50-100mV steps)	Up to 100mA	2.2µF Output Capacitor	- 5µA Iq - Current limited Switch mode
LDO7,8	1.71V to 5.5V	1V to 3.5V (50-100mV steps)	Up to 200mA	1µF Output Capacitor	- 0.003%/mA load regulation, - 0.025%/V line regulation - 30uV output noise from 10Hz to 100kHz - 85dB PSRR
LDO9,10	1.71V to 5.5V	1V to 3.5V (50-100mV steps)	Up to 150mA	1µF Output Capacitor	- 0.004%/mA load regulation - 0.025%/V line regulation - 30µV output noise from 10Hz to 100kHz - 85dB PSRR
LDO11	1.8V to 5.5V	0.8 to 1.55 (50-100mV steps)	Up to 10mA		- Stable with any output capacitor or without - 2µA quiescent - Can be enabled in OFF state - Option to track DCDC1 voltage code
EPE1,2 / Sequenced Control Channel	n/a	n/a	n/a	n/a	- Control channel for external regulator or devices. - Can be sequenced as if it was an internal regulator
LDO12 (VPMIC)	n/a	2.1V	Internal use only	0.1µF Output Capacitor	- Internal Supply (always ON)
LDO13	n/a	2.5V	Up to 20mA	1µF Output Capacitor	- Internal supply when ON - Used for Touch Panel (TPVDD)

Table 1 Regulator Feature Summary

Note: SYSVDD range is 2.7V to 5.5V

The WM8312 provides 4 DC-DC Converters and 11 LDO Regulators. The DC-DC Converters comprise 3 step-down (Buck) converters (including 2 Buckwise™ valley-mode converters) and 1 step-up (Boost) converter. The Regulators comprise general purpose LDOs (LDO1 - LDO6) and low-noise analogue LDOs (LDO7 - LDO10). The analogue LDOs offer superior PSRR, noise and load-transient performance. LDO11 is a low power LDO intended for powering "always on" circuits connected to the WM8312; this LDO can be configured to remain enabled in the OFF state.

These power management components are designed to support application processors and associated peripherals. DC-DC1 and DC-DC2 are intended to provide power to the processor voltage domains; DC-DC3 is suitable for powering memory circuits or for use as a pre-regulator for the LDOs. The output voltage of each of the buck converters and regulators is programmable in software through control registers.

The WM8312 can execute programmable sequences of enabling and disabling the DC-DC Buck Converters and LDO Regulators as part of the transitions between the ON, OFF and SLEEP power states. The WM8312 power management circuits can also interface with configurable hardware control functions supported via GPIO pins. These include GPIO inputs for selecting alternate voltages or operating modes, and GPIO outputs for controlling external power management circuits.

The configuration of the power management circuits, together with some of the GPIO pins and other functions, may be stored in the integrated OTP memory. This avoids any dependence on a host processor to configure the WM8312 at start-up.

BUCKWISE™ TECHNOLOGY

The Buckwise™ Converter is the first Valley mode DCDC converter integrated into a system PMIC. This technology has several key benefits:

FEATURE	BENEFIT
Market leading transient performance	- Able to use smaller capacitors to meet processor transient requirements. - Processors able to operate at lower voltages (saving power) without hitting minimum voltage specifications
Only system PMIC with Valley Mode Control (VMC)	- Ensures there is no performance degradation at low output voltages (0.6V) - Will support next gen processors (<45nm) with low voltage requirements.
>90% efficiency dc-dc	- Longer battery life in portable devices
Multiple modes of operation	- Maintains high efficiency across the full load range, increasing battery life
Dedicated Dynamic Voltage Scaling (DVS) with 1 register write or hardwired pin.	- Allows the regulator to go from one voltage output to another with a programmable slew rate. - Enables processor to switch seamlessly between power modes for optimum processor performance at the lowest possible power

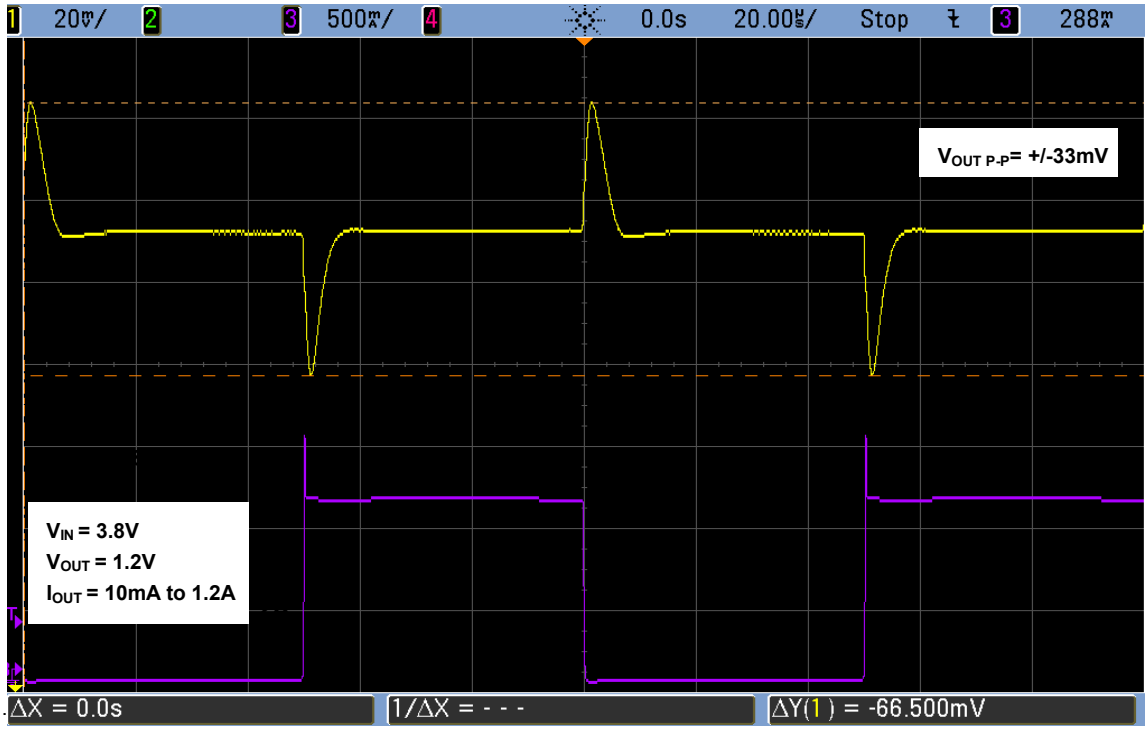


Figure 1 Buckwise™ Load Transient Response

Note: C_{out}=22µF, L_{out}=0.5µH, Load rise time =200ns

NON VOLATILE MEMORY SYSTEM CONFIGURATION

- Customisable standard product using the OTP NVM to store system startup sequence and regulator voltage defaults
- InstantConfig™ external EEPROM based development mode to facilitate rapid system prototyping
- PCB production line or in-factory configuration flows for OTP are supported.
- All main application processor startup requirements catered for with 5 startup/shutdown slots and flexible GPIO and Interrupt model.

The WM8312 is a highly configurable device which can be tailored specifically to the requirements of a complex system application. The sequencing and voltage control of the integrated DC-DC Converters and LDOs in power-up, shut-down and SLEEP conditions can be programmed in 5 startup and shutdown slots. Together with a flexible GPIO and interrupt model this allows the WM8312 to be a customized solution for each application. The WM8312 reads system configuration information from both the internal OTP NVM and an external EEPROM, if connected.

In the development phase the WM8312 allows designers to modify or experiment with different settings of the control sequences by writing to the applicable registers in the OFF state prior to commanding an 'ON' state transition. Configuration settings can also be stored on an external EEPROM and loaded onto the WM8312 as required. In this case the external EEPROM data takes precedence over any data programmed into the internal non volatile memory.

For production use the WM8312 provides an on-chip OTP non volatile memory, in which the essential parameters for starting up the device can be programmed. This allows the WM8312 to start up and shut down the system with no dependency on any other devices for application-specific configuration parameters. The WM8312 is normally supplied with the customer's system configuration data pre-programmed, however there is an alternate flow where the device can program itself with data from an external EEPROM when on the PCB.

POWER STATES

The WM8312 has 6 main power states, which are described below. Different levels of functionality are associated with each of the power states. Some of the state transitions are made autonomously by the WM8312 (eg. transitions to/from BACKUP are scheduled according to the available power supply conditions). Other transitions are initiated as a result of instructions issued over the Control Interface or as a result of software functions (eg. Watchdog timer) or hardware functions such as the ON pin. The valid transitions and the associated conditions are detailed below.

NO POWER - This is the device state when no power is available. All functions are disabled and all register data is lost.

OFF - This is the device state when power is available but the device is switched off. The RTC is enabled and the register map contents are maintained. The RST pin is pulled low in this state. LDO11 may optionally be enabled in this state; all other DC-DCs and LDOs are disabled.

ON - This is the normal operating state when the device is switched on. All device functions are available in this state.

SLEEP - This is a user-configurable operating state which is intended for a low-power operating condition. Selected functions may be enabled, disabled or re-configured according to the user's requirements. A programmable configuration sequence for the DC-DCs and LDOs is executed on transition to/from SLEEP mode.

BACKUP - This is the operating state when the available power supplies are below the reset threshold of the device. Typically, this means that USB or Wall supplies are not present and that the main battery is either discharged or removed. The RTC and oscillator and a 'software scratch' memory area can be maintained from the backup battery (if available) in this state. All other functions and registers are reset in BACKUP. (Note that, for power saving, an 'unclocked' mode, in which the RTC is held constant, may be selected if required.)

PROGRAM - This is a special operating state which is used for programming the integrated OTP memory with the device configuration data. The settings stored in the OTP define the device configuration in the ON state, and also the time/sequencing data associated with ON/OFF power state transitions.

The valid power state transitions are illustrated in Figure 2.

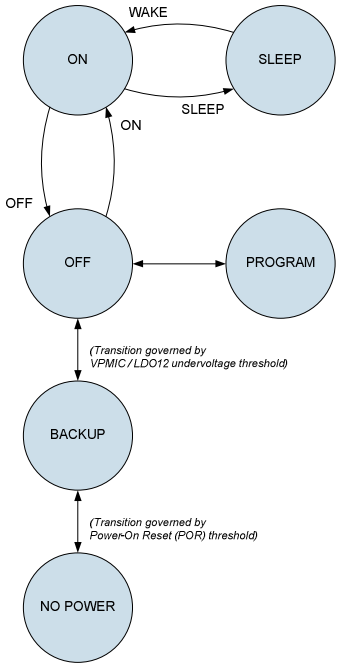


Figure 2 Power States and Transitions

State transitions to/from the NO POWER state are controlled automatically by the internal supply (VPMIC) voltage generated by LDO12. The device is in the NO POWER state when this voltage is below the Power-On Reset (POR) threshold.

State transitions to/from the BACKUP state are controlled automatically by the internal supply (VPMIC) voltage generated by LDO12. The device is in the BACKUP state when this voltage is below the Device Reset threshold.

State transitions to/from the PROGRAM state are required to follow specific control sequences.

The remaining transitions between the OFF, ON and SLEEP states may be initiated by a number of different mechanisms - some of them automatic, some of them user-controlled. Transitions between these states are time-controlled sequences of events are programmable, using data stored in the integrated OTP memory or else data loaded from an external InstantConfig™ EEPROM memory

.

BACKUP DOMAIN FOR RTC AND SYSTEM CONFIGURATION RETENTION

- Clocked Backup state quiescent current of 2uA with RTC running
- Unclocked Backup state quiescent current of 100nA with RTC paused
- Up to 5 minutes of data retention with a 22uF on VPMIC (LDO12VOUT) in unclocked backup state
- Automatic transition to backup power source
- 32kHz Crystal oscillator
- RTC with alarm function
- Secure-RTC tamper detection mechanism for unauthorised updates to the RTC
- Dedicated backup battery charger
  - Programmable output voltage 2.5V or 3.1V
  - CC or CC/CV charging modes
  - Programmable current 100µA to 400µA
  - Charging status flag
  - Automatic isolation of charger when SYSVDD headroom is low

STATE	CURRENT DRAW	COMMENTS
BACKUP	0.1µA	RTC disabled
	2µA	RTC enabled
OFF	8µA	RTC enabled
ON/SLEEP	365µA	DCDC1,2,3 LDO1-6 on, but in low power modes
	1.9mA	DCDC1,2,3 LDO1-6 on normal mode
	2.7mA	All regulators enabled, normal mode

Table 2 System Power Consumption

POWER PATH MANAGEMENT

- Integrated 100mΩ USB and battery switches (external battery P-FET control output)
- Programmable USB current limit from 2.5mA to 1.8A
- External wall P-FET driver with variable drive strength
- System power supplemented from Battery when USB current limit reached.
- Charger current throttling when USB current limit reached
- Hot switching between WALL and USB power sources
- System startup with dead battery when external power applied.
- Dead battery can be automatically charged when external power applied.

The WM8312 can take its power supply from a Wall adaptor, a USB interface or from a single-cell lithium battery. The WM8312 autonomously chooses the most appropriate power source available, and supports hot-swapping between sources (ie. the system can remain in operation while different sources are connected and disconnected).

Comparators within the WM8312 identify which apower supplies are available and select the power source in the following order of preference:

1. Wall adaptor (WALLVDD)
2. USB power rail (USBVDD)
3. Battery (BATTVDD)

Note that the Wall supply is normally the first choice of supply, provided that it is within the operating limits. The WM8312 can operate with any combination of these power supplies, or with just a single supply.

When WALLVDD or USBVDD is selected as the power source, this may be used to charge the Battery, using the integrated battery charger circuit.

The recommended connections between the WM8312 and the WALL, USB and Battery supplies are illustrated in Figure 3. Note that the external FET components may be omitted in some applications.

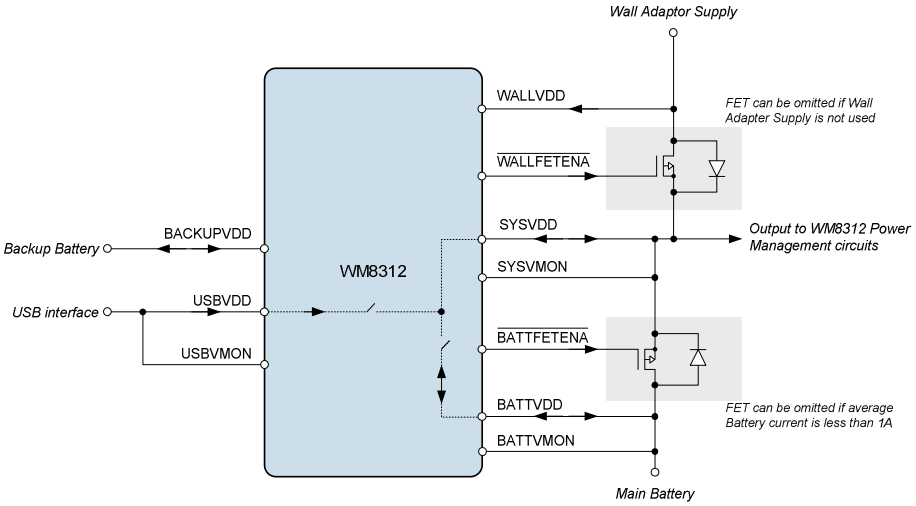


Figure 3 WM8312 Power Supply Connections

1A LI-ION BATTERY CHARGER

- Automomous charge and re-charge cycle
- Programmable 50mA to 1000mA Fast charge current
- Programmable 50mA to 200mA Trickle charge
- Programmable EOC Voltage 4.05 to 4.2V
- Charge top off status bit
- EOC detection via current or timeout
- Fault protection via NTC connection
- Charge current monitor output
- Charge status LED indicator

The WM8312 incorporates a battery charger which is designed for charging single-cell lithium batteries. The battery charger can operate from either the Wall or USB power sources. The battery charger implements constant-current (CC) and constant-voltage (CV) charge methods, and can run automatically without any intervention required by the host processor.

The battery charger voltage and current are programmable. Trickle charging and fast charging modes are supported. In both modes, the SYSVDD voltage is monitored to ensure the power supply capacity or USB current limit is not exceeded. If the SYSVDD voltage drops to 3.9V, (eg. if the USB current limit has been reached), then the battery charge current is automatically reduced to try and prevent further voltage drop at SYSVDD.

Under high operating load conditions, the battery may be required to supplement the USB or Wall Adaptor power sources. Note that this capability is supported even when battery charging is enabled; in this case, the battery provides power to the system when required, and the charger resumes when sufficient current capacity is available.

Typical connections for the WM8312 battery charger are illustrated in Figure 4

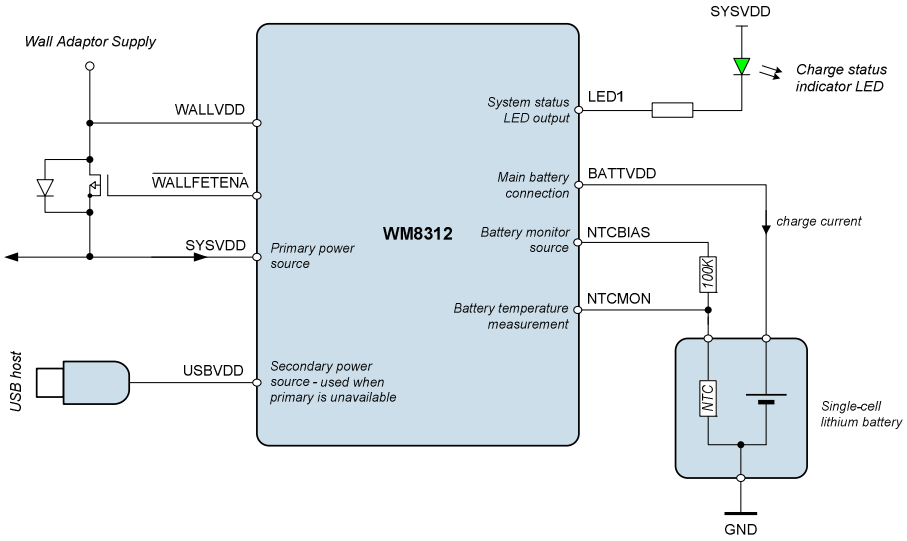


Figure 4 WM8312 Battery Charger Connections

AUXILLIARY ADC

- 12-Bit ADC for system supervision and resistive touch panel
- Monitor 4 external sources, plus key internal parameters and voltages
- Fully automatic mode for interleaving of samples between monitor inputs and touch panel
- 4 digital comparators with selectable input source.

The WM8312 incorporates a 12-bit Auxiliary ADC (AUXADC). This can be used to perform a number of system measurements (including supply voltages and battery temperature) and can also be used to measure analogue voltages from external sources and sensors.

External inputs to the AUXADC should be connected to the pins AUXADCIN1, AUXADCIN2, AUXADCIN3 and AUXADCIN4. The maximum voltage that can be measured is determined by the power domain associated with each. In the case of AUXADCIN 1-3, the maximum voltage is SYSVDD; in the case of AUXADCIN4, the maximum voltage is TPVDD. Note that SYSVDD varies according to the voltage of the preferred power source (WALLVDD, USBVDD or BATTVDD).

The AUXADC can also measure the voltage on WALLVDD, USBVDD and BATTVDD. Internal resistor dividers enable voltages higher than SYSVDD to be measured by the AUXADC - voltages up to 6V can be measured on these pins.

RESISTIVE TOUCH PANEL CONTROLLER

The WM8312 incorporates a Touch Panel controller interface, supporting standard resistive 4-wire and 5-wire panel types. The controller supports X, Y co-ordinate measurement and Pen Down detection. The 4-wire configuration also supports Touch Pressure (Z-axis) measurement.

The Touch Panel interfaces via GPIO pins 13-16. (In 5-wire mode, the AUXADCIN4 pin is also used.) The controller provides high resolution digitiser measurements, using the same 12-bit AUXADC as described above. Touch Panel conversion requests are automatically interleaved with AUXADC measurement requests by the 8312 AUXADC controller.

The Touch Panel can be enabled or disabled in the SLEEP state; Pen Down detection can be used to issue a WAKE request, including when the Touch Panel is disabled.

Touch Panel Interrupts can be generated on completion of a set of measurements, or on Pen Down detection. Read access to the Touch Panel measurement data is controlled in order to ensure the host always reads a complete set of data, and does not read mixed data that relates to separate measurement events.

SYSTEM CONTROL AND SUPERVISION

- I^2C or SPI compatible primary control interface
- Output fault monitoring on all regulator outputs (overcurrent or undervoltage) with programmable fault action
- Programmable system UV level
- Chip thermal monitor and programmable warning level interrupt
- Watchdog timer function
- Two-tier interrupts with full masking.
- Configurable GPIO power domain
- GPIO control for regulator functions for lower latency/flexibility

GPIOS

The WM8312 has 16 general-purpose input/output (GPIO) pins, GPIO1 - GPIO16. These can be configured as inputs or outputs, active high or active low, with optional on-chip pull-up or pull-down resistors. GPIO outputs can either be CMOS driven or Open Drain configuration. Each GPIO pin can be tri-stated and can also be used to trigger Interrupts. The function of each GPIO pin is selected individually. Different voltage power domains are selectable on a pin by pin basis for GPIOs 1-12, see Table 3

GPIO	DEFAULT POWER DOMAIN	ALTERNATE POWER DOMAIN
1-3,7-9	DBVDD	VPMIC (LDO12VOUT)
4-6,10-12	DBVDD	SYSVDD
13-16	TPVDD	n/a

Table 3 GPIO Power Domains

In addition to the default inputs and outputs, GPIOs have a wide range of secondary input and output functions. Input functions include power state change requests, DVS requests and hardware control of regulator modes. Outputs include functions such as power state notifications, 32kHz clock, DVS complete and system power or converter power good flags.

INTERRUPTS

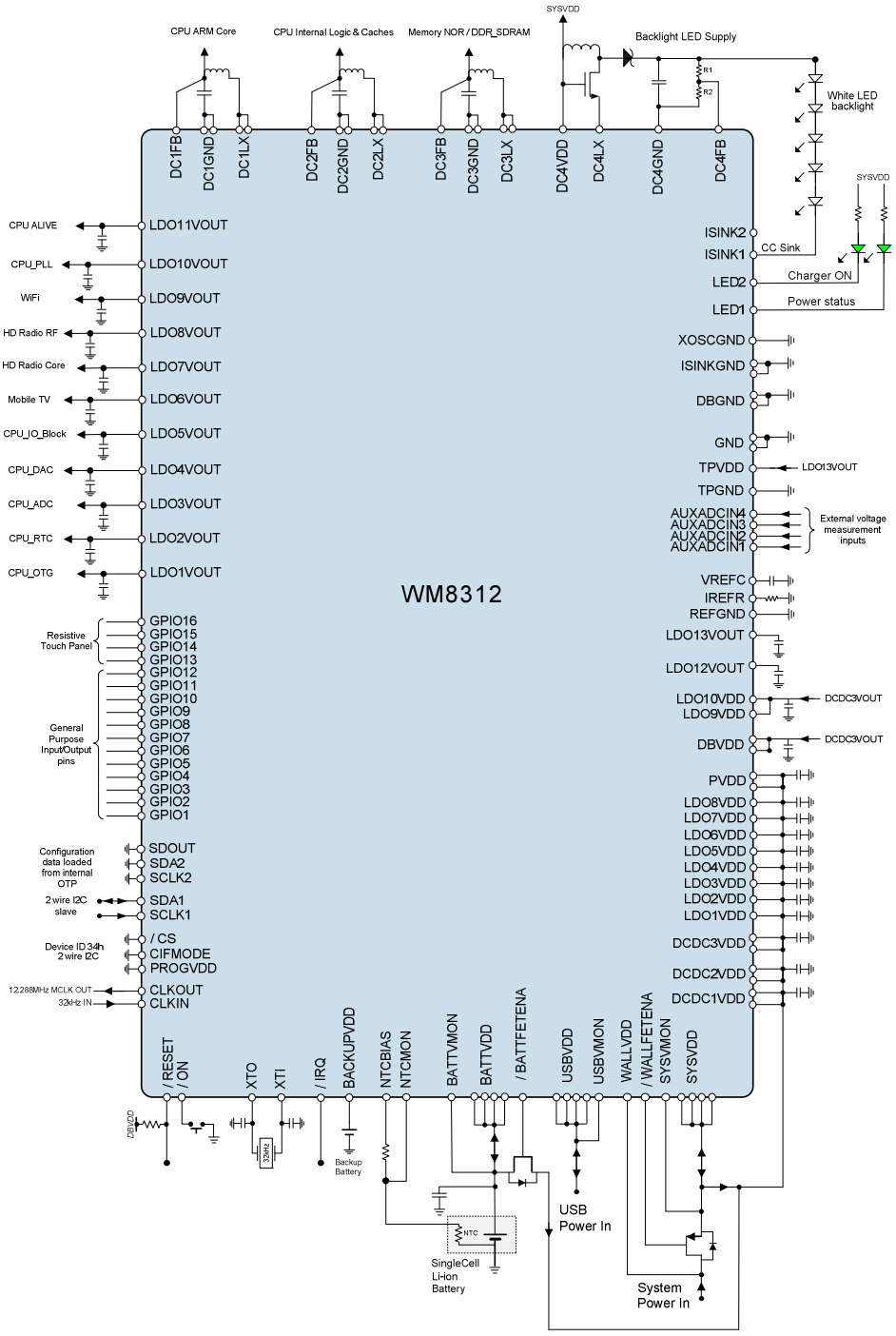
The WM8312 has a comprehensive Interrupt logic capability. The dedicated IRQ pin can be used to alert a host processor to selected events or fault conditions. Each of the interrupt conditions can be individually enabled or masked. Following an interrupt event, the host processor should read the interrupt registers in order to determine what caused the interrupt, and take appropriate action if required.

The WM8312 interrupt controller has two levels:

Secondary interrupts indicate a single event in one of the circuit blocks. The event is indicated by setting a register bit. This bit is a latching bit - once it is set, it remains at logic 1 even if the trigger condition is cleared. The secondary interrupts are cleared by writing a logic 1 to the relevant register bit. Note that reading the register does not clear the secondary interrupt.

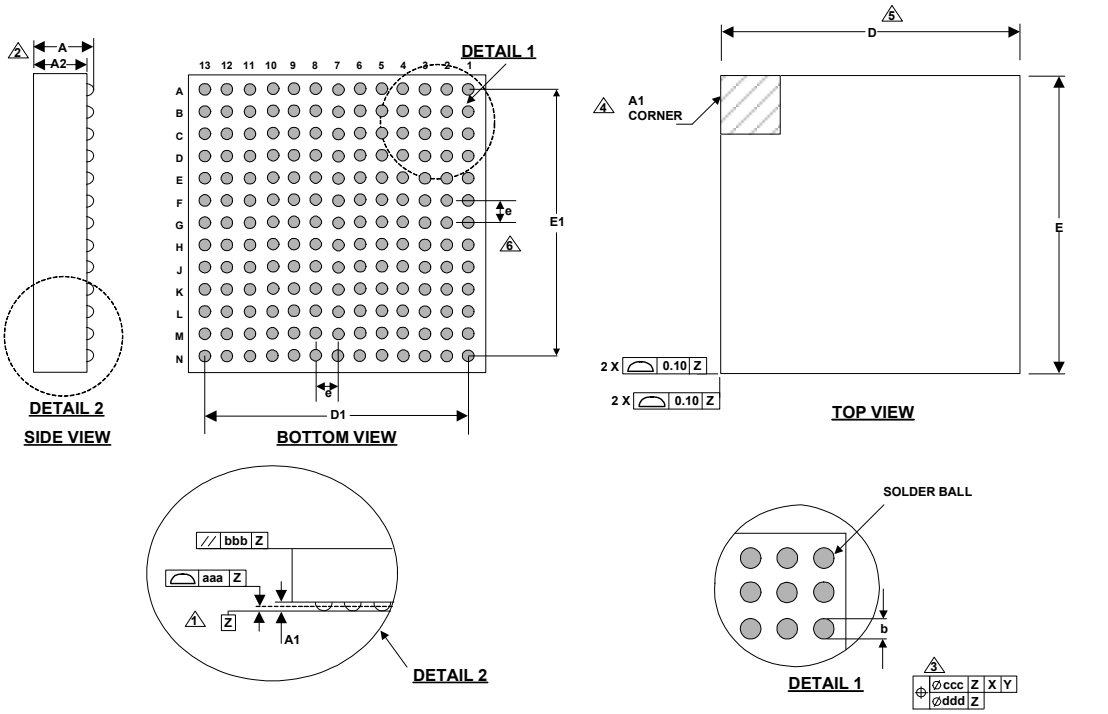
Primary interrupts are the logical OR of the associated secondary interrupts (usually all the interrupts associated with one particular circuit block). Each of the secondary interrupts can be individually masked or enabled as an input to the corresponding primary interrupt.

TYPICAL CONNECTIONS



PACKAGE DIAGRAM

B: 169 BALL BGA PLASTIC PACKAGE 7 x 7 x 1.17 mm BODY, 0.50 mm BALL PITCH **DM062.B**



Symbols		Dimensions (mm)		
	MIN	NOM	MAX	NOTE
A		1.17	1.27	
A1	0.17	0.21	0.26	
A2	0.91	0.96	1.01	
b	0.25	0.30	0.35	
D		7.00 BSC		
D1		6.00 BSC		
E		7.00 BSC		
E1		6.00 BSC		
e		0.50 BSC		6
Tolerances of Form and Position				
aaa	0.08			
bbb	0.10			
ccc	0.15			
ddd	0.05			
REF:	JEDEC, MO-195			

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1'.
3. DIMENSION 'b' IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -Z-.
4. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
5. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
6. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
8. FALLS WITHIN JEDEC, MO-195

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