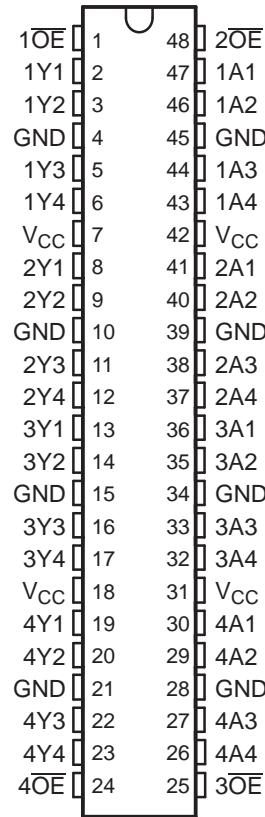


## FEATURES

- Member of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

**SN54LVT16244B . . . WD PACKAGE  
SN74LVT16244B . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)**



## DESCRIPTION/ORDERING INFORMATION

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^\circ\text{C}$ to $85^\circ\text{C}$	FBGA – GRD	Reel of 1000	SN74LVT16244BGRDR	VD244B
	FBGA – ZRD (Pb-free)		SN74LVT16244BZRDR	
	SSOP – DL	Tube of 25	SN74LVT16244BDL	LVT16244B
			SN74LVT16244BDLG4	
		Reel of 1000	SN74LVT16244BDLDR	
			74LVT16244BDLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVT16244BDGGR	LVT16244B
			74LVT16244BDGGRG4	
	TVSOP – DGV	Reel of 2000	SN74LVT16244BDGVR	VD244B
			74LVT16244BDGVRE4	
$-55^\circ\text{C}$ to $125^\circ\text{C}$	VFBGA – GQL	Reel of 1000	SN74LVT16244BGQLR	VD244B
	VFBGA – ZQL (Pb-free)		SN74LVT16244BZQLR	
$-55^\circ\text{C}$ to $125^\circ\text{C}$	CFP – WD	Tube	SNJ54LVT16244BWD	SNJ54LVT16244BWD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

**SN54LVT16244B, SN74LVT16244B  
3.3-V ABT 16-BIT BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

SCBS716E-MARCH 2000-REVISED DECEMBER 2006

 **TEXAS  
INSTRUMENTS**  
www.ti.com

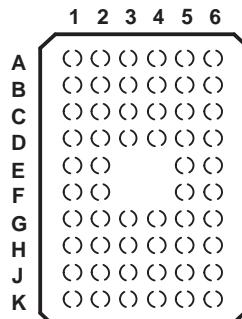
**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

The 'LVT16244B devices are 16-bit buffers and line drivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**GQL OR ZQL PACKAGE  
(TOP VIEW)**

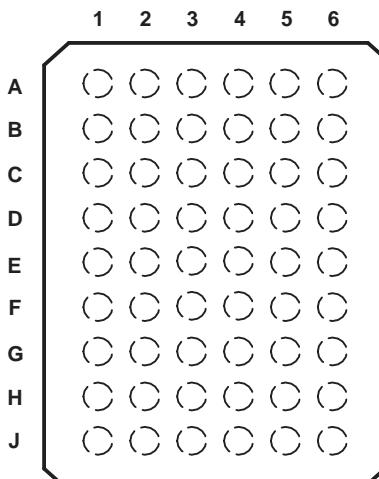


**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
A	1 $\overline{OE}$	NC	NC	NC	NC	2 $\overline{OE}$
B	1Y2	1Y1	GND	GND	1A1	1A2
C	1Y4	1Y3	$V_{CC}$	$V_{CC}$	1A3	1A4
D	2Y2	2Y1	GND	GND	2A1	2A2
E	2Y4	2Y3			2A3	2A4
F	3Y1	3Y2			3A2	3A1
G	3Y3	3Y4	GND	GND	3A4	3A3
H	4Y1	4Y2	$V_{CC}$	$V_{CC}$	4A2	4A1
J	4Y3	4Y4	GND	GND	4A4	4A3
K	4 $\overline{OE}$	NC	NC	NC	NC	3 $\overline{OE}$

(1) NC – No internal connection

**GRD OR ZRD PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(54-Ball GRD/ZRD Package)**

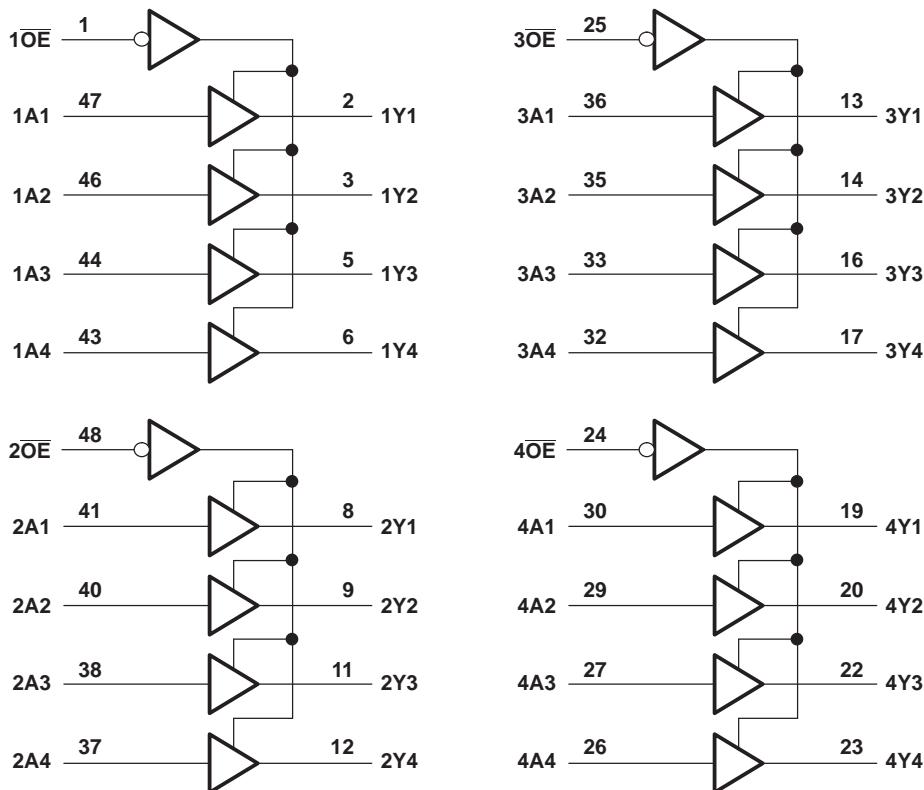
	1	2	3	4	5	6
A	1Y1	NC	1 $\overline{OE}$	2 $\overline{OE}$	NC	1A1
B	1Y3	1Y2	NC	NC	1A2	1A3
C	2Y1	1Y4	$V_{CC}$	$V_{CC}$	1A4	2A1
D	2Y3	2Y2	GND	GND	2A2	2A3
E	3Y1	2Y4	GND	GND	2A4	3A1
F	3Y3	3Y2	GND	GND	3A2	3A3
G	4Y1	3Y4	$V_{CC}$	$V_{CC}$	3A4	4A1
H	4Y3	4Y2	NC	NC	4A2	4A3
J	4Y4	NC	4 $\overline{OE}$	3 $\overline{OE}$	NC	4A4

(1) NC – No internal connection

FUNCTION TABLE  
(EACH 4-BIT BUFFER)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DGV, DL, and WD packages.

**SN54LVT16244B, SN74LVT16244B  
3.3-V ABT 16-BIT BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

SCBS716E-MARCH 2000-REVISED DECEMBER 2006



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>		-0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		-0.5	7	V
$V_O$	Voltage range applied to any output in the high state <sup>(2)</sup>		-0.5	$V_{CC} + 0.5$	V
$I_O$	Current into any output in the low state	SN54LVT16244B	96	mA	
		SN74LVT16244B	128		
$I_O$	Current into any output in the high state <sup>(3)</sup>	SN54LVT16244B	48	mA	
		SN74LVT16244B	64		
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA	
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA	
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package	70	°C/W	
		DGV package	58		
		DL package	63		
		GQL/ZQL package	42		
		GRD/ZRD package	36		
$T_{stg}$	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This current flows only when the output is in the high state and  $V_O > V_{CC}$ .

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

		SN54LVT16244B <sup>(2)</sup>		SN74LVT16244B		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage			0.8	0.8	V
$V_I$	Input voltage			5.5	5.5	V
$I_{OH}$	High-level output current			-24	-32	mA
$I_{OL}$	Low-level output current			48	64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate			200	200	μs/V
$T_A$	Operating free-air temperature			-55	125	°C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Product preview

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVT16244B <sup>(1)</sup>			SN74LVT16244B			UNIT
		MIN	TYP <sup>(2)</sup>	MAX	MIN	TYP <sup>(2)</sup>	MAX	
$V_{IK}$	$V_{CC} = 2.7 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 2.7 \text{ to } 3.6 \text{ V}$ , $I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$			$V_{CC} - 0.2$			V
	$V_{CC} = 2.7 \text{ V}$ , $I_{OH} = -8 \text{ mA}$	2.4			2.4			
	$V_{CC} = 3 \text{ V}$	$I_{OH} = -24 \text{ mA}$	2				2	
$V_{OL}$		$I_{OH} = -32 \text{ mA}$						V
$V_{CC} = 2.7 \text{ V}$	$I_{OL} = 100 \mu\text{A}$	0.2		0.2				
	$I_{OL} = 24 \text{ mA}$	0.5		0.5				
	$I_{OL} = 16 \text{ mA}$	0.4		0.4				
	$I_{OL} = 32 \text{ mA}$	0.5		0.5				
$V_{CC} = 3 \text{ V}$	$I_{OL} = 48 \text{ mA}$	0.55						
	$I_{OL} = 64 \text{ mA}$			0.55				
$I_I$	$V_{CC} = 0 \text{ or } 3.6 \text{ V}$ , $V_I = 5.5 \text{ V}$		50		10			$\mu\text{A}$
	$V_{CC} = 3.6 \text{ V}$ , $V_I = V_{CC} \text{ or GND}$		$\pm 1$		$\pm 1$			
	$V_{CC} = 3.6 \text{ V}$	$V_I = V_{CC}$	1		1			
$I_{off}$		$V_I = 0$	-5		-5			$\mu\text{A}$
$V_{CC} = 0$ , $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$				$\pm 100$				
$I_{OZH}$	$V_{CC} = 3.6 \text{ V}$ , $V_O = 3 \text{ V}$		5		5			$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 3.6 \text{ V}$ , $V_O = 0.5 \text{ V}$		-5		-5			$\mu\text{A}$
$I_{OZPU}$	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$ , $V_O = 0.5 \text{ V} \text{ to } 3 \text{ V}$ , $\text{OE} = \text{don't care}$		$\pm 100^{(3)}$		$\pm 100$			$\mu\text{A}$
$I_{OZPD}$	$V_{CC} = 1.5 \text{ V} \text{ to } 0$ , $V_O = 0.5 \text{ V} \text{ to } 3 \text{ V}$ , $\text{OE} = \text{don't care}$		$\pm 100^{(3)}$		$\pm 100$			$\mu\text{A}$
$I_{CC}$	$V_{CC} = 3.6 \text{ V}$ , $I_O = 0$ , $V_I = V_{CC} \text{ or GND}$	Outputs high	0.19		0.19			mA
		Outputs low	5		5			
		Outputs disabled	0.19		0.19			
$\Delta I_{CC}^{(4)}$	$V_{CC} = 3 \text{ V} \text{ to } 3.6 \text{ V}$ , One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC} \text{ or GND}$		0.2		0.2			mA
$C_I$	$V_I = 3 \text{ V} \text{ or } 0$		4		4			pF
$C_O$	$V_O = 3 \text{ V} \text{ or } 0$		9		9			pF

(1) Product preview

(2) All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

**SN54LVT16244B, SN74LVT16244B  
3.3-V ABT 16-BIT BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

SCBS716E-MARCH 2000-REVISED DECEMBER 2006



**Switching Characteristics**

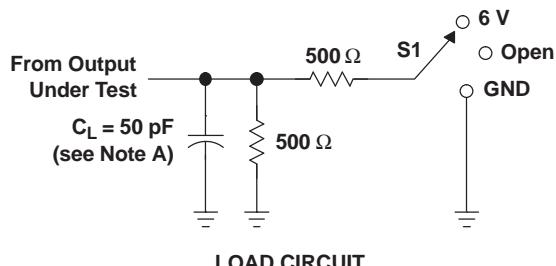
over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16244B <sup>(1)</sup>		SN74LVT16244B				UNIT	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP <sup>(2)</sup>	MAX	
$t_{PLH}$	A	Y	1.1	4.4	4.6	1.2	2.3	3.2	3.7	ns
$t_{PHL}$			1.1	3.6	3.9	1.2	2	3.2	3.7	
$t_{PZH}$	$\overline{OE}$	Y	1.1	4.6	5.4	1.2	2.6	4	5	ns
$t_{PZL}$			1.1	5.4	6.2	1.2	2.7	4	5	
$t_{PHZ}$	$\overline{OE}$	Y	1.6	5.7	6.2	2.2	3.3	4.5	5	ns
$t_{PLZ}$			1.2	5	4.7	2	3.1	4.2	4.4	
$t_{sk(LH)}$								0.5		ns
$t_{sk(HL)}$								0.5		

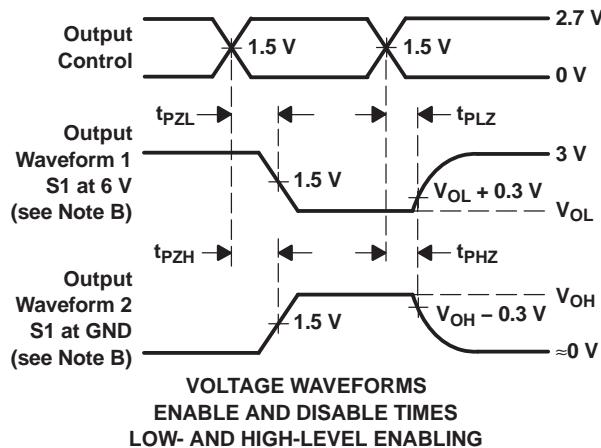
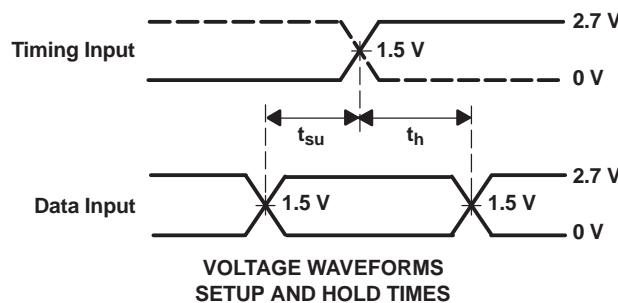
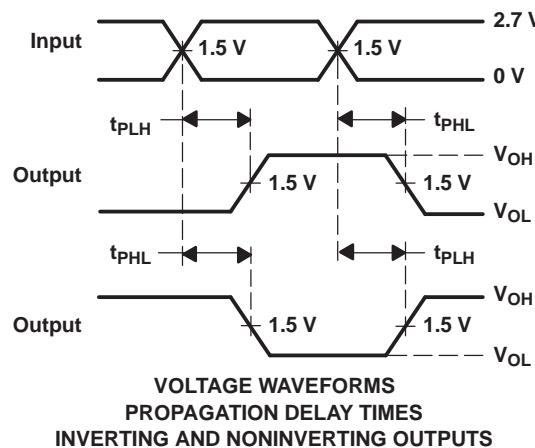
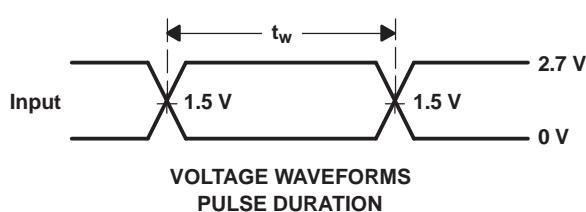
(1) Product preview

(2) All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $\text{PRR} \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVT16244BDGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16244B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT16244BDGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16244B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT16244BDGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VD244B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT16244BDL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16244B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT16244BDLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16244B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT16244BDLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16244B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT16244BGQLR	OBsolete	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	-40 to 85		
SN74LVT16244BZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	VD244B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT16244BZRDR	ACTIVE	BGA MICROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	VD244B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

---

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

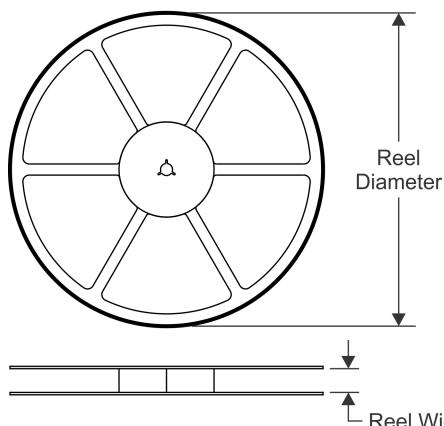
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

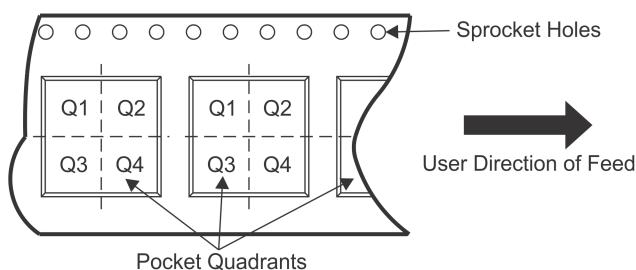
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT16244BDGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74LVT16244BDGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVT16244BDLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVT16244BZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74LVT16244BZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1

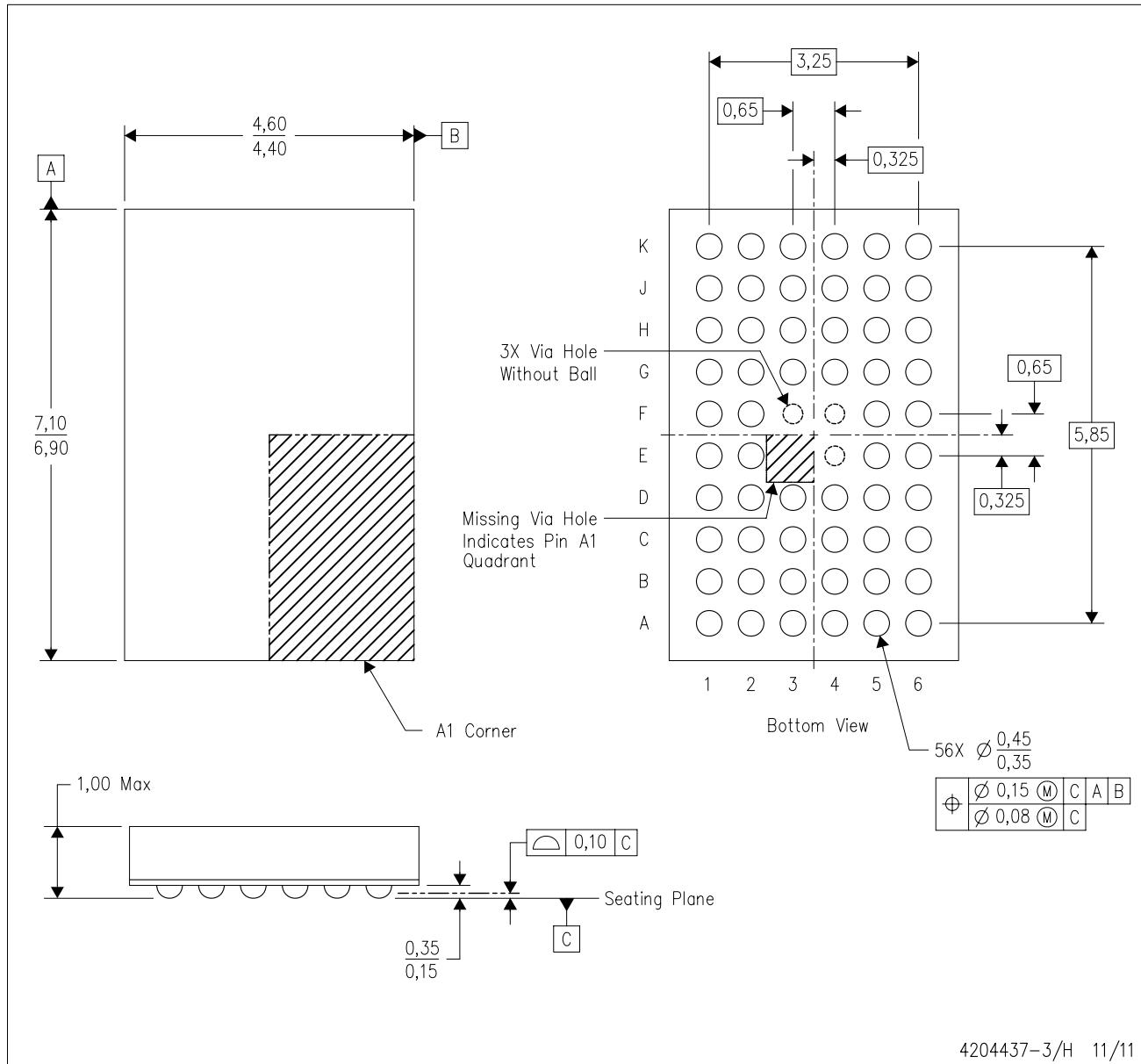
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT16244BDGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVT16244BDGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
SN74LVT16244BDLR	SSOP	DL	48	1000	367.0	367.0	55.0
SN74LVT16244BZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	336.6	336.6	28.6
SN74LVT16244BZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	336.6	336.6	28.6

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



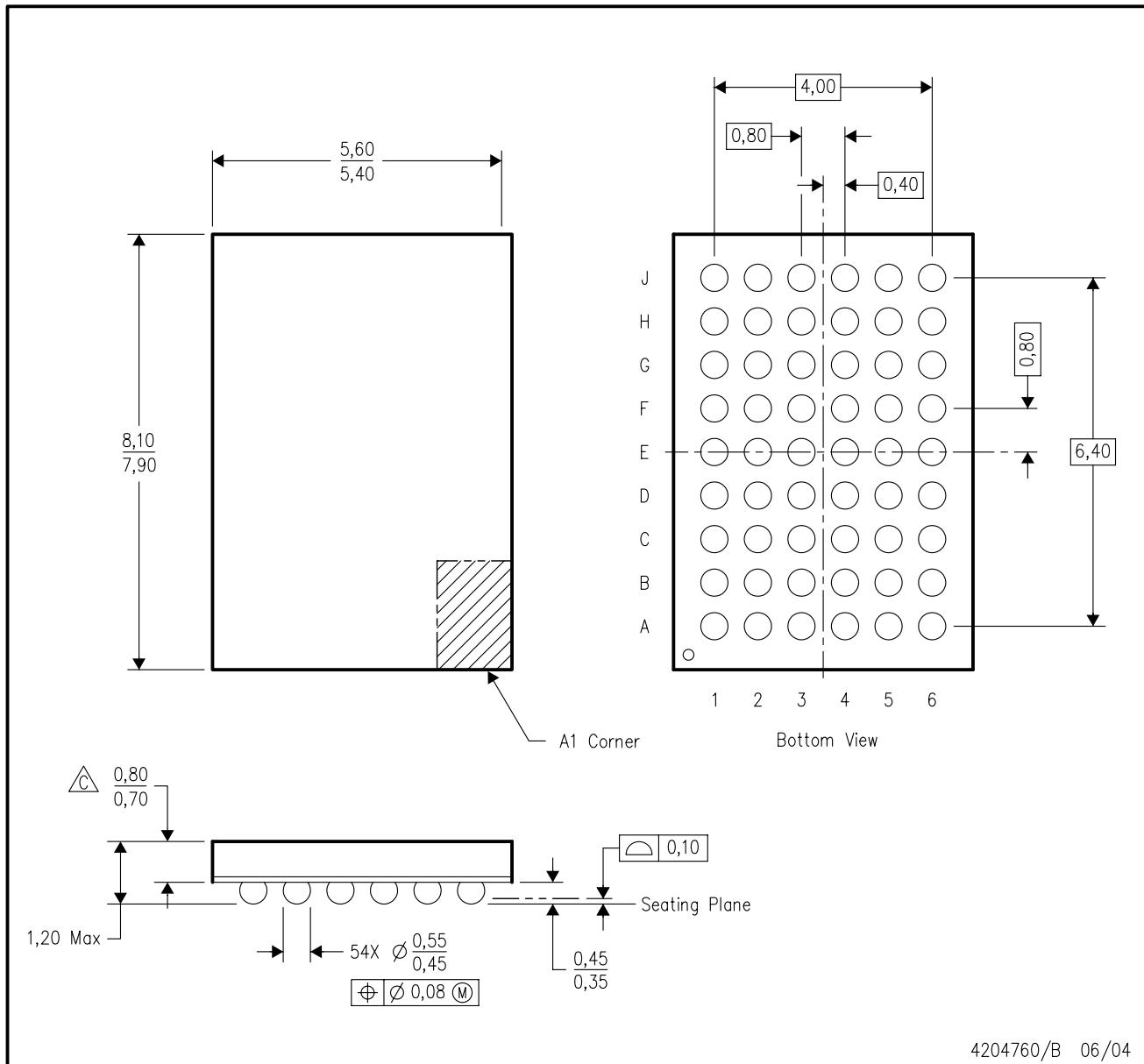
4204437-3/H 11/11

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-285 variation BA-2.
- This package is Pb-free. Refer to the 56 QGL package (drawing 4200583) for tin-lead (SnPb).

## ZRD (R-PBGA-N54)

## PLASTIC BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.

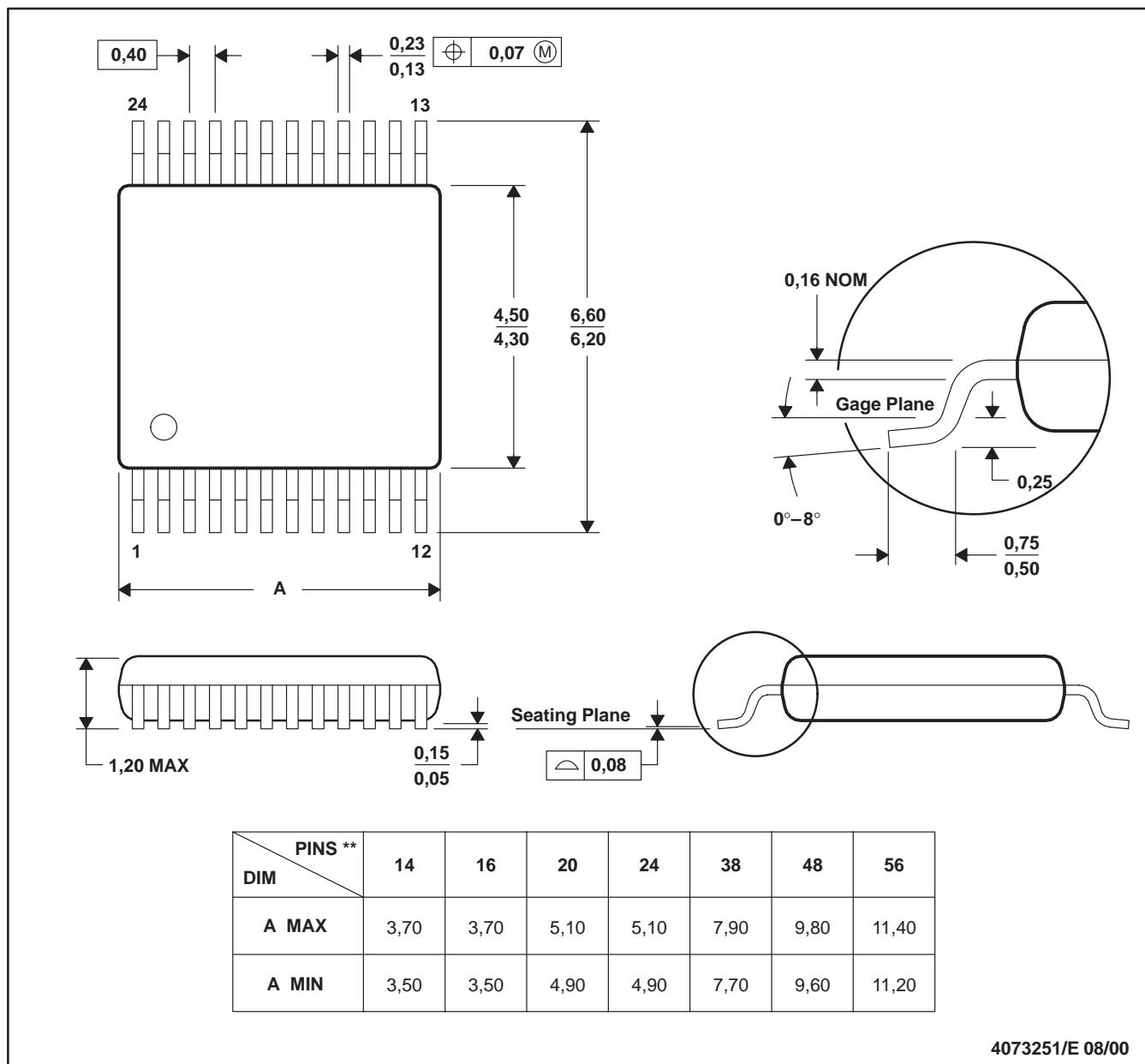
Falls within JEDEC MO-205 variation DD.

D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

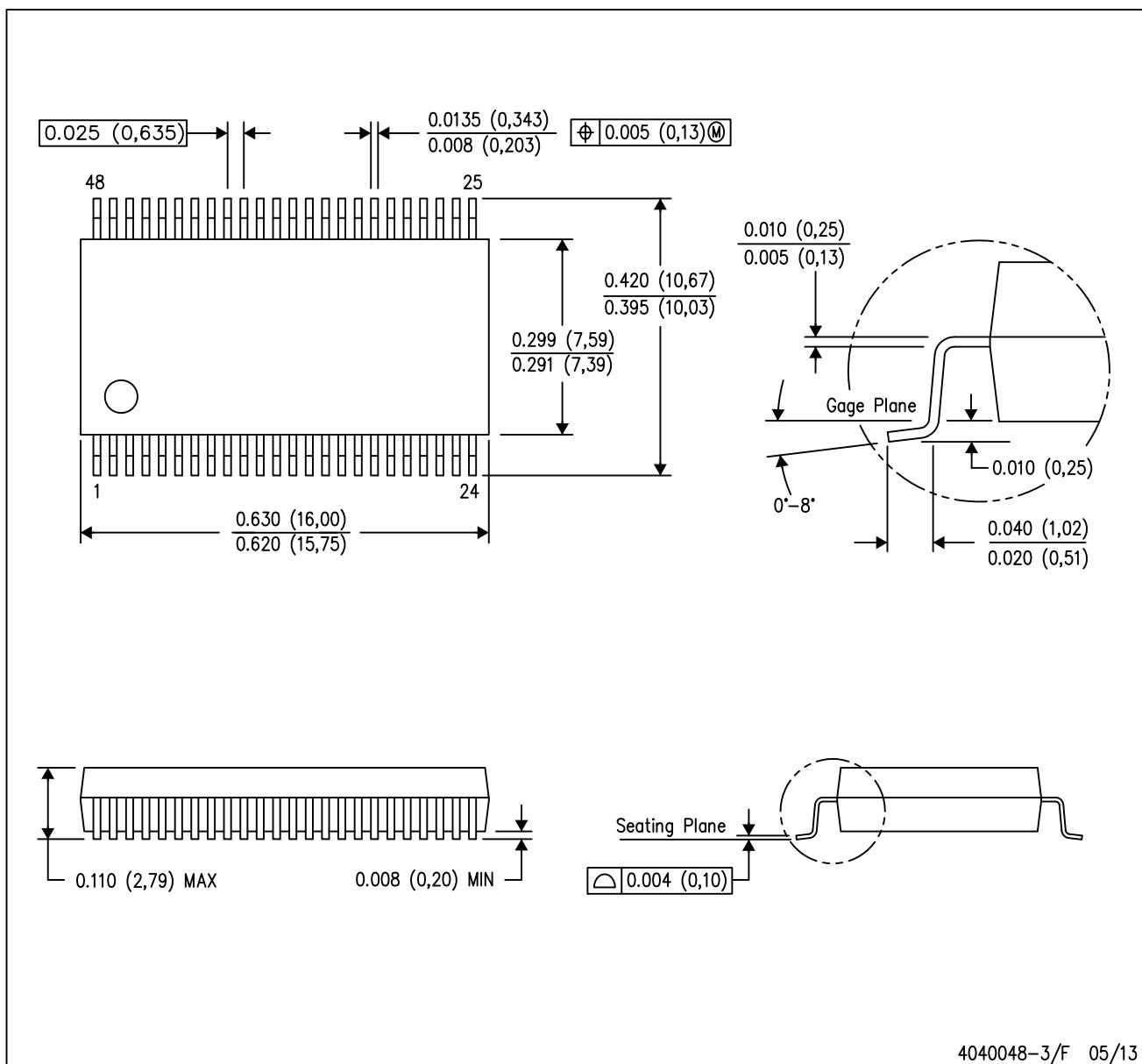
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



4040048-3/F 05/13

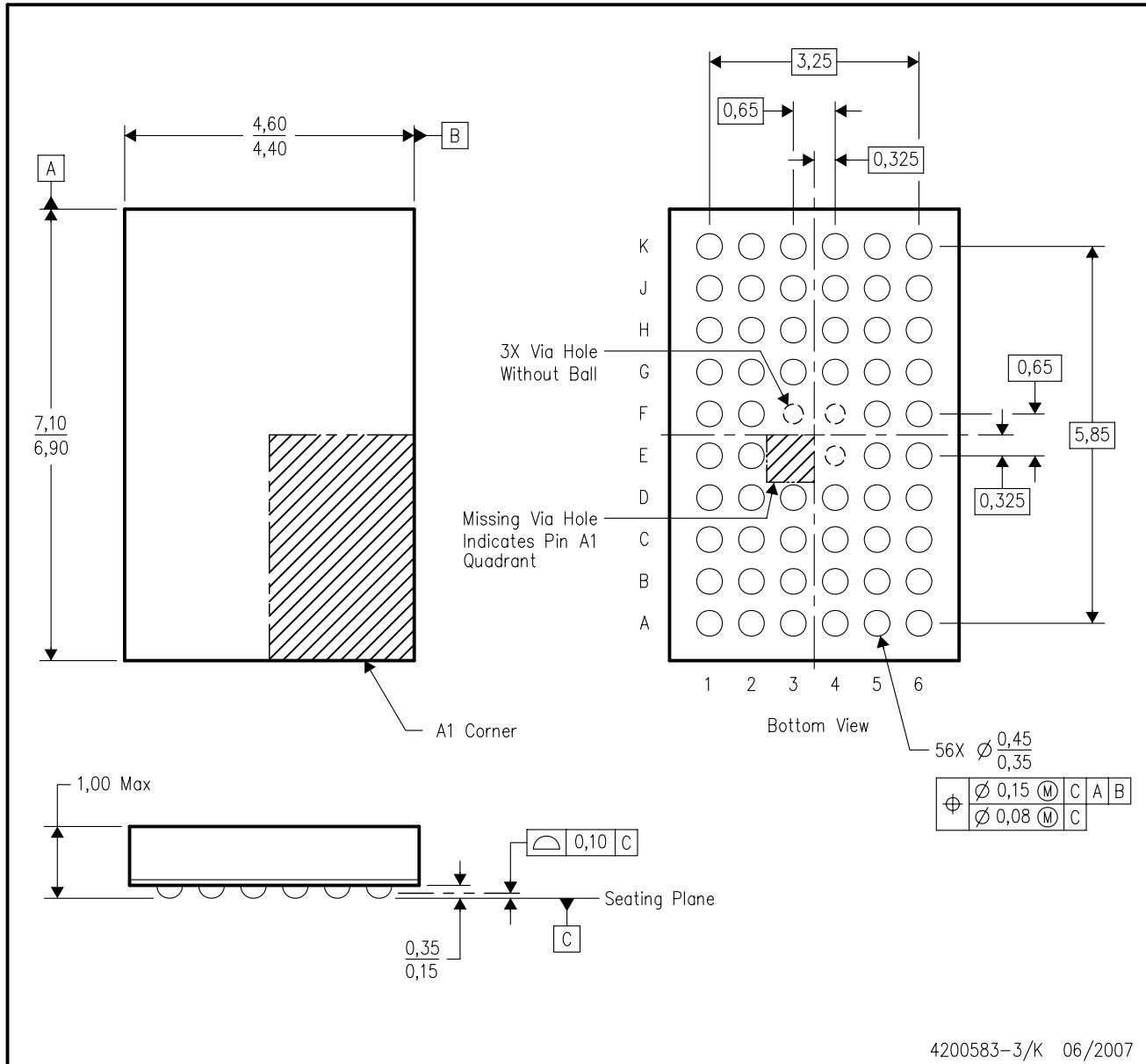
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

## GQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY



4200583-3/K 06/2007

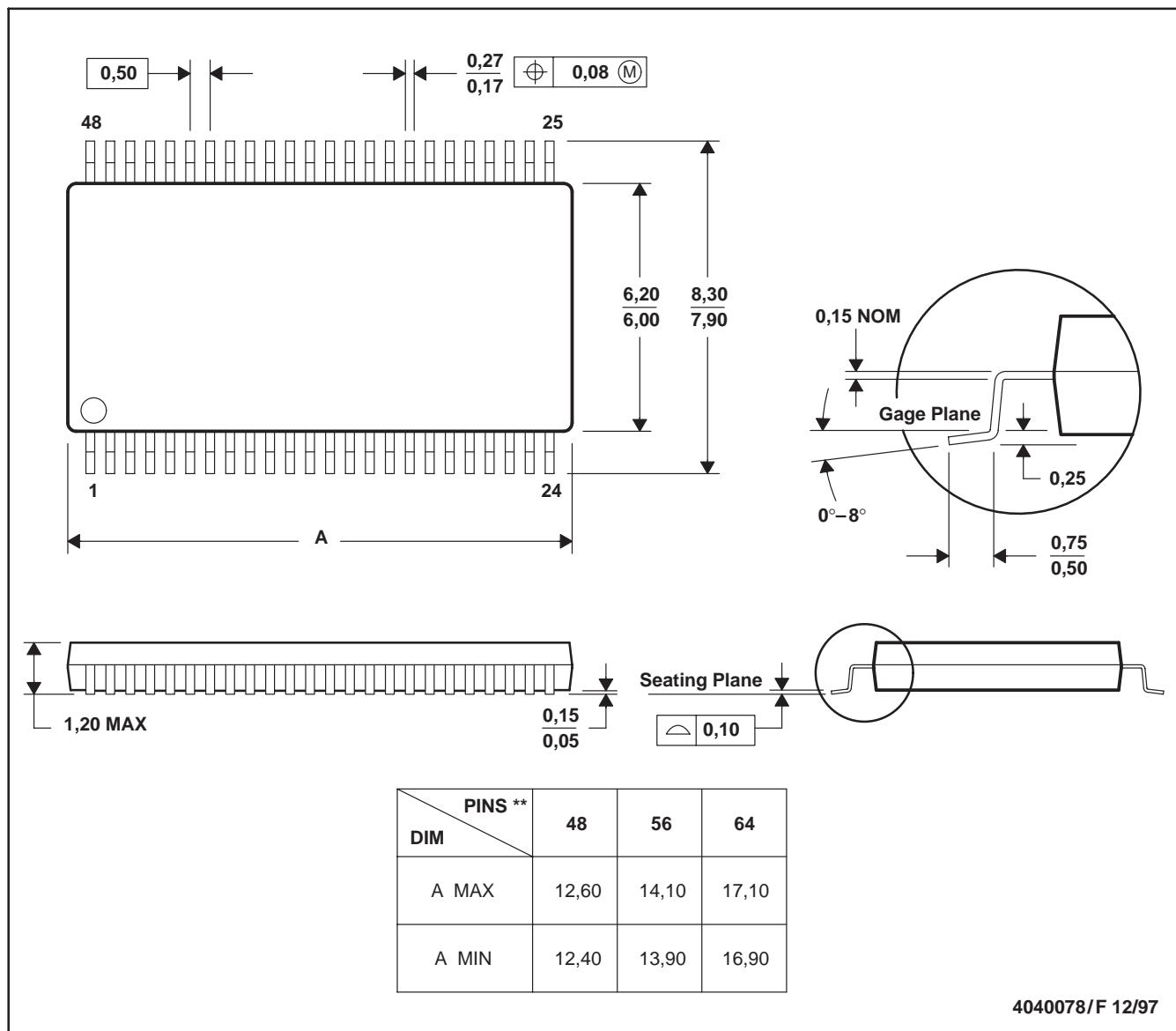
NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-285 variation BA-2.
- This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>
	<b>TI E2E Community</b>
	<a href="http://e2e.ti.com">e2e.ti.com</a>