40V, 2A Synchronous Buck-Boost DC/DC Converter

FEATURES

- **Wide V_{IN} Range: 2.7V to 40V**
- **Wide V_{OUT} Range: 2.7V to 40V**
- **0.8A Output Current for $V_{IN} \geq 3.6V$, $V_{OUT} = 5V$**
- **2A Output Current in Step-Down Operation for $V_{IN} \geq 6V$**
- **Programmable Frequency: 100kHz to 2MHz**
- Synchronizable Up to 2MHz with an External Clock
- Up to 95% Efficiency
- 30µA No-Load Quiescent Current in Burst Mode® Operation
- Ultralow Noise Buck-Boost PWM
- Internal Soft-Start
- 3µA Supply Current in Shutdown
- Programmable Input Undervoltage Lockout
- Small 4mm × 5mm × 0.75mm DFN Package
- Thermally Enhanced 20-Lead TSSOP Package

APPLICATIONS

- 24V/28V Industrial Applications
- Automotive Power Systems
- Telecom, Servers and Networking Equipment
- FireWire Regulator
- Multiple Power Source Supplies

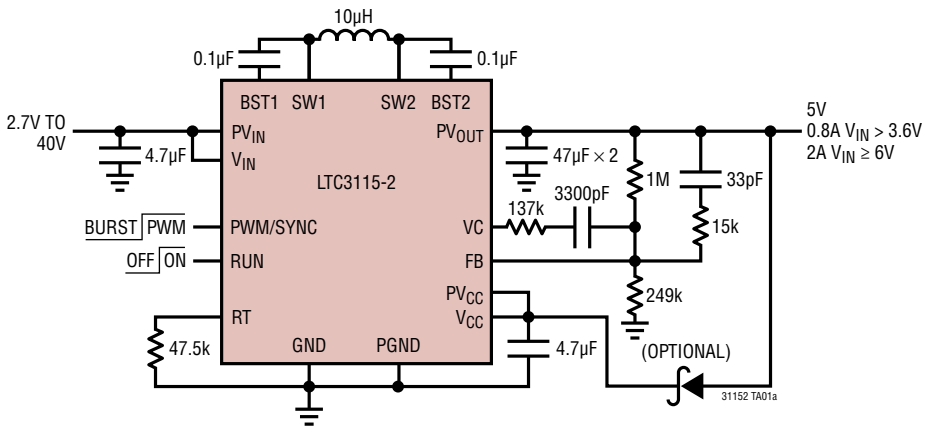
DESCRIPTION

The LTC®3115-2 is a high voltage monolithic synchronous buck-boost DC/DC converter optimized for applications subject to fast (<1ms) input voltage transients. For all other applications, the LTC3115-1 is recommended. With its wide 2.7V to 40V input and output voltage ranges, the LTC3115-2 is well suited for use in a wide variety of automotive and industrial power supplies. A proprietary low noise switching algorithm optimizes efficiency with input voltages that are above, below or even equal to the output voltage and ensures seamless transitions between operational modes.

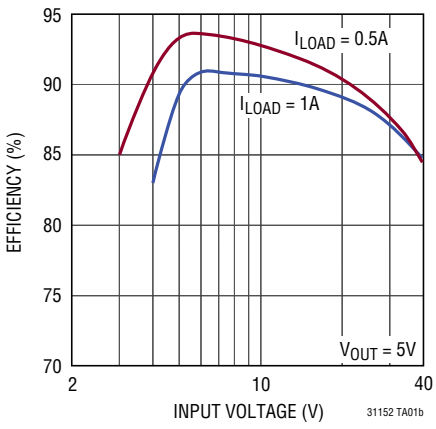
Programmable frequency PWM mode operation provides low noise, high efficiency operation and the ability to synchronize switching to an external clock. Switching frequencies up to 2MHz are supported to allow use of small value inductors for miniaturization of the application circuit. Pin selectable Burst Mode operation reduces standby current and improves light load efficiency which, combined with a 3µA shutdown current, make the LTC3115-2 ideally suited for battery-powered applications. Additional features include output disconnect in shutdown, short-circuit protection and internal soft-start. The LTC3115-2 is available in thermally enhanced 16-lead 4mm × 5mm × 0.75mm DFN and 20-lead TSSOP packages.

TYPICAL APPLICATION

5V, 750kHz Wide Input Voltage Range Buck-Boost Regulator



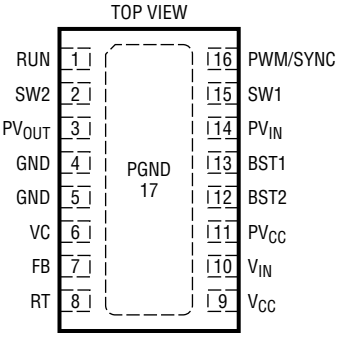
Efficiency vs V_{IN}



ABSOLUTE MAXIMUM RATINGS (Note 1)

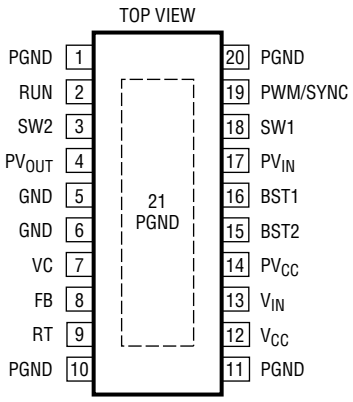
V_{IN}, PV_{IN}, PV_{OUT} ..... –0.3V to 45V
V_{SW1}
DC ..... –0.3V to (PV_{IN} + 0.3V)
Pulsed (<100ns) ..... –1.5V to (PV_{IN} + 1.5V)
V_{SW2}
DC ..... –0.3V to (PV_{OUT} + 0.3V)
Pulsed (<100ns) ..... –1.5V to (PV_{OUT} + 1.5V)
V_{RUN} ..... –0.3V to (V_{IN} + 0.3V)
V_{BST1} ..... V_{SW1} – 0.3V to V_{SW1} + 6V
V_{BST2} ..... V_{SW2} – 0.3V to V_{SW2} + 6V
$V_{PWM/SYNC}$ ..... –0.3V to 6V
Voltage, All Other Pins ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 4)
LTC3115E-2/LTC3115I-2 ..... –40°C to 125°C
LTC3115H-2 ..... –40°C to 150°C
LTC3115MP-2 ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE ..... 300°C

PIN CONFIGURATION



DHD PACKAGE
16-LEAD (5mm × 4mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 38°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 21) IS PGND, MUST BE SOLDERED TO PCB FOR RATED THERMAL PERFORMANCE

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3115EDHD-2#PBF	LTC3115EDHD-2#TRPBF	31152	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 125°C
LTC3115IDHD-2#PBF	LTC3115IDHD-2#TRPBF	31152	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 125°C
LTC3115EFE-2#PBF	LTC3115EFE-2#TRPBF	LTC3115FE-2	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3115IFE-2#PBF	LTC3115IFE-2#TRPBF	LTC3115FE-2	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3115HFE-2#PBF	LTC3115HFE-2#TRPBF	LTC3115FE-2	20-Lead Plastic TSSOP	–40°C to 150°C
LTC3115MPFE-2#PBF	LTC3115MPFE-2#TRPBF	LTC3115FE-2	20-Lead Plastic TSSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are for T_A = 25°C (Note 2). PV_{IN} = V_{IN} = 24V, PV_{OUT} = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Operating Voltage		●	2.7		40	V
Output Operating Voltage		●	2.7		40	V
Input Undervoltage Lockout Threshold	V_{IN} Falling V_{IN} Rising V_{IN} Rising (0°C to 125°C)	● ●		2.4 2.6	2.7 2.8 2.725	V V V
Input Undervoltage Lockout Hysteresis				100		mV
V_{CC} Undervoltage Lockout Threshold	V_{CC} Falling	●		2.4	2.6	V
V_{CC} Undervoltage Lockout Hysteresis				200		mV
Input Current in Shutdown	V_{RUN} = 0V			3	10	µA
Input Quiescent Current in Burst Mode Operation	V_{FB} = 1.1V (Not Switching), $V_{PWM/SYNC}$ = Low			50		µA
Oscillator Frequency	R_T = 35.7k, $V_{PWM/SYNC}$ = High	●	900	1000	1100	kHz
Oscillator Operating Frequency	$V_{PWM/SYNC}$ = High	●	100		2000	kHz
PWM/SYNC Clock Input Frequency		●	100		2000	kHz
PWM/SYNC Input Logic Threshold		●	0.5	1.0	1.5	V
Soft-Start Duration				9		ms
Feedback Voltage		●	977	1000	1017	mV
Feedback Voltage Line Regulation	V_{IN} = 2.7V to 40V			0.1		%
Feedback Pin Input Current				1	50	nA
RUN Pin Input Logic Threshold		●	0.3	0.8	1.1	V
RUN Pin Comparator Threshold	V_{RUN} Rising	●	1.16	1.21	1.26	V
RUN Pin Hysteresis Current				500		nA
RUN Pin Hysteresis Voltage				100		mV
Inductor Current Limit	(Note 3)	●	2.4	3.0	3.7	A
Reverse Inductor Current Limit	Current into PV_{OUT} (Note 3)			1.5		A
Burst Mode Inductor Current Limit	(Note 3)		0.65	1.0	1.35	A
Maximum Duty Cycle	Percentage of Period SW2 is Low in Boost Mode, R_T = 35.7k (Note 5)	●	90	95		%
Minimum Duty Cycle	Percentage of Period SW1 is High in Buck Mode, R_T = 35.7k (Note 5)	●			0	%
SW1, SW2 Minimum Low Time	R_T = 35.7k (Note 5)			100		ns
N-Channel Switch Resistance	Switch A (From PV_{IN} to SW1) Switch B (From SW1 to PGND) Switch C (From SW2 to PGND) Switch D (From PV_{OUT} to SW2)			150 150 150 150		mΩ mΩ mΩ mΩ
N-Channel Switch Leakage	PV_{IN} = PV_{OUT} = 40V			0.1	10	µA
PV_{CC}/V_{CC} External Forcing Voltage			4.58		5.5	V
V_{CC} Regulation Voltage	I_{VCC} = 1mA		4.33	4.45	4.58	V
V_{CC} Load Regulation	I_{VCC} = 1mA to 20mA			1.2		%
V_{CC} Line Regulation	I_{VCC} = 1mA, V_{IN} = 5V to 40V			0.5		%
V_{CC} Current Limit	V_{CC} = 2.5V		50	110		mA
V_{CC} Dropout Voltage	I_{VCC} = 5mA, V_{IN} = 2.7V			50		mV
V_{CC} Reverse Current	V_{CC} = 5V, V_{IN} = 3.6V			10		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3115-2 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3115E-2 is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are ensured by design, characterization and correlation with statistical process controls. The LTC3115I-2 specifications are guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3115H-2 specifications are guaranteed over the –40°C to 150°C operating junction temperature range. The LTC3115MP-2 specifications are guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade

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operating lifetime; operating lifetime is derated for junction temperatures greater than 125°C. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} is the thermal impedance of the package.

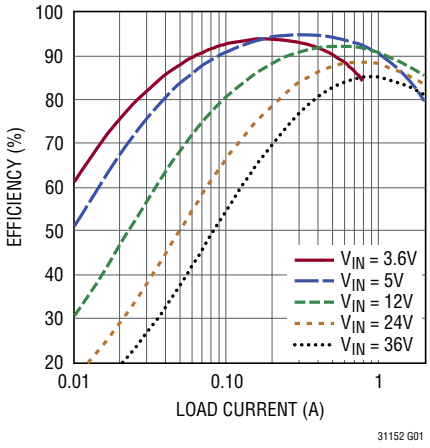
Note 3: Current measurements are performed when the LTC3115-2 is not switching. The current limit values measured in operation will be somewhat higher due to the propagation delay of the comparators.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

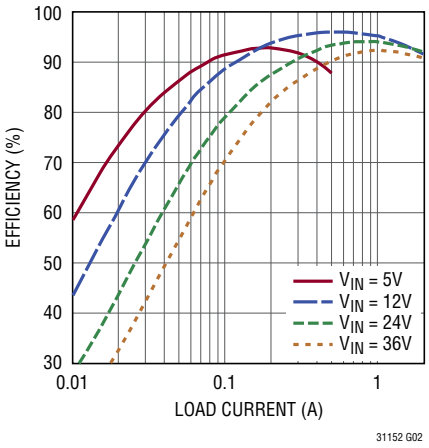
Note 5: Switch timing measurements are made in an open-loop test configuration. Timing in the application may vary somewhat from these values due to differences in the switch pin voltage during the non-overlap durations when switch pin voltage is influenced by the magnitude and direction of the inductor current.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

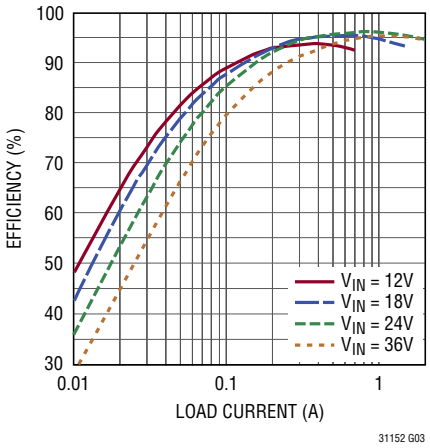
PWM Mode Efficiency, V_{OUT} = 5V, f_{SW} = 500kHz, Non-Bootstrapped



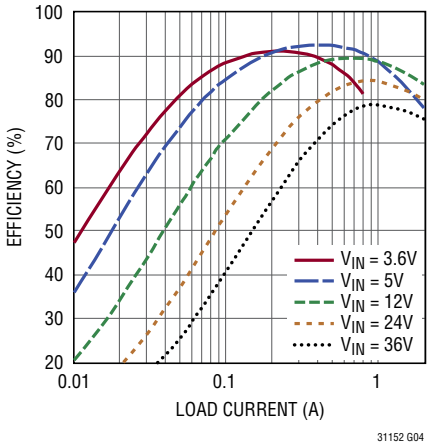
PWM Mode Efficiency, V_{OUT} = 12V, f_{SW} = 500kHz



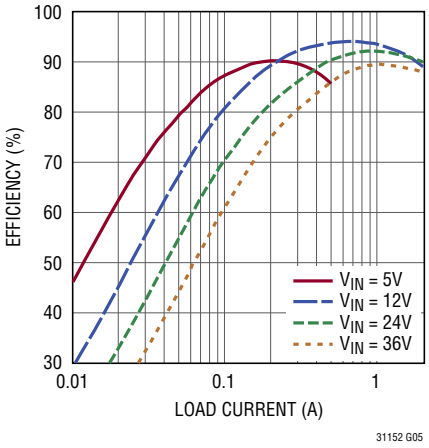
PWM Mode Efficiency, V_{OUT} = 24V, f_{SW} = 500kHz



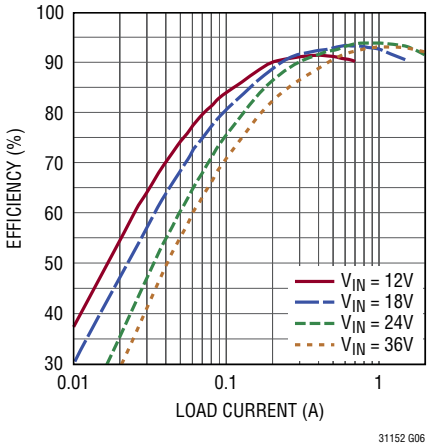
PWM Mode Efficiency, V_{OUT} = 5V, f_{SW} = 1MHz, Non-Bootstrapped



PWM Mode Efficiency, V_{OUT} = 12V, f_{SW} = 1MHz

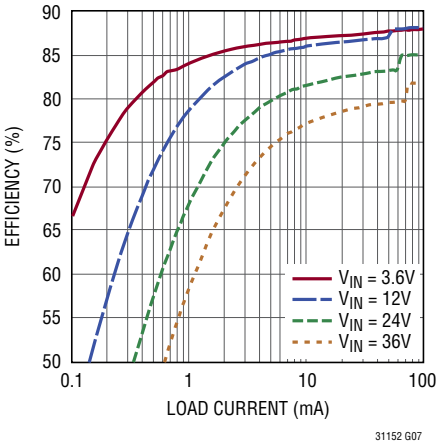


PWM Mode Efficiency, V_{OUT} = 24V, f_{SW} = 1MHz

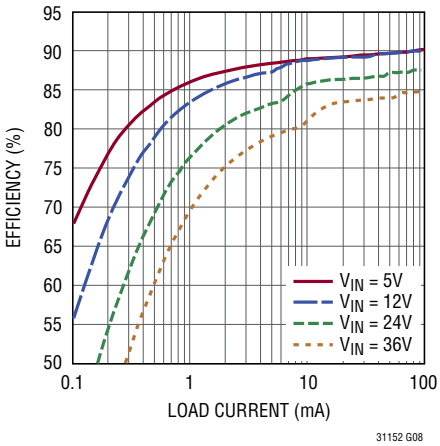


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

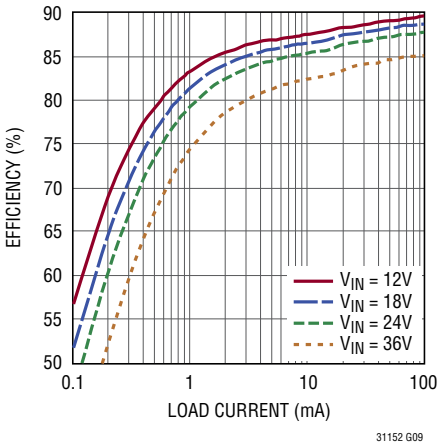
Burst Mode Efficiency, V_{OUT} = 5V, L = 15µH, Non-Bootstrapped



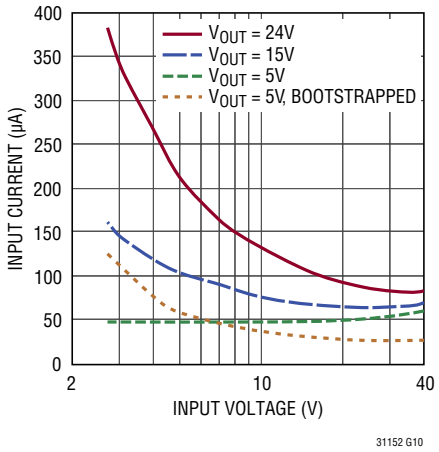
Burst Mode Efficiency, V_{OUT} = 12V, L = 15µH



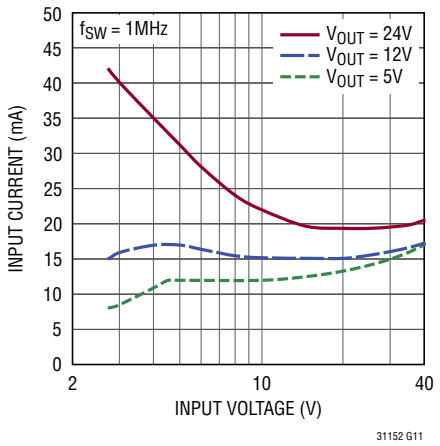
Burst Mode Efficiency, V_{OUT} = 24V, L = 15µH



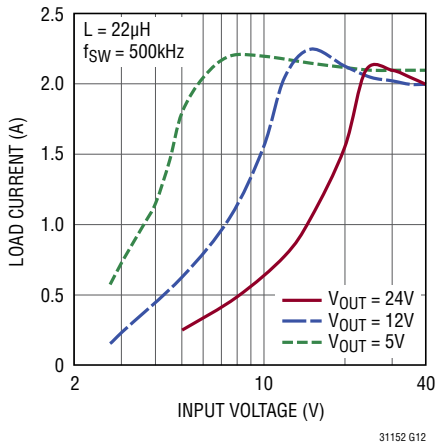
Burst Mode No-Load Input Current vs V_{IN}



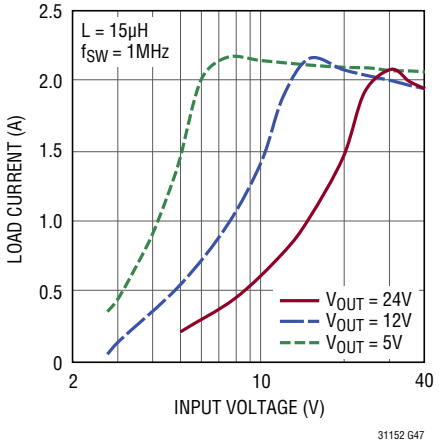
PWM Mode No-Load Input Current vs V_{IN}



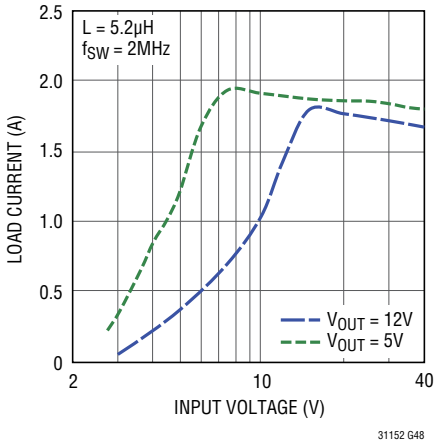
Maximum Load Current vs V_{IN}, PWM Mode



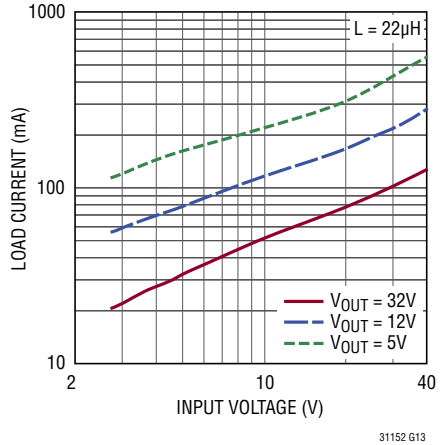
Maximum Load Current vs V_{IN}, PWM Mode



Maximum Load Current vs V_{IN}, PWM Mode

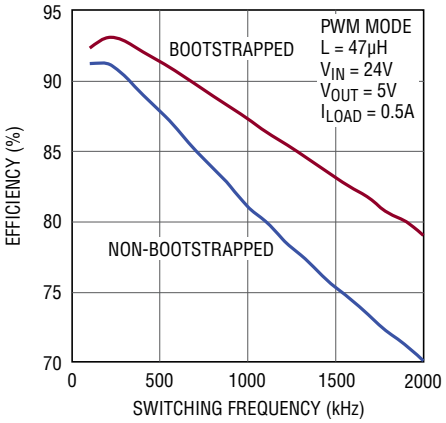


Maximum Load Current vs V_{IN}, Burst Mode Operation



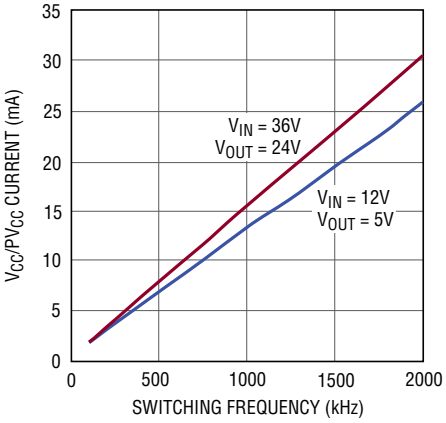
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Efficiency vs Switching Frequency



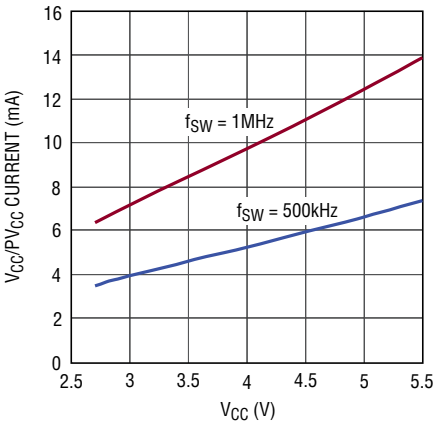
31152 G14

Combined V_{CC}/PV_{CC} Supply Current vs Switching Frequency



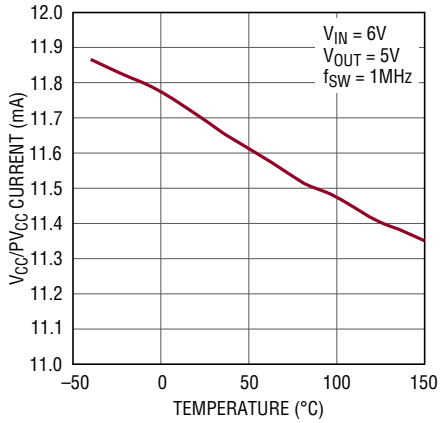
31152 G15

Combined V_{CC}/PV_{CC} Supply Current vs V_{CC}



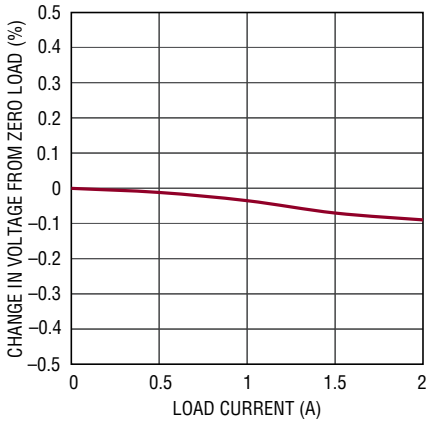
31152 G16

Combined V_{CC}/PV_{CC} Supply Current vs Temperature



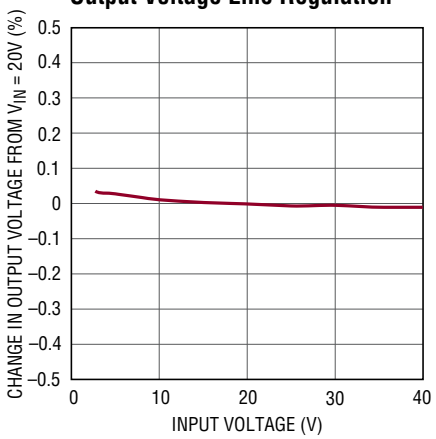
31152 G17

Output Voltage Load Regulation



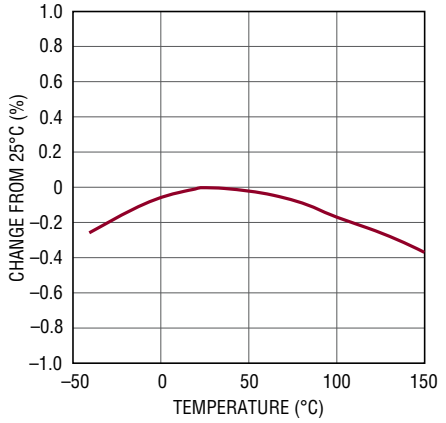
31152 G18

Output Voltage Line Regulation



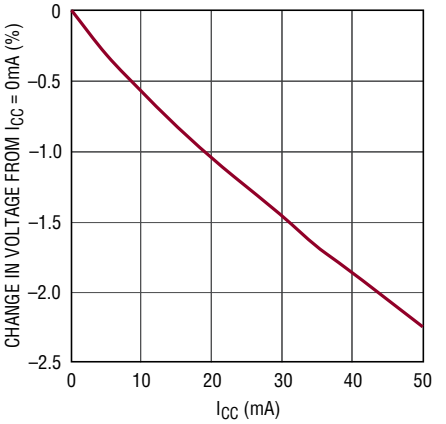
31152 G19

V_{CC} Voltage vs Temperature



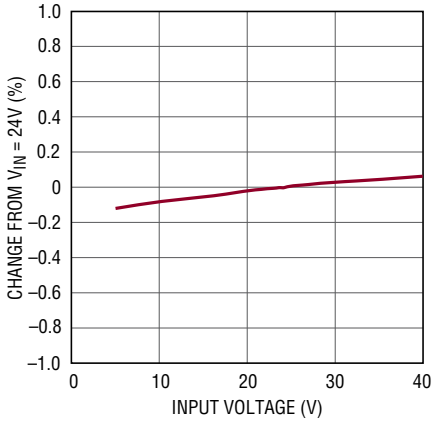
31152 G20

V_{CC} Regulator Load Regulation



31152 G21

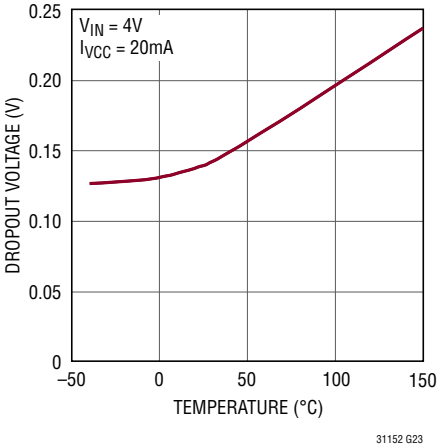
V_{CC} Regulator Line Regulation



31152 G22

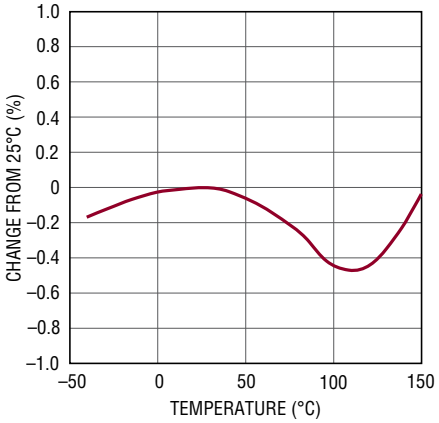
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

V_{CC} Regulator Dropout Voltage vs Temperature



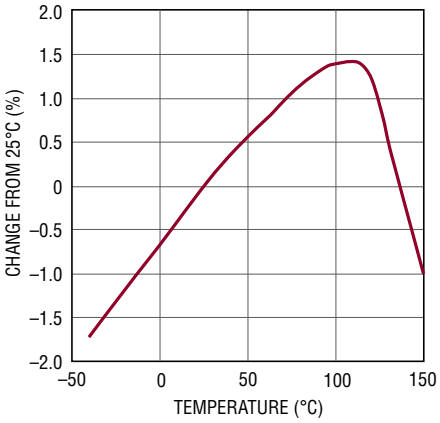
31152 G23

RUN Pin Threshold vs Temperature



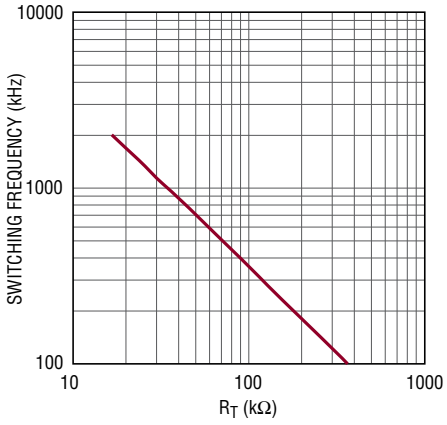
31152 G24

RUN Pin Hysteresis Current vs Temperature



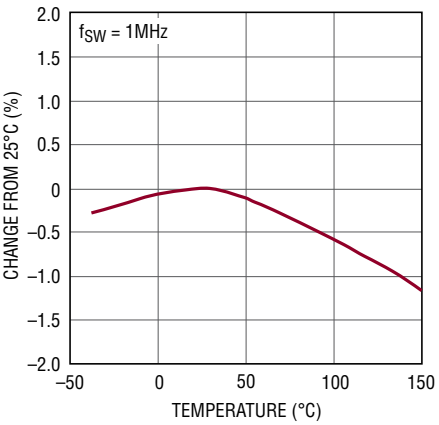
31152 G25

Oscillator Frequency vs R_T



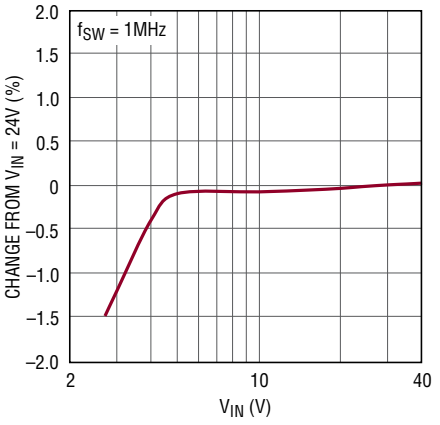
31152 G26

Oscillator Frequency vs Temperature



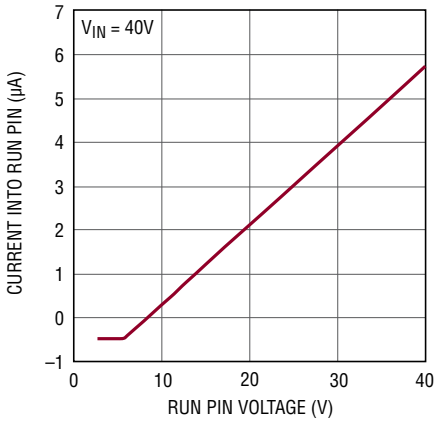
31152 G27

Oscillator Frequency vs V_{IN}



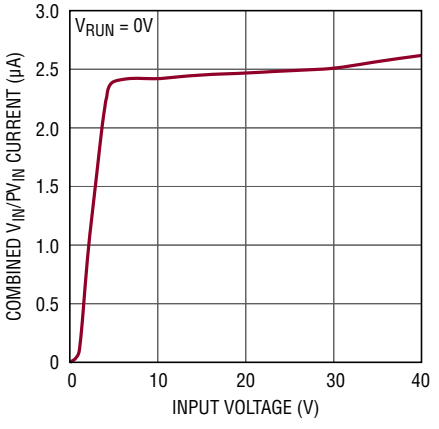
31152 G28

RUN Pin Current vs RUN Pin Voltage



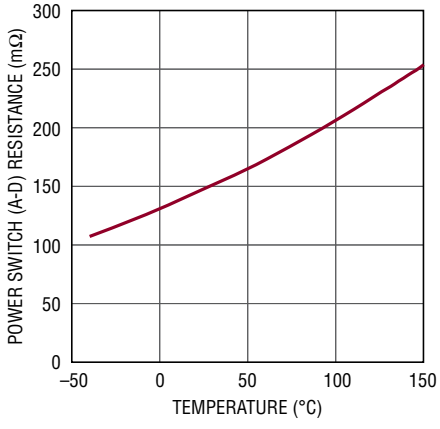
31152 G29

Shutdown Current on V_{IN}/PV_{IN} vs Input Voltage



31152 G30

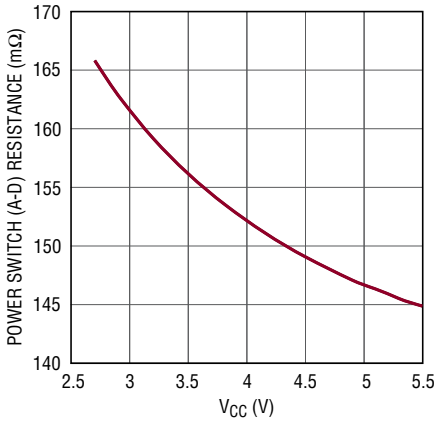
Power Switch Resistance vs Temperature



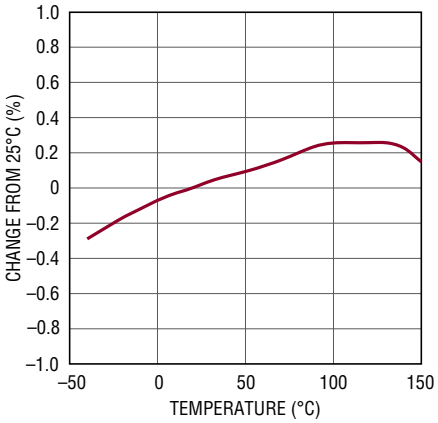
31152 G31

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

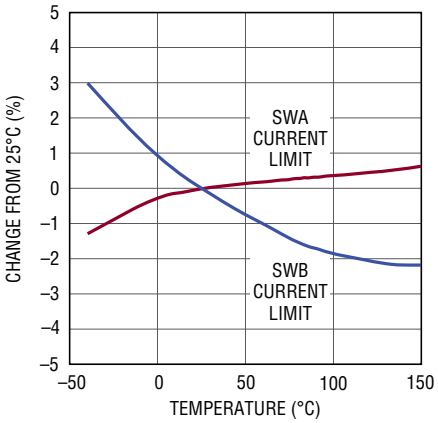
Power Switch Resistance vs V_{CC}



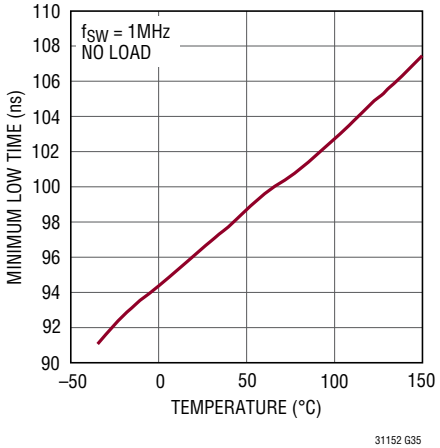
FB Voltage vs Temperature



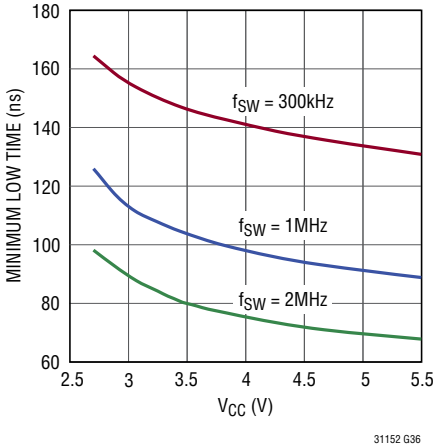
Inductor Current Limit Thresholds vs Temperature



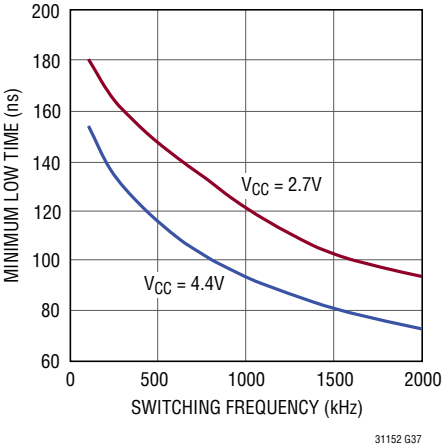
SW1, SW2 Minimum Low Time vs Temperature



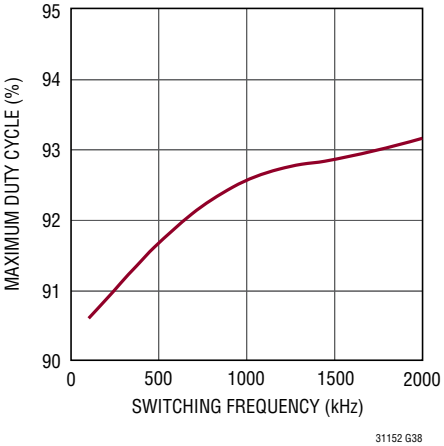
SW1, SW2 Minimum Low Time vs V_{CC}



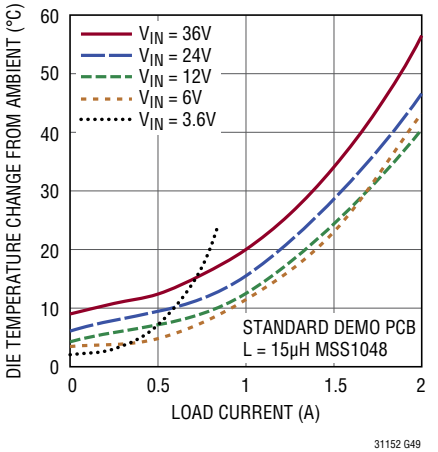
SW1, SW2 Minimum Low Time vs Switching Frequency



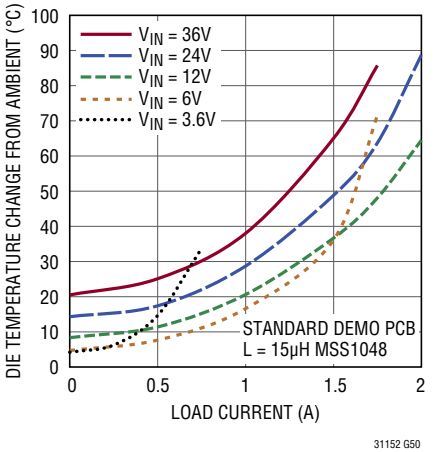
SW2 Maximum Duty Cycle vs Switching Frequency



Die Temperature Rise vs Load Current, V_{OUT} = 5V, f_{SW} = 750kHz

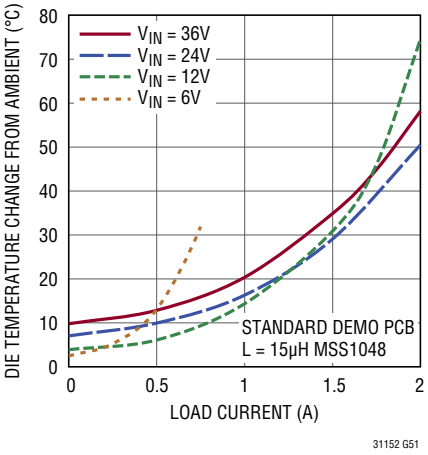


Die Temperature Rise vs Load Current, V_{OUT} = 5V, f_{SW} = 1.5MHz

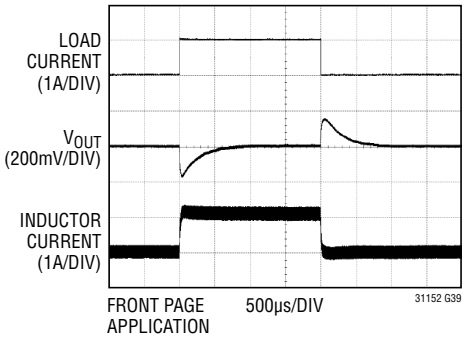


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

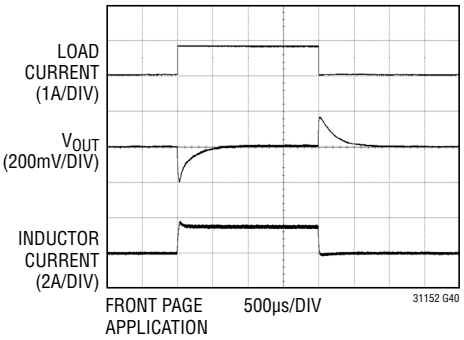
Die Temperature Rise vs Load Current, V_{OUT} = 12V, f_{SW} = 750kHz



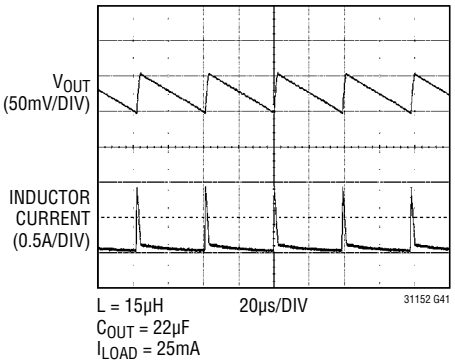
Load Transient (0A to 1A), V_{IN} = 24V, V_{OUT} = 5V



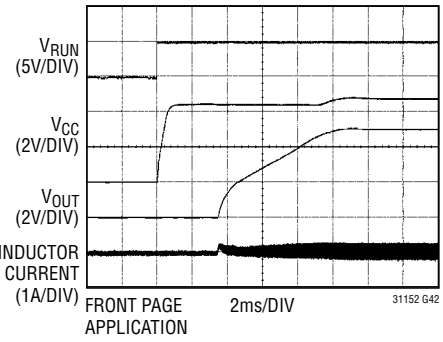
Load Transient (0A to 0.8A), V_{IN} = 3.6V, V_{OUT} = 5V



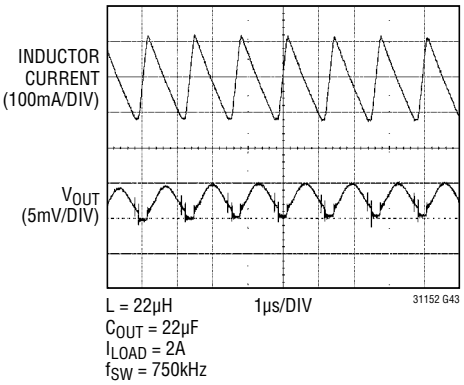
Output Voltage Ripple in Burst Mode Operation, V_{IN} = 24V, V_{OUT} = 5V



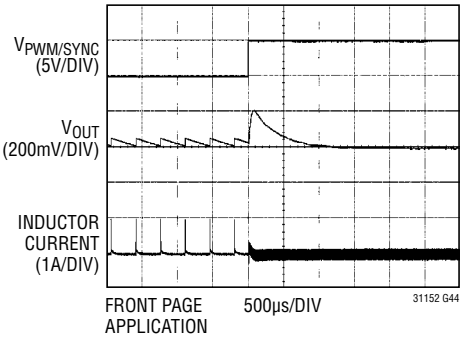
Soft-Start Waveforms



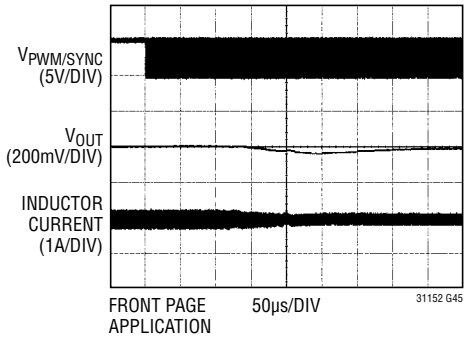
Output Voltage Ripple in PWM Mode, V_{IN} = 24V, V_{OUT} = 5V



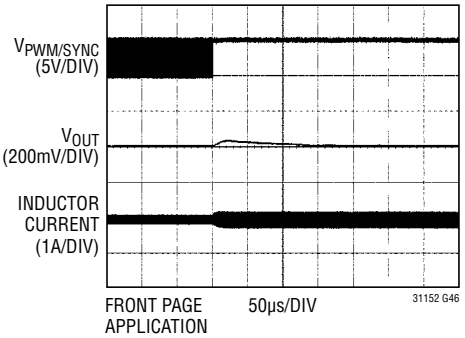
Burst Mode Operation to PWM Mode Output Voltage Transient



Phase-Locked Loop Acquisition, V_{IN} = 24V 1.2MHz Clock



Phase-Locked Loop Release, V_{IN} = 24V, 1.2MHz Clock



PIN FUNCTIONS (DHD/FE)

RUN (Pin 1/Pin 2): Input to Enable and Disable the IC and Set Custom Input UVLO Thresholds. The RUN pin can be driven by an external logic signal to enable and disable the IC. In addition, the voltage on this pin can be set by a resistor divider connected to the input voltage in order to provide an accurate undervoltage lockout threshold. The IC is enabled if RUN exceeds 1.21V nominally. Once enabled, a 0.5µA current is sourced by the RUN pin to provide hysteresis. To continuously enable the IC, this pin can be tied directly to the input voltage. The RUN pin cannot be forced more than 0.3V above V_{IN} under any condition.

SW2 (Pin 2/Pin 3): Buck-Boost Converter Power Switch Pin. This pin should be connected to one side of the buck-boost inductor.

PV_{OUT} (Pin 3/Pin 4): Buck-Boost Converter Power Output. This pin should be connected to a low ESR capacitor with a value of at least 10µF. The capacitor should be placed as close to the IC as possible and should have a short return path to ground. In applications with V_{OUT} > 20V that are subject to output overload or short-circuit conditions, it is recommended that a Schottky diode be installed from SW2 (anode) to PV_{OUT} (cathode). In applications subject to output short circuits through an inductive load, it is recommended that a Schottky diode be installed from ground (anode) to PV_{OUT} (cathode) to limit the extent that PV_{OUT} is driven below ground during the short-circuit transient.

GND (Pins 4, 5/Pins 5, 6): Signal Ground. These pins are the ground connections for the control circuitry of the IC and must be tied to ground in the application.

VC (Pin 6/Pin 7): Error Amplifier Output. A frequency compensation network must be connected between this pin and FB to stabilize the voltage control loop.

FB (Pin 7/Pin 8): Feedback Voltage Input. A resistor divider connected to this pin sets the output voltage for the buck-boost converter. The nominal FB voltage is 1000mV. Care should be taken in the routing of connections to this pin in order to minimize stray coupling to the switch pin traces.

RT (Pin 8/Pin 9): Oscillator Frequency Programming Pin. A resistor placed between this pin and ground sets the switching frequency of the buck-boost converter.

V_{CC} (Pin 9/Pin 12): Low Voltage Supply Input for IC Control Circuitry. This pin powers internal IC control circuitry and must be connected to the PV_{CC} pin in the application. A 4.7µF or larger bypass capacitor should be connected between this pin and ground. **The V_{CC} and PV_{CC} pins must be connected together in the application.**

V_{IN} (Pin 10/Pin 13): Power Supply Connection for Internal Circuitry and the V_{CC} Regulator. This pin provides power to the internal V_{CC} regulator and is the input voltage sense connection for the V_{IN} divider. A 0.1µF bypass capacitor should be connected between this pin and ground. The bypass capacitor should be located as close to the IC as possible and should have a short return path to ground.

PV_{CC} (Pin 11/Pin 14): Internal V_{CC} Regulator Output. This pin is the output pin of the internal linear regulator that generates the V_{CC} rail from V_{IN}. The PV_{CC} pin is also the supply connection for the power switch gate drivers. If the trace connecting PV_{CC} to V_{CC} cannot be made short in length, an additional bypass capacitor should be connected between this pin and ground. **The V_{CC} and PV_{CC} pins must be connected together in the application.**

BST2 (Pin 12/Pin 15): Flying Capacitor Pin for SW2. This pin must be connected to SW2 through a 0.1µF capacitor. This pin is used to generate the gate drive rail for power switch D.

BST1 (Pin 13/Pin 16): Flying Capacitor Pin for SW1. This pin must be connected to SW1 through a 0.1µF capacitor. This pin is used to generate the gate drive rail for power switch A.

PIN FUNCTIONS (DHD/FE)

PV_{IN} (Pin 14/Pin 17): Power Input for the Buck-Boost Converter. A 4.7µF or larger bypass capacitor should be connected between this pin and ground. The bypass capacitor should be located as close to the IC as possible and should via directly down to the ground plane. When powered through long leads or from a high ESR power source, a larger bulk input capacitor (typically 47µF to 100µF) may be required to stabilize the input voltage and prevent input filter interactions which could reduce phase margin and output current capability in boost mode operation.

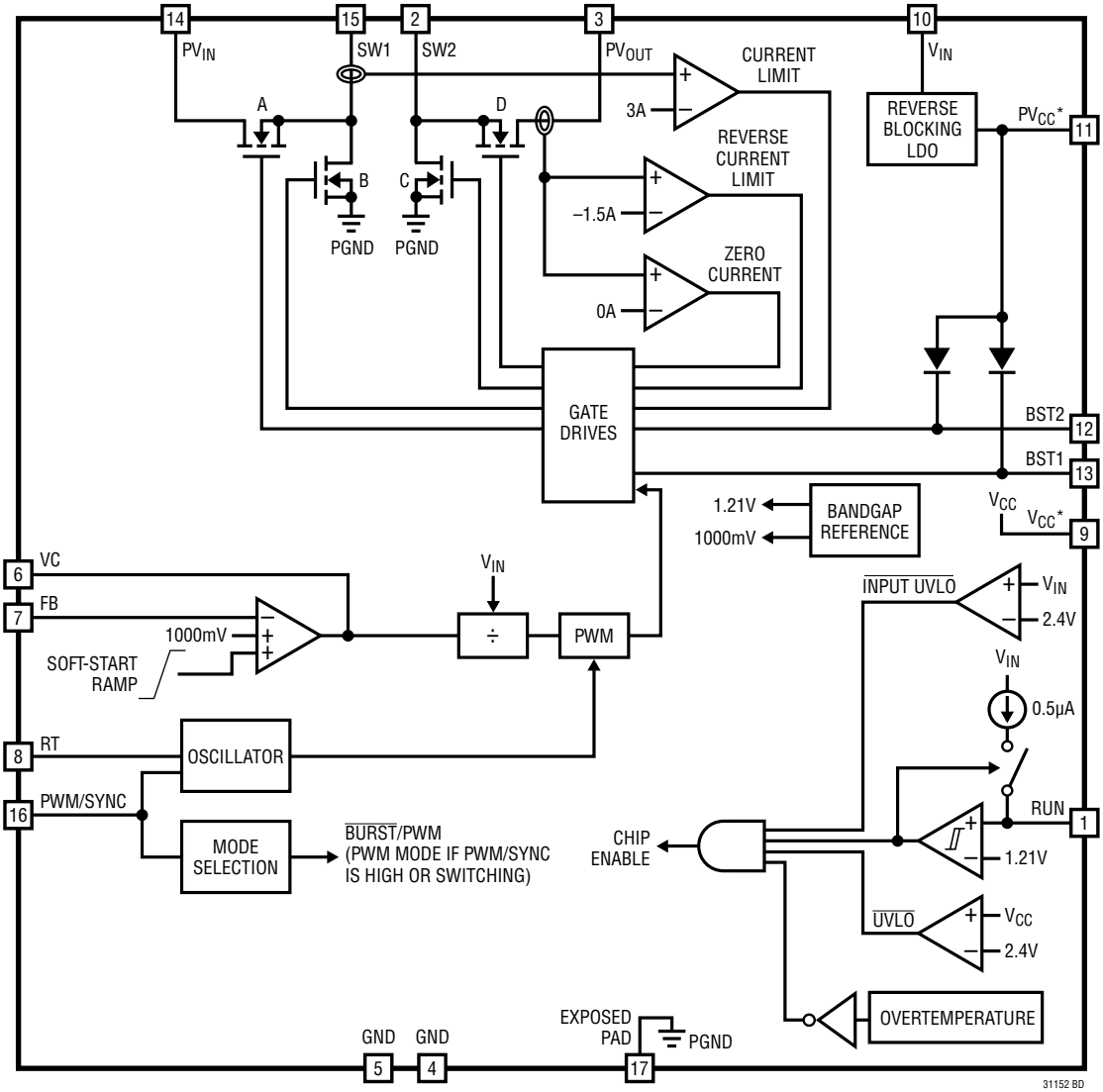
SW1 (Pin 15/Pin 18): Buck-Boost Converter Power Switch Pin. This pin should be connected to one side of the buck-boost inductor.

PWM/SYNC (Pin 16/Pin 19): Burst Mode/PWM Mode Control Pin and Synchronization Input. Forcing this pin high causes the IC to operate in fixed frequency PWM mode at all loads using the internal oscillator at the frequency set by the RT Pin. Forcing this pin low places the IC into Burst Mode operation regardless of load current. Burst Mode operation improves light load efficiency and reduces standby current. If an external clock signal is connected to this pin, the buck-boost converter will synchronize its switching with the external clock using fixed frequency PWM mode operation. The pulse width (negative or positive) of the applied clock should be at least 100ns. The maximum operating voltage for the PWM/SYNC pin is 5.5V. The PWM/SYNC pin can be connected to V_{CC} to force it high continuously.

PGND (Exposed Pad Pin 17/Pins 1, 10, 11, 20, Exposed Pad Pin 21): Power Ground Connections. These pins should be connected to the power ground in the application. The exposed pad is the power ground connection. It must be soldered to the PCB and electrically connected to ground through the shortest and lowest impedance connection possible and to the PCB ground plane for rated thermal performance.

BLOCK DIAGRAM

Pin numbers are shown for the DHD package only.



*PV_{CC} AND V_{CC} MUST BE CONNECTED TOGETHER IN THE APPLICATION

THE EXPOSED PAD IS AN ELECTRICAL CONNECTION AND MUST BE SOLDERED TO THE BOARD AND ELECTRICALLY CONNECTED TO GROUND

OPERATION

INTRODUCTION

The LTC3115-2 is a monolithic buck-boost converter that can operate with input and output voltages from as low as 2.7V to as high as 40V. Four internal low resistance N-channel DMOS switches minimize the size of the application circuit and reduce power losses to maximize efficiency. Internal high side gate drivers, which require only the addition of two small external capacitors, further simplify the design process. A proprietary switch control algorithm allows the buck-boost converter to maintain output voltage regulation with input voltages that are above, below or equal to the output voltage. Transitions between these operating modes are seamless and free of transients and subharmonic switching. The LTC3115-2 can be configured to operate over a wide range of switching frequencies, from 100kHz to 2MHz, allowing applications to be optimized for board area and efficiency. With its configurability and wide operating voltage range, the LTC3115-2 is ideally suited to a wide range of power systems especially those requiring compatibility with a variety of input power sources such as lead-acid batteries, USB ports, and industrial supply rails as well as from power sources which have wide or poorly controlled voltage ranges such as FireWire and unregulated wall adapters.

The LTC3115-2 has an internal fixed-frequency oscillator with a switching frequency that is easily set by a single external resistor. In noise sensitive applications, the converter can also be synchronized to an external clock via the PWM/SYNC pin. The LTC3115-2 has been optimized to reduce input current in shutdown and standby for applications which are sensitive to quiescent current draw, such as battery-powered devices. In Burst Mode operation, the no-load standby current is only 50µA (typical) and in shutdown the total supply current is reduced to 3µA (typical).

PWM MODE OPERATION

With the PWM/SYNC pin forced high or driven by an external clock, the LTC3115-2 operates in a fixed-frequency pulse width modulation (PWM) mode using a voltage mode control loop. This mode of operation maximizes the output current that can be delivered by the converter, reduces output voltage ripple, and yields a low noise fixed-frequency switching spectrum. A proprietary switching algorithm provides seamless transitions between operating modes and eliminates discontinuities in the average inductor current, inductor current ripple, and loop transfer function throughout all regions of operation. These advantages result in increased efficiency, improved loop stability, and lower output voltage ripple in comparison to the traditional 4-switch buck-boost converter.

Figure 1 shows the topology of the LTC3115-2 power stage which is comprised of four N-channel DMOS switches and their associated gate drivers. In PWM mode operation both switch pins transition on every cycle independent of the input and output voltage. In response to the error amplifier output, an internal pulse width modulator generates the appropriate switch duty cycles to maintain regulation of the output voltage.

When stepping down from a high input voltage to a lower output voltage, the converter operates in buck mode and switch D remains on for the entire switching cycle except for the minimum switch low duration (typically 100ns). During the switch low duration switch C is turned on which forces SW2 low and charges the flying capacitor, C_{BST2}, to ensure that the voltage of the switch D gate driver supply rail is maintained. The duty cycle of switches A and B are adjusted to provide the appropriate buck mode duty cycle.

If the input voltage is lower than the output voltage, the converter operates in boost mode. Switch A remains on for the entire switching cycle except for the minimum switch low duration (typically 100ns) while switches C and D are modulated to maintain the required boost mode duty cycle. The minimum switch low duration ensures that flying capacitor C_{BST1} is charged sufficiently to maintain the voltage on the BST1 rail.

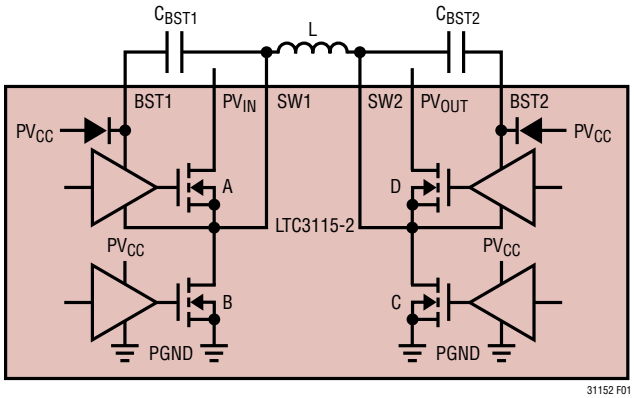


Figure 1. Power Stage Schematic

OPERATION

Oscillator and Phase-Locked Loop

The LTC3115-2 operates from an internal oscillator with a switching frequency that is configured by a single external resistor between the RT pin and ground. For noise sensitive applications, an internal phase-locked loop allows the LTC3115-2 to be synchronized to an external clock signal applied to the PWM/SYNC pin. The phase-locked loop is only able to increase the frequency of the internal oscillator to obtain synchronization. Therefore, the R_T resistor must be chosen to program the internal oscillator to a lower frequency than the frequency of the clock applied to the PWM/SYNC pin. Sufficient margin must be included to account for the frequency variation of the external synchronization clock as well as the worst-case variation in frequency of the internal oscillator. Whether operating from its internal oscillator or synchronized to an external clock signal, the LTC3115-2 is able to operate with a switching frequency from 100kHz to 2MHz, providing the ability to minimize the size of the external components and optimize the power conversion efficiency.

Error Amplifier and V_{IN} Divider

The LTC3115-2 has an internal high gain operational amplifier which provides frequency compensation of the control loop that maintains output voltage regulation. To ensure stability of this control loop, an external compensation network must be installed in the application circuit. A Type III compensation network as shown in Figure 2 is recommended for most applications since it provides the flexibility to optimize the converter's transient response while simultaneously minimizing any DC error in the output voltage.

As shown in Figure 2, the error amplifier is followed by an internal analog divider which adjusts the loop gain by the reciprocal of the input voltage in order to minimize loop-gain variation over changes in the input voltage. This simplifies design of the compensation network and optimizes the transient response over the entire range of input voltages. In addition, the analog divider provides a feed-forward correction for input voltage transients by immediately adjusting the voltage at the input to the PWM in response to a change in input voltage. This minimizes output voltage transients especially for line steps with rise

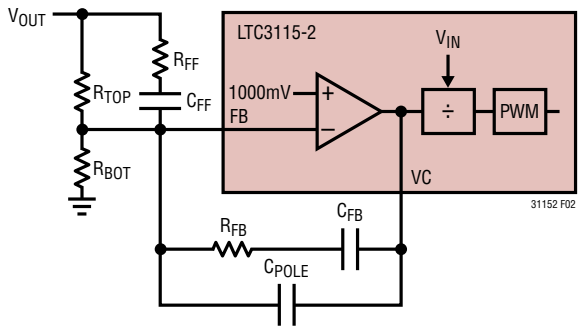


Figure 2. Error Amplifier and Compensation Network

and fall times that are much faster than the bandwidth of the control loop. However, when powered from an inductive or high ESR source the V_{IN} divider may respond to drops in the input voltage caused by changes in input current resulting in a loop interaction with the input impedance. This is most likely to occur in boost mode operation at high inductor currents. This interaction can degrade the phase margin of the control loop and even lead to oscillation. This situation can be avoided by reducing the impedance of the connection to PV_{IN} or by adding an electrolytic capacitor at PV_{IN} of sufficient value to damp the input filter and stabilize the voltage at the input of the part.

Details on designing the compensation network in LTC3115-2 applications can be found in the Applications Information section of this data sheet.

Inductor Current Limits

The LTC3115-2 has two current limit circuits that are designed to limit the peak inductor current to ensure that the switch currents remain within the capabilities of the IC during output short-circuit or overload conditions. The primary inductor current limit operates by injecting a current into the feedback pin which is proportional to the extent that the inductor current exceeds the current limit threshold (typically 3A). Due to the high gain of the feedback loop, this injected current forces the error amplifier output to decrease until the average current through the inductor is approximately reduced to the current limit threshold. This current limit circuit maintains the error amplifier in an active state to ensure a smooth recovery and minimal overshoot once the current limit fault condition is removed. However, the reaction speed

OPERATION

of this current limit circuit is limited by the dynamics of the error amplifier. On a hard output short, it is possible for the inductor current to increase substantially beyond the current limit threshold before the average current limit has time to react and reduce the inductor current. For this reason, there is a second current limit circuit which turns off power switch A if the current through switch A exceeds approximately 160% of the primary inductor current limit threshold. This provides additional protection in the case of an instantaneous hard output short and provides time for the primary current limit to react. In addition, if V_{OUT} falls below 1.85V, the inductor current limit is folded back to half its nominal value in order to minimize power dissipation.

Reverse Current Limit

In PWM mode operation, the LTC3115-2 synchronously switches all four power devices. As a result, in addition to being able to supply current to the output, the converter has the ability to actively conduct current away from the output if that is necessary to maintain regulation. If the output is held above regulation, this could result in large reverse currents. This situation can occur if the output of the LTC3115-2 is held up momentarily by another supply as may occur during a power-up or power-down sequence. To prevent damage to the part under such conditions, the LTC3115-2 has a reverse current comparator that monitors the current entering power switch D from the load. If this current exceeds 1.5A (typical) switch D is turned off for the remainder of the switching cycle in order to prevent the reverse inductor current from reaching unsafe levels.

Output Current Capability

The maximum output current that can be delivered by the LTC3115-2 is dependent upon many factors, the most significant being the input and output voltages. For V_{OUT} = 5V and $V_{IN} \geq$ 3.6V, the LTC3115-2 is able to support up to a 0.8A load continuously. For V_{OUT} = 12V and $V_{IN} \geq$ 12V, the LTC3115-2 is able to support up to a 2A load continuously. Typically, the output current capability is greatest when the input voltage is approximately equal to the output voltage. At larger step-up voltage ratios, the output current capability is reduced because the lower duty cycle of switch D results in a larger inductor current being needed to support a given load. Additionally, the output current capability generally decreases at large step-down voltage ratios due to higher inductor current ripple which reduces the maximum attainable inductor current.

The output current capability can also be affected by inductor characteristics. An inductor with large DC resistance will degrade output current capability, particularly in boost mode operation. Larger value inductors generally maximize output current capability by reducing inductor current ripple. In addition, higher switching frequencies (especially above 750kHz) will reduce the maximum output current that can be supplied (see the Typical Performance Characteristics for details).

Burst Mode OPERATION

When the PWM/SYNC pin is held low, the buck-boost converter employs Burst Mode operation using a variable frequency switching algorithm that minimizes the no-load input quiescent current and improves efficiency at light load by reducing the amount of switching to the minimum level required to support the load. The output current capability in Burst Mode operation is substantially lower than in PWM mode and is intended to support light standby loads (typically under 50mA). Curves showing the maximum Burst Mode load current as a function of the input and output voltage can be found in the Typical Characteristics section of this data sheet. If the converter load in Burst Mode operation exceeds the maximum Burst Mode current capability, the output will lose regulation.

Each Burst Mode cycle is initiated when switches A and C turn on producing a linearly increasing current through the inductor. When the inductor current reaches the Burst Mode current limit (1A typically) switches B and D are turned on, discharging the energy stored in the inductor into the output capacitor and load. Once the inductor current reaches zero, all switches are turned off and the cycle is complete. Current pulses generated in this manner are repeated as often as necessary to maintain regulation of the output voltage. In Burst Mode operation, the error amplifier is not used but is instead placed in a low current standby mode to reduce supply current and improve light load efficiency.

OPERATION

SOFT-START

To minimize input current transients on power-up, the LTC3115-2 incorporates an internal soft-start circuit with a nominal duration of 9ms. The soft-start is implemented by a linearly increasing ramp of the error amplifier reference voltage during the soft-start duration. As a result, the duration of the soft-start period is largely unaffected by the size of the output capacitor or the output regulation voltage. Given the closed-loop nature of the soft-start implementation, the converter is able to respond to load transients that occur during the soft-start interval. The soft-start period is reset by thermal shutdown and UVLO events on both V_{IN} and V_{CC}.

V_{CC} REGULATOR

An internal low dropout regulator generates the 4.45V (nominal) V_{CC} rail from V_{IN}. The V_{CC} rail powers the internal control circuitry and power device gate drivers of the LTC3115-2. The V_{CC} regulator is disabled in shutdown to reduce quiescent current and is enabled by forcing the RUN pin above its logic threshold. The V_{CC} regulator includes current limit protection to safeguard against short circuiting of the V_{CC} rail. For applications where the output voltage is set to 5V, the V_{CC} rail can be driven from the output rail through a Schottky diode. Bootstrapping in this manner can provide a significant efficiency improvement, particularly at large voltage step down ratios, and may also allow operation down to a lower input voltage. The maximum operating voltage for the V_{CC} pin is 5.5V. When forcing V_{CC} externally, care must be taken to ensure that this limit is not exceeded.

UNDERVOLTAGE LOCKOUT

To eliminate erratic behavior when the input voltage is too low to ensure proper operation, the LTC3115-2 incorporates internal undervoltage lockout (UVLO) circuitry. There are two UVLO comparators, one that monitors V_{IN} and another that monitors V_{CC}. The buck-boost converter is disabled if either V_{IN} or V_{CC} falls below its respective UVLO threshold. The input voltage UVLO comparator has a falling threshold of 2.4V (typical). If the input voltage falls below this level all switching is disabled until the input voltage rises above 2.6V (nominal). The V_{CC} UVLO has a falling threshold of 2.4V. If V_{CC} falls below this threshold the buck-boost converter is prevented from switching until V_{CC} rises above 2.6V.

Depending on the particular application circuit it is possible that either of these UVLO thresholds could be the factor limiting the minimum input operating voltage of the LTC3115-2. The dominant factor depends on the voltage drop between V_{IN} and V_{CC} which is determined by the dropout voltage of the V_{CC} regulator and is proportional to the total load current drawn from V_{CC}. The load current on the V_{CC} regulator is principally generated by the gate driver supply currents which are proportional to operating frequency and generally increase with larger input and output voltages. As a result, at higher switching frequencies and higher input and output voltages the V_{CC} regulator dropout voltage will increase, making it more likely that the V_{CC} UVLO threshold could become the limiting factor. Curves provided in the Typical Performance Characteristics section of this data sheet show the typical V_{CC} current and can be used to estimate the V_{CC} regulator dropout voltage in a particular application. In applications where V_{CC} is bootstrapped (powered by V_{OUT} or by an auxiliary supply rail through a Schottky diode) the minimum input operating voltage will be limited only by the input voltage UVLO threshold.

RUN PIN COMPARATOR

In addition to serving as a logic-level input to enable the IC, the RUN pin features an accurate internal comparator allowing it to be used to set custom rising and falling input undervoltage lockout thresholds with the addition of an external resistor divider. When the RUN pin is driven above its logic threshold (typically 0.8V) the V_{CC} regulator is enabled which provides power to the internal control circuitry of the IC and the accurate RUN pin comparator is enabled. If the RUN pin voltage is increased further so that it exceeds the RUN comparator threshold (1.21V nominal), the buck-boost converter will be enabled.

If the RUN pin is brought below the RUN comparator threshold, the buck-boost converter will inhibit switching, but the V_{CC} regulator and control circuitry will remain powered unless the RUN pin is brought below its logic

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threshold. Therefore, in order to place the part in shutdown and reduce the input current to its minimum level (3µA typical) it is necessary to ensure that the RUN pin is brought below the worst-case logic threshold (0.3V). The RUN pin is a high voltage input and can be connected directly to V_{IN} to continuously enable the part when the input supply is present. If the RUN pin is forced above approximately 5V it will sink a small current as given by the following equation:

$$I_{RUN} \cong \frac{V_{RUN} - 5V}{5M\Omega}$$

With the addition of an external resistor divider as shown in Figure 3, the RUN pin can be used to establish a custom input undervoltage lockout threshold. The buck-boost converter is enabled when the RUN pin reaches 1.21V which allows the rising UVLO threshold to be set via the resistor divider ratio. Once the RUN pin reaches the threshold voltage, the comparator switches and the buck-boost converter is enabled. In addition, an internal 0.5µA (typical) current source is enabled which sources current out of the RUN pin raising the RUN pin voltage away from the threshold. In order to disable the part, V_{IN} must be reduced sufficiently to overcome the hysteresis generated by this current as well as the 100mV hysteresis of the RUN comparator. As a result, the amount of hysteresis can be independently programmed without affecting the rising UVLO threshold by scaling the values of both resistors.

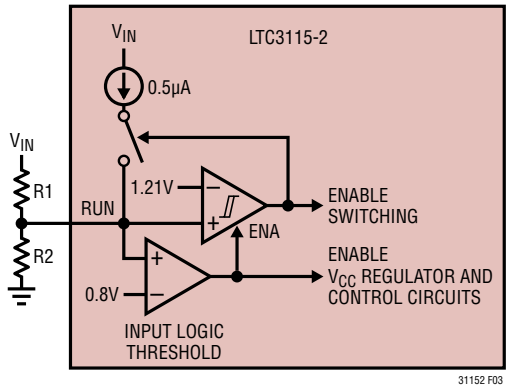

Figure 3. Accurate RUN Pin Comparator

THERMAL CONSIDERATIONS

The power switches in the LTC3115-2 are designed to operate continuously with currents up to the internal current limit thresholds. However, when operating at high current levels there may be significant heat generated within the IC. In addition, in many applications the V_{CC} regulator is operated with large input-to-output voltage differentials resulting in significant levels of power dissipation in its pass element which can add significantly to the total power dissipated within the IC. As a result, careful consideration must be given to the thermal environment of the IC in order to optimize efficiency and ensure that the LTC3115-2 is able to provide its full-rated output current. Specifically, the exposed die attach pad of both the DHD and FE packages should be soldered to the PC board and the PC board should be designed to maximize the conduction of heat out of the IC package. This can be accomplished by utilizing multiple vias from the die attach pad connection to other PCB layers containing a large area of exposed copper.

If the die temperature exceeds approximately 165°C, the IC will enter overtemperature shutdown and all switching will be inhibited. The part will remain disabled until the die cools by approximately 10°C. The soft-start circuit is re-initialized in overtemperature shutdown to provide a smooth recovery when the fault condition is removed.

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The standard LTC3115-2 application circuit is shown as the typical application on the front page of this data sheet. The appropriate selection of external components is dependent upon the required performance of the IC in each particular application given considerations and trade-offs such as PCB area, cost, output and input voltage, allowable ripple voltage, efficiency and thermal considerations. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the application circuit.

V_{CC} Capacitor Selection

The V_{CC} output on the LTC3115-2 is generated from the input voltage by an internal low dropout regulator. The V_{CC} regulator has been designed for stable operation with a wide range of output capacitors. For most applications, a low ESR ceramic capacitor of at least 4.7µF should be utilized. The capacitor should be placed as close to the pin as possible and should connect to the PV_{CC} pin and ground through the shortest traces possible. The PV_{CC} pin is the regulator output and is also the internal supply pin for the gate drivers and boost rail charging diodes. The V_{CC} pin is the supply connection for the remainder of the control circuitry. The PV_{CC} and V_{CC} pins must be connected together on the application PCB. If the trace connecting V_{CC} to PV_{CC} cannot be made via a short connection, an additional 0.1µF bypass capacitor should be placed between the V_{CC} pin and ground using the shortest connections possible.

Inductor Selection

The choice of inductor used in LTC3115-2 application circuits influences the maximum deliverable output current, the magnitude of the inductor current ripple, and the power conversion efficiency. The inductor must have low DC series resistance or output current capability and efficiency will be compromised. Larger inductance values reduce inductor current ripple and will therefore generally yield greater output current capability. For a fixed DC resistance, a larger value of inductance will yield higher efficiency by reducing the peak current to be closer to the average output current and therefore minimize resistive losses due to high RMS currents. However, a larger inductor value within any given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage. In general, inductors with larger inductance values and lower DC resistance will increase the deliverable output current and improve the efficiency of LTC3115-2 applications.

An inductor used in LTC3115-2 applications should have a saturation current rating that is greater than the worst-case average inductor current plus half the ripple current. The peak-to-peak inductor current ripple for each operational mode can be calculated from the following formula, where f is the switching frequency, L is the inductance, and t_{LOW} is the switch pin minimum low time. The switch pin minimum low time can be determined from curves given in the Typical Performance Characteristics section of this data sheet.

$$\Delta I_{L(P-P)(BUCK)} = \frac{V_{OUT}}{L}\left(\frac{V_{IN}-V_{OUT}}{V_{IN}}\right)\left(\frac{1}{f}-t_{LOW}\right)$$

$$\Delta I_{L(P-P)(BOOST)} = \frac{V_{IN}}{L}\left(\frac{V_{OUT}-V_{IN}}{V_{OUT}}\right)\left(\frac{1}{f}-t_{LOW}\right)$$

In addition to its influence on power conversion efficiency, the inductor DC resistance can also impact the maximum output current capability of the buck-boost converter particularly at low input voltages. In buck mode, the output current of the buck-boost converter is generally limited only by the inductor current reaching the current limit threshold. However, in boost mode, especially at large step-up ratios, the output current capability can also be limited by the total resistive losses in the power stage. These include switch resistances, inductor resistance, and PCB trace resistance. Use of an inductor with high DC resistance can degrade the output current capability from that shown in the Typical Performance Characteristics section of this data sheet. As a guideline, in most applications the inductor DC resistance should be significantly smaller than the typical power switch resistance of 150mΩ.

Different inductor core materials and styles have an impact on the size and price of an inductor at any given current rating. Shielded construction is generally preferred as it minimizes the chances of interference with other circuitry. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 1

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provides a small sampling of inductors that are well suited to many LTC3115-2 applications.

In applications with $V_{OUT} \geq 20V$, it is recommended that a minimum inductance value, L_{MIN}, be utilized where f is the switching frequency:

$$L_{MIN} = \frac{12H}{(f/Hz)}$$

Table 1. Representative Surface Mount Inductors

PART NUMBER	VALUE (µH)	DCR (mΩ)	MAX DC CURRENT (A)	SIZE (mm) W × L × H
Coilcraft				
LPS6225	4.7	65	3.2	6.2 × 6.2 × 2.5
LPS6235	6.8	75	2.8	6.2 × 6.2 × 3.5
MSS1038	22	70	3.3	10.2 × 10.5 × 3.8
D03316P	15	50	3.0	12.9 × 9.4 × 5.2
Cooper-Bussmann				
CD1-150-R	15	50	3.6	10.5 × 10.4 × 4.0
DR1030-100-R	10	40	3.18	10.3 × 10.5 × 3.0
FP3-8R2-R	8.2	74	3.4	7.3 × 6.7 × 3.0
DR1040-220-R	22	54	2.9	10.3 × 10.5 × 4.0
Panasonic				
ELLCTV180M	18	30	3.0	12 × 12 × 4.2
ELLATV100M	10	23	3.3	10 × 10 × 4.2
Sumida				
CDRH8D28/HP	10	78	3.0	8.3 × 8.3 × 3
CDR10D48MNNP	39	105	3.0	10.3 × 10.3 × 5
CDRH8D28NP	4.7	24.7	3.4	8.3 × 8.3 × 3
Taiyo-Yuden				
NR10050T150M	15	46	3.6	9.8 × 9.8 × 5
TOKO				
B1047AS-6R8N	6.8	36	2.9	7.6 × 7.6 × 5
B1179BS-150M	15	56	3.3	10.3 × 10.3 × 4
892NAS-180M	18	42	3.0	12.3 × 12.3 × 4.5
Würth				
7447789004	4.7	33	2.9	7.3 × 7.3 × 3.2
744771133	33	49	2.7	12 × 12 × 6
744066150	15	40	3.2	10 × 10 × 3.8

Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck-boost converter output in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent option as they have low ESR and are available in small footprints. The capacitor value should be chosen large enough to reduce the output voltage ripple to acceptable levels. Neglecting the capacitor ESR and ESL, the peak-to-peak output voltage ripple can be calculated by the following formulas, where f is the switching frequency, C_{OUT} is the capacitance, t_{LOW} is the switch pin minimum low time, and I_{LOAD} is the output current. Curves for the value of t_{LOW} as a function of switching frequency and temperature can be found in Typical Performance Characteristics section of this data sheet.

$$\Delta V_{P-P(BUCK)} = \frac{I_{LOAD} t_{LOW}}{C_{OUT}}$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD}}{f C_{OUT}} \left(\frac{V_{OUT} - V_{IN} + t_{LOW} f V_{IN}}{V_{OUT}} \right)$$

The output voltage ripple increases with load current and is generally higher in boost mode than in buck mode. These expressions only take into account the output voltage ripple that results from the output current being discontinuous. They provide a good approximation to the ripple at any significant load current but underestimate the output voltage ripple at very light loads where output voltage ripple is dominated by the inductor current ripple.

In addition to output voltage ripple generated across the output capacitance, there is also output voltage ripple produced across the internal resistance of the output capacitor. The ESR-generated output voltage ripple is proportional to the series resistance of the output capacitor and is given by the following expressions where R_{ESR} is the series resistance of the output capacitor and all other terms are as previously defined.

$$\Delta V_{P-P(BUCK)} = \frac{I_{LOAD} R_{ESR}}{1 - t_{LOW} f} \cong I_{LOAD} R_{ESR}$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD} R_{ESR} V_{OUT}}{V_{IN}(1 - t_{LOW} f)} \cong I_{LOAD} R_{ESR} \left(\frac{V_{OUT}}{V_{IN}} \right)$$

Input Capacitor Selection

The PV_{IN} pin carries the full inductor current and provides power to internal control circuits in the IC. To minimize input voltage ripple and ensure proper operation of the IC, a low ESR bypass capacitor with a value of at least 4.7µF should be located as close to this pin as possible. The traces connecting this capacitor to PV_{IN} and the ground plane should be made as short as possible. The V_{IN} pin provides power to the V_{CC} regulator and other internal circuitry. If the PCB trace connecting V_{IN} to PV_{IN} is long, it

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may be necessary to add an additional small value bypass capacitor near the V_{IN} pin.

When powered through long leads or from a high ESR power source, a larger value bulk input capacitor may be required. In such applications, a 47µF to 100µF electrolytic capacitor in parallel with a 1µF ceramic capacitor generally yields a high performance, low cost solution.

Recommended Input and Output Capacitors

The capacitors used to filter the input and output of the LTC3115-2 must have low ESR and must be rated to handle the large AC currents generated by switching converters. This is important to maintain proper functioning of the IC and to reduce output voltage ripple. There are many capacitor types that are well suited to such applications including multilayer ceramic, low ESR tantalum, OS-CON and POSCAP technologies. In addition, there are certain types of electrolytic capacitors such as solid aluminum organic polymer capacitors that are designed for low ESR and high AC currents and these are also well suited to LTC3115-2 applications (Table 2). The choice of capacitor technology is primarily dictated by a trade-off between cost, size and leakage current. Notice that some capacitors such as the OS-CON and POSCAP technologies can exhibit significant DC leakage currents which may limit their applicability in devices which require low no-load quiescent current in Burst Mode operation.

Ceramic capacitors are often utilized in switching converter applications due to their small size, low ESR, and low leakage currents. However, many ceramic capacitors designed for power applications experience significant loss in capacitance from their rated value with increased DC bias voltages. For example, it is not uncommon for a small surface mount ceramic capacitor to lose more than 50% of its rated capacitance when operated near its rated voltage. As a result, it is sometimes necessary to use a larger value capacitance or a capacitor with a higher voltage rating than required in order to actually realize the intended capacitance at the full operating voltage. To ensure that the intended capacitance is realized in the application circuit, be sure to consult the capacitor vendor's curve of capacitance versus DC bias voltage.

Table 2. Representative Bypass and Output Capacitors

MANUFACTURER, PART NUMBER	VALUE (µF)	VOLTAGE (V)	SIZE L × W × H (mm), TYPE, ESR
AVX			
12103D226MAT2A	22	25	3.2 × 2.5 × 2.79 X5R Ceramic
TPME226K050R0075	22	50	7.3 × 4.3 × 4.1 Tantalum, 75mΩ
Kemet			
C2220X226K3RACTU	22	25	5.7 × 5.0 × 2.4 X7R Ceramic
A700D226M016ATE030	22	16	7.3 × 4.3 × 2.8 Alum. Polymer, 30mΩ
Murata			
GRM32ER71E226KE15L	22	25	3.2 × 2.5 × 2.5 X7R Ceramic
Nichicon			
PLV1E121MDL1	82	25	8 × 8 × 12 Alum. Polymer, 25mΩ
Panasonic			
ECJ-4YB1E226M	22	25	3.2 × 2.5 × 2.5 X5R Ceramic
Sanyo			
25TQC22MV	22	25	7.3 × 4.3 × 3.1 POSCAP, 50mΩ
16TQC100M	100	16	7.3 × 4.3 × 1.9 POSCAP, 45mΩ
25SVPF47M	47	25	6.6 × 6.6 × 5.9 OS-CON, 30mΩ
Taiyo Yuden			
UMK325BJ106MM-T	10	50	3.2 × 2.5 × 2.5 X5R Ceramic
TMK325BJ226MM-T	22	25	3.2 × 2.5 × 2.5 X5R Ceramic
TDK			
KTJ500B226M55BFT00	22	50	6.0 × 5.3 × 5.5 X7R Ceramic
C5750X7R1H106M	10	50	5.7 × 5.0 × 2.0 X7R Ceramic
CKG57NX5R1E476M	47	25	6.5 × 5.5 × 5.5 X5R Ceramic
Vishay			
94SVPD476X0035F12	47	35	10.3 × 10.3 × 12.6 OS-CON, 30mΩ

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Programming Custom Input UVLO Thresholds

With the addition of an external resistor divider connected to the input voltage as shown in Figure 4, the RUN pin can be used to program the input voltage at which the LTC3115-2 is enabled and disabled.

For a rising input voltage, the LTC3115-2 is enabled when V_{IN} reaches the threshold given by the following equation, where R1 and R2 are the values of the resistor divider resistors:

$$V_{TH(RISING)} = 1.21V\left(\frac{R1+R2}{R2}\right)$$

To ensure robust operation in the presence of noise, the RUN pin has two forms of hysteresis. A fixed 100mV of hysteresis within the RUN pin comparator provides a minimum RUN pin hysteresis equal to 8.3% of the input turn-on voltage independent of the resistor divider values. In addition, an internal hysteresis current that is sourced from the RUN pin during operation generates an additive level of hysteresis which can be programmed by the value of R1 to increase the overall hysteresis to suit the requirements of specific applications.

Once the IC is enabled, it will remain enabled until the input voltage drops below the comparator threshold by the hysteresis voltage, V_{HYST}, as given by the following equation where R1 and R2 are values of the divider resistors:

$$V_{HYST} = R1 \bullet 0.5\mu A + \left(\frac{R1+R2}{R2}\right)0.1V$$

Therefore, the rising UVLO threshold and amount of hysteresis can be independently programmed via appropriate selection of resistors R1 and R2. For high levels of hysteresis, the value of R1 can become larger than is desirable in a practical implementation (greater than 1MΩ to 2MΩ). In such cases, the amount of hysteresis can be increased further through the addition of an additional resistor, R_H, as shown in Figure 5.

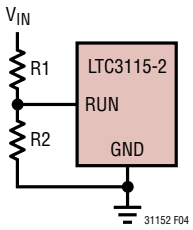

Figure 4. Setting the Input UVLO Threshold and Hysteresis

When using the additional R_H resistor, the rising RUN pin threshold remains as given by the original equation and the hysteresis is given by the following expression:

$$V_{HYST} = \left(\frac{R1+R2}{R2}\right)0.1V + \frac{R_H R2 + R_H R1 + R1R2}{R2}(0.5\mu A)$$

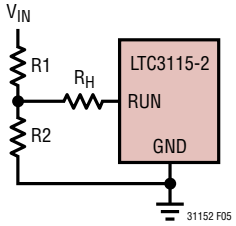

Figure 5. Increasing Input UVLO hysteresis

To improve the noise robustness and accuracy of the UVLO thresholds, the RUN pin input can be filtered by adding a 1000pF capacitor from RUN to GND. Larger valued capacitors should not be utilized because they could interfere with operation of the hysteresis.

Bootstrapping the V_{CC} Regulator

The high and low side gate drivers are powered through the PV_{CC} rail which is generated from the input voltage through an internal linear regulator. In some applications, especially at higher operating frequencies and high input and output voltages, the power dissipation in the linear V_{CC} regulator can become a key factor in the conversion efficiency of the converter and can even become a significant source of thermal heating. For example, at a 1.2MHz switching frequency, an input voltage of 36V, and an output voltage of 24V, the total PV_{CC}/V_{CC} current is approximately 18mA as shown in the Typical Performance Characteristics section of this data sheet. As a result, this will generate 568mW of power dissipation in the V_{CC} regulator which will result in an increase in die temperature of approximately 24° above ambient in the DFN package. This significant power loss will have a substantial impact on the conversion efficiency and the additional heating may limit the maximum ambient operating temperature for the application.

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A significant performance advantage can be attained in applications which have the converter output voltage programmed to 5V if the output voltage is utilized to power the PV_{CC} and V_{CC} rails. This can be done by connecting a Schottky diode from V_{OUT} to PV_{CC}/V_{CC} as shown in Figure 6. With this bootstrap diode installed, the gate driver currents are generated directly by the buck-boost converter at high efficiency rather than through the internal linear regulator. To minimize current drawn from the output, the internal V_{CC} regulator contains reverse blocking circuitry which minimizes the current into the PV_{CC}/V_{CC} pins when they are driven above the input voltage.

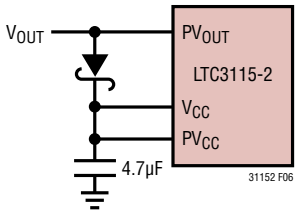

Figure 6. Bootstrapping PV_{CC} and V_{CC}

Buck Mode Small-Signal Model

The LTC3115-2 uses a voltage mode control loop to maintain regulation of the output voltage. An externally compensated error amplifier drives the VC pin to generate the appropriate duty cycle of the power switches. Use of an external compensation network provides the flexibility for optimization of closed loop performance over the wide variety of output voltages, switching frequencies, and external component values supported by the LTC3115-2.

The small-signal transfer function of the buck-boost converter is different in the buck and boost modes of operation and care must be taken to ensure stability in both operating regions. When stepping down from a higher input voltage to a lower output voltage, the converter will operate in buck mode and the small-signal transfer function from the error amplifier output, V_C, to the converter output voltage is given by the following equation:

$$\left.\frac{V_O}{V_C}\right|_{BUCK\ MODE} = G_{BUCK}\frac{\left(1+\frac{s}{2\pi f_Z}\right)}{1+\frac{s}{2\pi f_0 Q}+\left(\frac{s}{2\pi f_0}\right)^2}$$

The gain term, G_{BUCK}, is comprised of three different components: the gain of the analog divider, the gain of the pulse width modulator, and the gain of the power stage as given by the following expressions where V_{IN} is the input voltage to the converter, f is the switching frequency, R is the load resistance, and t_{LOW} is the switch pin minimum low time. Curves showing the switch pin minimum low time can be found in the Typical Performance Characteristics section of this data sheet. The parameter R_S represents the average series resistance of the power stage and can be approximated as twice the average power switch resistance plus the DC resistance of the inductor.

$$G_{BUCK} = G_{DIVIDER}\,G_{PWM}\,G_{POWER}$$

$$G_{DIVIDER} = \frac{19.8V}{V_{IN}}$$

$$G_{PWM} = \frac{3}{2V}\left(1-t_{LOW}f\right)$$

$$G_{POWER} = \frac{V_{IN}R}{\left(1-t_{LOW}f\right)\left(R+R_S\right)}$$

Notice that the gain of the analog divider cancels the input voltage dependence of the power stage. As a result, the buck mode gain is well approximated by a constant as given by the following equation:

$$G_{BUCK} = 29.7\frac{R}{R+R_S} \cong 29.7 = 29.5dB$$

The buck mode transfer function has a single zero which is generated by the ESR of the output capacitor. The zero frequency, f_Z, is given by the following expression where R_C and C_O are the ESR and value of the output filter capacitor respectively.

$$f_Z = \frac{1}{2\pi R_C C_O}$$

In most applications, an output capacitor with a very low ESR is utilized in order to reduce the output voltage ripple to acceptable levels. Such low values of capacitor ESR result in a very high frequency zero and as a result the zero is commonly too high in frequency to significantly impact compensation of the feedback loop.

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The denominator of the buck mode transfer function exhibits a pair of resonant poles generated by the LC filtering of the power stage. The resonant frequency of the power stage, f_O, is given by the following expression where L is the value of the inductor:

$$f_O = \frac{1}{2\pi}\sqrt{\frac{R+R_S}{LC_O(R+R_C)}} \cong \frac{1}{2\pi}\sqrt{\frac{1}{LC_O}}$$

The quality factor, Q, has a significant impact on compensation of the voltage loop since a higher Q factor produces a sharper loss of phase near the resonant frequency. The quality factor is inversely related to the amount of damping in the power stage and is substantially influenced by the average series resistance of the power stage, R_S. Lower values of R_S will increase the Q and result in a sharper loss of phase near the resonant frequency and will require more phase boost or lower bandwidth to maintain an adequate phase margin.

$$Q = \frac{\sqrt{LC_O(R+R_C)(R+R_S)}}{RR_CC_O + L + C_OR_S(R+R_C)} \cong \frac{\sqrt{LC_O}}{\frac{L}{R} + C_OR_S}$$

Boost Mode Small-Signal Model

When stepping up from a lower input voltage to a higher output voltage, the buck-boost converter will operate in boost mode where the small-signal transfer function from control voltage, V_C, to the output voltage is given by the following expression.

$$\left.\frac{V_O}{V_C}\right|_{BOOST\ MODE} = G_{BOOST}\frac{\left(1+\frac{s}{2\pi f_Z}\right)\left(1-\frac{s}{2\pi f_{RHPZ}}\right)}{1+\frac{s}{2\pi f_O Q}+\left(\frac{s}{2\pi f_O}\right)^2}$$

In boost mode operation, the transfer function is characterized by a pair of resonant poles and a zero generated by the ESR of the output capacitor as in buck mode. However, in addition there is a right half plane zero which generates increasing gain and decreasing phase at higher frequencies. As a result, the crossover frequency in boost mode operation generally must be set lower than in buck mode in order to maintain sufficient phase margin.

The boost mode gain, G_{BOOST}, is comprised of three components: the analog divider, the pulse width modulator and the power stage. The gain of the analog divider and PWM remain the same as in buck mode operation, but the gain of the power stage in boost mode is given by the following equation:

$$G_{POWER} \cong \frac{V_{OUT}^2}{(1-t_{LOW}f)V_{IN}}$$

By combining the individual terms, the total gain in boost mode can be reduced to the following expression. Notice that unlike in buck mode, the gain in boost mode is a function of both the input and output voltage.

$$G_{BOOST} \cong \frac{29.7V_{OUT}^2}{V_{IN}^2}$$

In boost mode operation, the frequency of the right half plane zero, f_{RHPZ}, is given by the following expression. The frequency of the right half plane zero decreases at higher loads and with larger inductors.

$$f_{RHPZ} = \frac{R(1-t_{LOW}f)^2V_{IN}^2}{2\pi L V_{OUT}^2}$$

In boost mode, the resonant frequency of the power stage has a dependence on the input and output voltage as shown by the following equation.

$$f_O = \frac{1}{2\pi}\sqrt{\frac{R_S+\frac{RV_{IN}^2}{V_{OUT}^2}}{LC_O(R+R_C)}} \cong \frac{1}{2\pi}\bullet\frac{V_{IN}}{V_{OUT}}\sqrt{\frac{1}{LC}}$$

Finally, the magnitude of the quality factor of the power stage in boost mode operation is given by the following expression.

$$Q = \frac{\sqrt{LC_OR\left(R_S+\frac{RV_{IN}^2}{V_{OUT}^2}\right)}}{L+C_OR_SR}$$

APPLICATIONS INFORMATION

Compensation of the Voltage Loop

The small-signal models of the LTC3115-2 reveal that the transfer function from the error amplifier output, VC, to the output voltage is characterized by a set of resonant poles and a possible zero generated by the ESR of the output capacitor as shown in the Bode plot of Figure 7. In boost mode operation, there is an additional right half plane zero that produces phase lag and increasing gain at higher frequencies. Typically, the compensation network is designed to ensure that the loop crossover frequency is low enough that the phase loss from the right half plane zero is minimized. The low frequency gain in buck mode is a constant, but varies with both V_{IN} and V_{OUT} in boost mode.

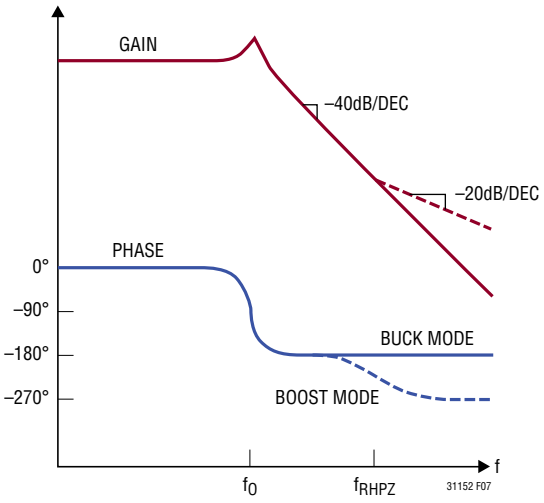

Figure 7. Buck-Boost Converter Bode Plot

For charging or other applications that do not require an optimized output voltage transient response, a simple Type I compensation network as shown in Figure 8 can be used to stabilize the voltage loop. To ensure sufficient phase margin, the gain of the error amplifier must be low enough that the resultant crossover frequency of the control loop is well below the resonant frequency.

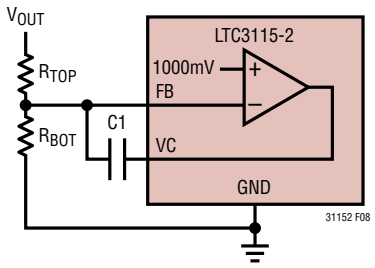

Figure 8. Error Amplifier with Type I Compensation

In most applications, the low bandwidth of the Type I compensated loop will not provide sufficient transient response performance. To obtain a wider bandwidth feedback loop, optimize the transient response, and minimize the size of the output capacitor, a Type III compensation network as shown in Figure 9 is required.

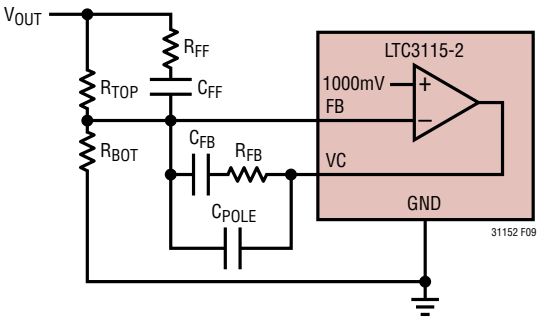

Figure 9. Error Amplifier with Type III Compensation

A Bode plot of the typical Type III compensation network is shown in Figure 10. The Type III compensation network provides a pole near the origin which produces a very high loop gain at DC to minimize any steady-state error in the regulation voltage. Two zeros located at f_{ZERO1} and f_{ZERO2} provide sufficient phase boost to allow the loop crossover frequency to be set above the resonant frequency, f_O, of the power stage. The Type III compensation network also introduces a second and third pole. The second pole, at frequency f_{POLE2}, reduces the error amplifier gain to a zero slope to prevent the loop crossover from extending too high in frequency. The third pole at frequency f_{POLE3} provides attenuation of high frequency switching noise.

APPLICATIONS INFORMATION

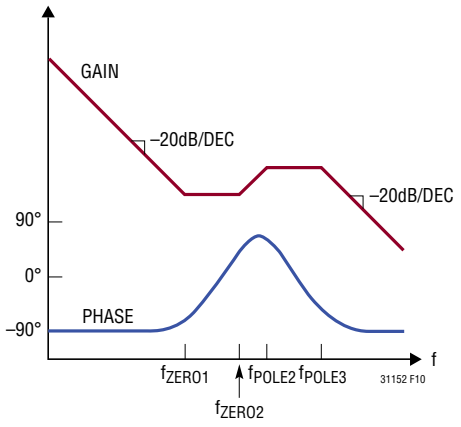

Figure 10. Type III Compensation Bode Plot

The transfer function of the compensated Type III error amplifier from the input of the resistor divider to the output of the error amplifier, VC, is:

$$\frac{V_C(s)}{V_{OUT}(s)} = G_{EA} \frac{\left(1+\frac{s}{2\pi f_{ZERO1}}\right)\left(1+\frac{s}{2\pi f_{ZERO2}}\right)}{s\left(1+\frac{s}{2\pi f_{POLE2}}\right)\left(1+\frac{s}{2\pi f_{POLE3}}\right)}$$

The error amplifier gain is given by the following equation. The simpler approximate value is sufficiently accurate in most cases since C_{FB} is typically much larger in value than C_{POLE}.

$$G_{EA} = \frac{1}{R_{TOP}\left(C_{FB}+C_{POLE}\right)} \cong \frac{1}{R_{TOP}C_{FB}}$$

The pole and zero frequencies of the Type III compensation network can be calculated from the following equations where all frequencies are in Hz, resistances are in ohms, and capacitances are in farads.

$$f_{ZERO1} = \frac{1}{2\pi R_{FB}C_{FB}}$$

$$f_{ZERO2} = \frac{1}{2\pi\left(R_{TOP}+R_{FF}\right)C_{FF}} \cong \frac{1}{2\pi R_{TOP}C_{FF}}$$

$$f_{POLE2} = \frac{C_{FB}+C_{POLE}}{2\pi C_{FB}C_{POLE}R_{FB}} \cong \frac{1}{2\pi C_{POLE}R_{FB}}$$

$$f_{POLE3} = \frac{1}{2\pi C_{FF}R_{FF}}$$

In most applications the compensation network is designed so that the loop crossover frequency is above the resonant frequency of the power stage, but sufficiently below the boost mode right half plane zero to minimize the additional phase loss. Once the crossover frequency is decided upon, the phase boost provided by the compensation network is centered at that point in order to maximize the phase margin. A larger separation in frequency between the zeros and higher order poles will provide a higher peak phase boost but may also increase the gain of the error amplifier which can push out the loop crossover to a higher frequency.

The Q of the power stage can have a significant influence on the design of the compensation network because it determines how rapidly the 180° of phase loss in the power stage occurs. For very low values of series resistance, R_S, the Q will be higher and the phase loss will occur sharply. In such cases, the phase of the power stage will fall rapidly to –180° above the resonant frequency and the total phase margin must be provided by the compensation network. However, with higher losses in the power stage (larger R_S) the Q factor will be lower and the phase loss will occur more gradually. As a result, the power stage phase will not be as close to –180° at the crossover frequency and less phase boost is required of the compensation network.

The LTC3115-2 error amplifier is designed to have a fixed maximum bandwidth in order to provide rejection of switching noise to prevent it from interfering with the control loop. From a frequency domain perspective, this can be viewed as an additional single pole as illustrated in Figure 11. The nominal frequency of this pole is 300kHz. For typical loop crossover frequencies below about 50kHz the phase contributed by this additional pole is negligible. However, for loops with higher crossover frequencies this additional phase loss should be taken into account when designing the compensation network.

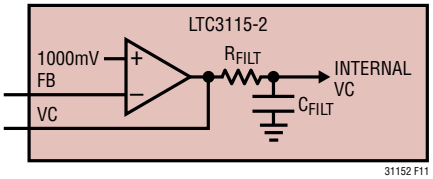

Figure 11. Internal Loop Filter

APPLICATIONS INFORMATION

Loop Compensation Example

This section provides an example illustrating the design of a compensation network for a typical LTC3115-2 application circuit. In this example a 5V regulated output voltage is generated with the ability to supply a 500mA load from an input power source ranging from 3.5V to 30V. To reduce switching losses a 750kHz switching frequency has been chosen for this example. In this application the maximum inductor current ripple will occur at the highest input voltage. An inductor value of 8.2µH has been chosen to limit the worst-case inductor current ripple to approximately 600mA. A low ESR output capacitor with a value of 20µF is specified to yield a worst-case output voltage ripple (occurring at the worst-case step-up ratio and maximum load current) of approximately 12mV. In summary, the key power stage specifications for this LTC3115-2 example application are given below.

f = 0.75MHz, t_{LOW} = 0.1µs

V_{IN} = 3.5V to 30V

V_{OUT} = 5V at 500mA

C_{OUT} = 20µF, R_C = 10mΩ

L = 8.2µH, R_L = 45mΩ

With the power stage parameters specified, the compensation network can be designed. In most applications, the most challenging compensation corner is boost mode operation at the greatest step-up ratio and highest load current since this generates the lowest frequency right half plane zero and results in the greatest phase loss. Therefore, a reasonable approach is to design the compensation network at this worst-case corner and then verify that sufficient phase margin exists across all other operating conditions. In this example application, at V_{IN} = 3.5V and the full 500mA load current, the right half plane zero will be located at 81kHz and this will be a dominant factor in determining the bandwidth of the control loop.

The first step in designing the compensation network is to determine the target crossover frequency for the compensated loop. A reasonable starting point is to assume that the compensation network will generate a peak phase boost of approximately 60°. Therefore, in order to obtain a phase margin of 60°, the loop crossover frequency, f_C, should be selected as the frequency at which the phase of the buck-boost converter reaches –180°. As a result, at the loop crossover frequency the total phase will be simply the 60° of phase provided by the error amplifier as shown:

$$\text{Phase Margin} = \phi_{\text{BUCK-BOOST}} + \phi_{\text{ERRORAMPLIFIER}} + 180°$$
$$= -180° + 60° + 180° = 60°$$

Similarly, if a phase margin of 45° is required, the target crossover frequency should be picked as the frequency at which the buck-boost converter phase reaches –195° so that the combined phase at the crossover frequency yields the desired 45° of phase margin.

This example will be designed for a 60° phase margin to ensure adequate performance over parametric variations and varying operating conditions. As a result, the target crossover frequency, f_C, will be the point at which the phase of the buck-boost converter reaches –180°. It is generally difficult to determine this frequency analytically given that it is significantly impacted by the Q factor of the resonance in the power stage. As a result, it is best determined from a Bode plot of the buck-boost converter as shown in Figure 12. This Bode plot is for the LTC3115-2 buck-boost converter using the previously specified power stage parameters and was generated from the small-signal model equations using LTspice® software. In this case, the phase reaches –180° at 24kHz making f_C = 24kHz the target crossover frequency for the compensated loop.

From the Bode plot of Figure 12 the gain of the power stage at the target crossover frequency is 19dB. Therefore, in order to make this frequency the crossover frequency in the compensated loop, the total loop gain at f_C must be adjusted to 0dB. To achieve this, the gain of the compensation network must be designed to be –19dB at the crossover frequency.

APPLICATIONS INFORMATION

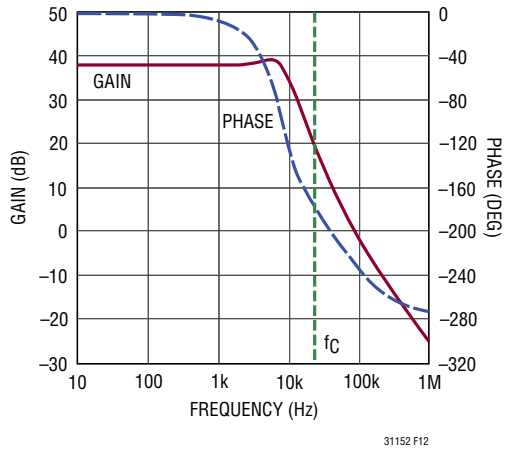

Figure 12. Converter Bode Plot, V_{IN} = 3.5V, I_{LOAD} = 500mA

At this point in the design process, there are three constraints that have been established for the compensation network. It must have –19dB gain at f_C = 24kHz, a peak phase boost of 60° and the phase boost must be centered at f_C = 24kHz. One way to design a compensation network to meet these targets is to simulate the compensated error amplifier Bode plot in LTspice for the typical compensation network shown on the front page of this data sheet. Then, the gain, pole frequencies and zero frequencies can be iteratively adjusted until the required constraints are met.

Alternatively, an analytical approach can be used to design a compensation network with the desired phase boost, center frequency and gain. In general, this procedure can be cumbersome due to the large number of degrees of freedom in a Type III compensation network. However the design process can be simplified by assuming that both compensation zeros occur at the same frequency, f_Z, and both higher order poles (f_{POLE2} and f_{POLE3}) occur at the common frequency, f_P. In most cases this is a reasonable assumption since the zeros are typically located between 1kHz and 10kHz and the poles are typically located near each other at much higher frequencies. Given this assumption, the maximum phase boost, f_{MAX}, provided by the compensated error amplifier is determined simply by the amount of separation between the poles and zeros as shown by the following equation:

$$\phi_{MAX} = 4\tan^{-1}\left(\sqrt{\frac{f_P}{f_Z}}\right) - 270^\circ$$

A reasonable choice is to pick the frequency of the poles, f_P, to be about 50 times higher than the frequency of the zeros, f_Z, which provides a peak phase boost of approximately ϕ_{MAX} = 60° as was assumed previously. Next, the phase boost must be centered so that the peak phase occurs at the target crossover frequency. The frequency of the maximum phase boost, f_{CENTER}, is the geometric mean of the pole and zero frequencies as:

$$f_{CENTER} = \sqrt{f_P \bullet f_Z} = \sqrt{50} \bullet f_Z \cong 7 \bullet f_Z$$

Therefore, in order to center the phase boost given a factor of 50 separation between the pole and zero frequencies, the zeros should be located at one seventh of the crossover frequency and the poles should be located at seven times the crossover frequency as given by the following equations:

$$f_Z = \frac{1}{7} \bullet f_C = \frac{1}{7}(24kHz) = 3.43kHz$$

$$f_P = 7 \bullet f_C = 7(24kHz) = 168kHz$$

This placement of the poles and zeros will yield a peak phase boost of 60° that is centered at the crossover frequency, f_C. Next, in order to produce the desired target crossover frequency, the gain of the compensation network at the point of maximum phase boost, G_{CENTER}, must be set to –19dB. The gain of the compensated error amplifier at the point of maximum phase gain is given by:

$$G_{CENTER} = 10\log\left[\frac{2\pi f_P}{(2\pi f_Z)^3 (R_{TOP} C_{FB})^2}\right] dB$$

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Assuming a multiple of 50 separation between the pole frequencies and zero frequencies this can be simplified to the following expression:

$$G_{CENTER} = 20\log\left[\frac{50}{2\pi f_C R_{TOP} C_{FB}}\right] dB$$

This equation completes the set of constraints needed to determine the compensation component values. Specifically, the two zeros, f_{ZERO1} and f_{ZERO2}, should be located near 3.43kHz. The two poles, f_{POLE2} and f_{POLE3}, should be located near 168kHz and the gain should be set to provide a gain at the crossover frequency of G_{CENTER} = –19dB.

The first step in defining the compensation component values is to pick a value for R_{TOP} that provides an acceptably low quiescent current through the resistor divider. A value of R_{TOP} = 1MΩ is a reasonable choice. Next, the value of C_{FB} can be found in order to set the error amplifier gain at the crossover frequency to –19dB as follows:

$$G_{CENTER} = -19.1dB$$

$$= 20\log\left[\frac{50}{2\pi(24kHz)(1M\Omega)C_{FB}}\right]$$

$$C_{FB} = \frac{50}{2\pi(24kHz)(1M\Omega)a\log\left(\frac{-19.1}{20}\right)} @3.0nF$$

The compensation poles can be set at 168kHz and the zeros at 3.43kHz by using the expressions for the pole and zero frequencies given in the previous section. Setting the frequency of the first zero, f_{ZERO1}, to 3.43kHz results in the following value for R_{FB}:

$$R_{FB} = \frac{1}{2\pi(3nF)(3.43kHz)} \cong 15.4k\Omega$$

This leaves the free parameter, C_{POLE}, to set the frequency f_{POLE1} to the common pole frequency of 168kHz as given:

$$C_{POLE} = \frac{1}{2\pi(15.4k\Omega)(168kHz)} \cong 62pF$$

Next, C_{FF} can be chosen to set the second zero, f_{ZERO2}, to the common zero frequency of 3.43kHz.

$$C_{FF} = \frac{1}{2\pi(1M\Omega)(3.43kHz)} \cong 47pF$$

Finally, the resistor value R_{FF} can be chosen to place the second pole at 168kHz.

$$R_{FF} = \frac{1}{2\pi(47pF)(168Hz)} \cong 20.0k\Omega$$

Now that the pole frequencies, zero frequencies and gain of the compensation network have been established, the next step is to generate a Bode plot for the compensated error amplifier to confirm its gain and phase properties. A Bode plot of the error amplifier with the designed compensation component values is shown in Figure 13. The Bode plot confirms that the peak phase occurs at 24kHz and the phase boost at that point is 57.7°. In addition, the gain at the peak phase frequency is –19.3dB which is close to the design target.

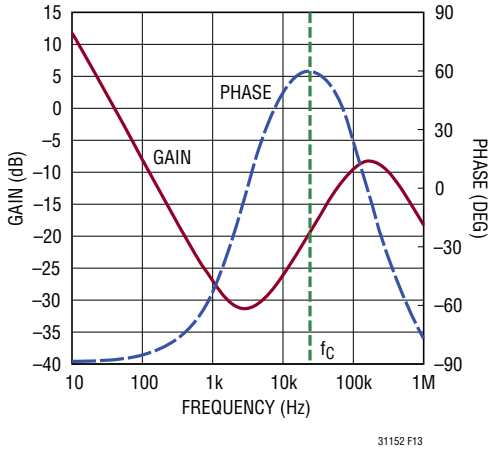


Figure 13. Compensated Error Amplifier Bode Plot

APPLICATIONS INFORMATION

The final step in the design process is to compute the Bode plot for the entire loop using the designed compensation network and confirm its phase margin and crossover frequency. The complete loop Bode plot for this example is shown in Figure 14. The loop crossover frequency is 22kHz which is close to the design target and the phase margin is approximately 60°.

The Bode plot for the complete loop should be checked over all operating conditions and for variations in component values to ensure that sufficient phase margin exists in all cases. The stability of the loop should also be confirmed via time domain simulation and by evaluating the transient response of the converter in the actual circuit.

Output Voltage Programming

The output voltage is set via the external resistor divider comprised of resistors R_{TOP} and R_{BOT} as show in Figures 8 and 9. The resistor divider values determine the output regulation voltage according to:

$$V_{OUT} = 1.000V\left(1+\frac{R_{TOP}}{R_{BOT}}\right)$$

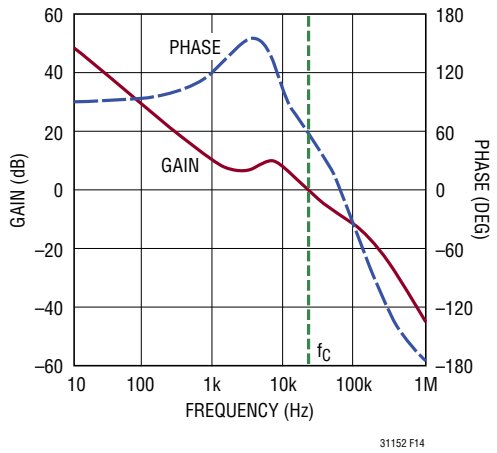


Figure 14. Complete Loop Bode Plot

In addition to setting the output voltage, the value of R_{TOP} is instrumental in controlling the dynamics of the compensation network. When changing the value of this resistor, care must be taken to understand the impact this will have on the compensation network.

In addition to setting the output voltage, the Thevenin equivalent resistance of the resistor divider determines the gain of the current limit. For applications with a top divider resistor (R_{TOP}) of less than 1M, it is recommended that components R1 and C1 be added at the FB pin as shown in Figure 15 to maintain the gain of the current limit loop and minimize overshot on recovery from output short circuits. This additional circuit has no impact on compensation of the control loop.

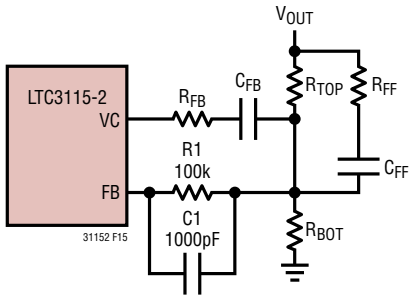


Figure 15. R1 and C1 are Recommended if R_{TOP} < 1MΩ

Switching Frequency Selection

The switching frequency is set by the value of a resistor connected between the RT pin and ground. The switching frequency, f, is related to the resistor value by the following equation where R_T is the resistance:

$$f = \frac{35.7MHz}{(R_T/k\Omega)}$$

Higher switching frequencies facilitate the use of smaller inductors as well as smaller input and output filter capacitors which results in a smaller solution size and reduced component height. However, higher switching frequencies also generally reduce conversion efficiency due to the increased switching losses.

In addition, higher switching frequencies (above 750kHz) will reduce the maximum output current that can be supplied (see Typical Performance Characteristics for details). For applications with $V_{OUT} \geq 20V$, a maximum switching frequency of 1MHz is recommended.

APPLICATIONS INFORMATION

PCB Layout Considerations

The LTC3115-2 buck-boost converter switches large currents at high frequencies. Special attention should be paid to the PC board layout to ensure a stable, noise-free and efficient application circuit. Figures 17 and 18 show a representative PCB layout for each package option to outline some of the primary considerations. A few key guidelines are provided below:

1. The parasitic inductance and resistance of all circulating high current paths should be minimized. This can be accomplished by keeping the routes to all bold components in Figures 17 and 18 as short and as wide as possible. Capacitor ground connections should via down to the ground plane by way of the shortest route possible. The bypass capacitors on PV_{IN}, PV_{OUT} and PV_{CC}/V_{CC} should be placed as close to the IC as possible and should have the shortest possible paths to ground.
2. The exposed pad is the electrical power ground connection for the LTC3115-2 in the DHD package. Multiple vias should connect the backpad directly to the ground plane. In addition, maximization of the metallization connected to the backpad will improve the thermal environment and improve the power handling capabilities of the IC in both the FE and DHD packages.
3. The components shown in bold and their connections should all be placed over a complete ground plane to minimize loop cross-sectional areas. This minimizes EMI and reduces inductive drops.
4. Connections to all of the components shown in bold should be made as wide as possible to reduce the series resistance. This will improve efficiency and maximize the output current capability of the buck-boost converter.
5. To prevent large circulating currents in the ground plane from disrupting operation of the LTC3115-2, all small-signal grounds should return directly to GND by way of a dedicated Kelvin route. This includes the ground connection for the RT pin resistor, and the ground connection for the feedback network as shown in Figures 17 and 18.
6. Keep the routes connecting to the high impedance, noise sensitive inputs FB and RT as short as possible to reduce noise pick-up.
7. The BST1 and BST2 pins transition at the switching frequency to the full input and output voltage respectively. To minimize radiated noise and coupling, keep the BST1 and BST2 routes as short as possible and away from all sensitive circuitry and pins (VC, FB, RT). In many applications the length of traces connecting to the boost capacitors can be minimized by placing the boost capacitors on the back side of the PC board and routing to them via traces on an internal copper layer.

8 Connections from the BST1 and BST2 capacitors must Kelvin directly back to the respective SW pin as shown in Figure 16.

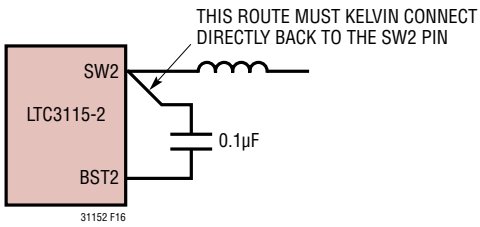


Figure 16. Kelvin BST Connections

9. If the optional Schottky diode from SW2 to PV_{OUT} is utilized, the Schottky should be placed as close to the SW2 and PV_{OUT} pins as possible and connected with the shortest possible traces.

APPLICATIONS INFORMATION

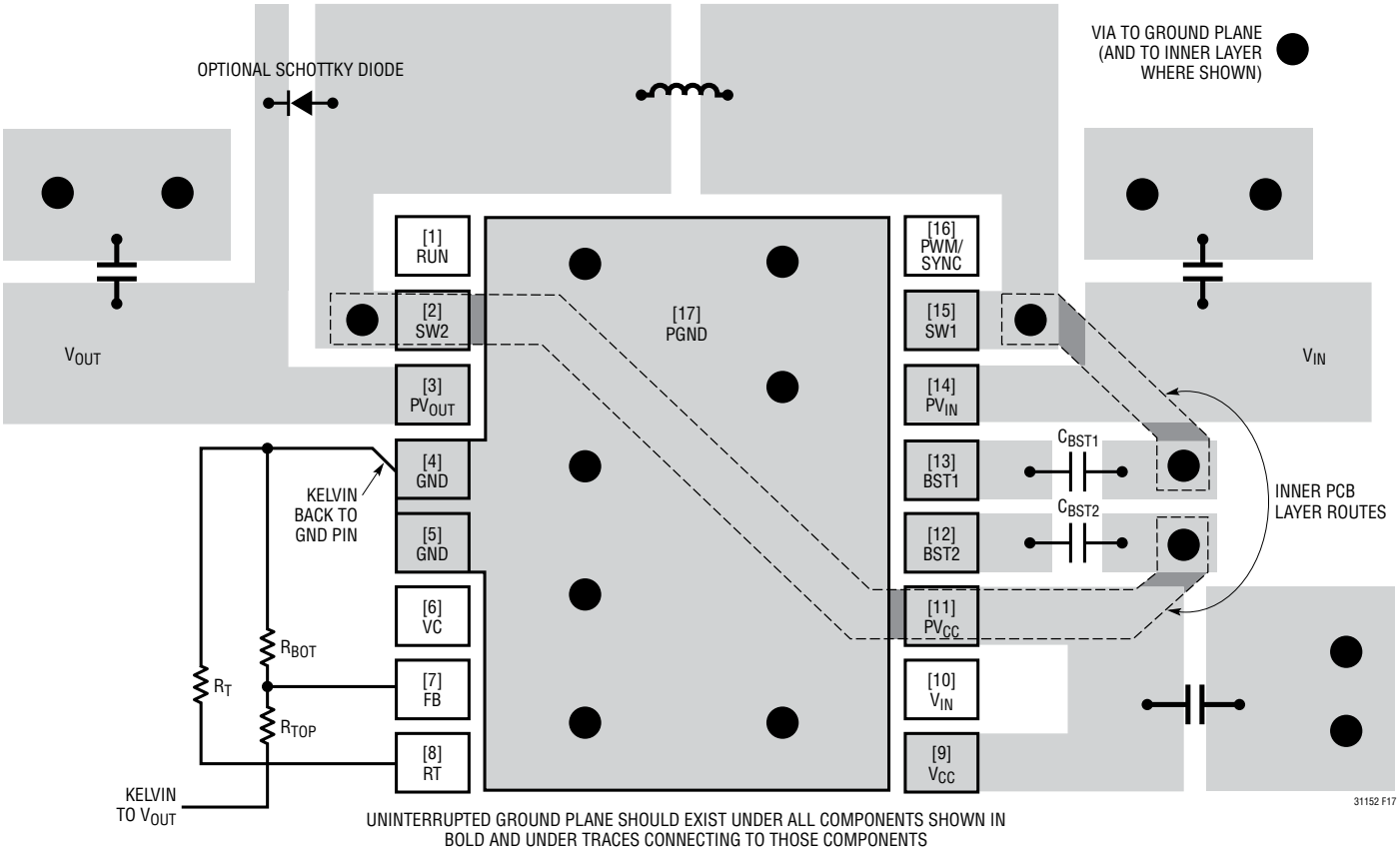


Figure 17. PCB Layout Recommended for the DHD Package

APPLICATIONS INFORMATION

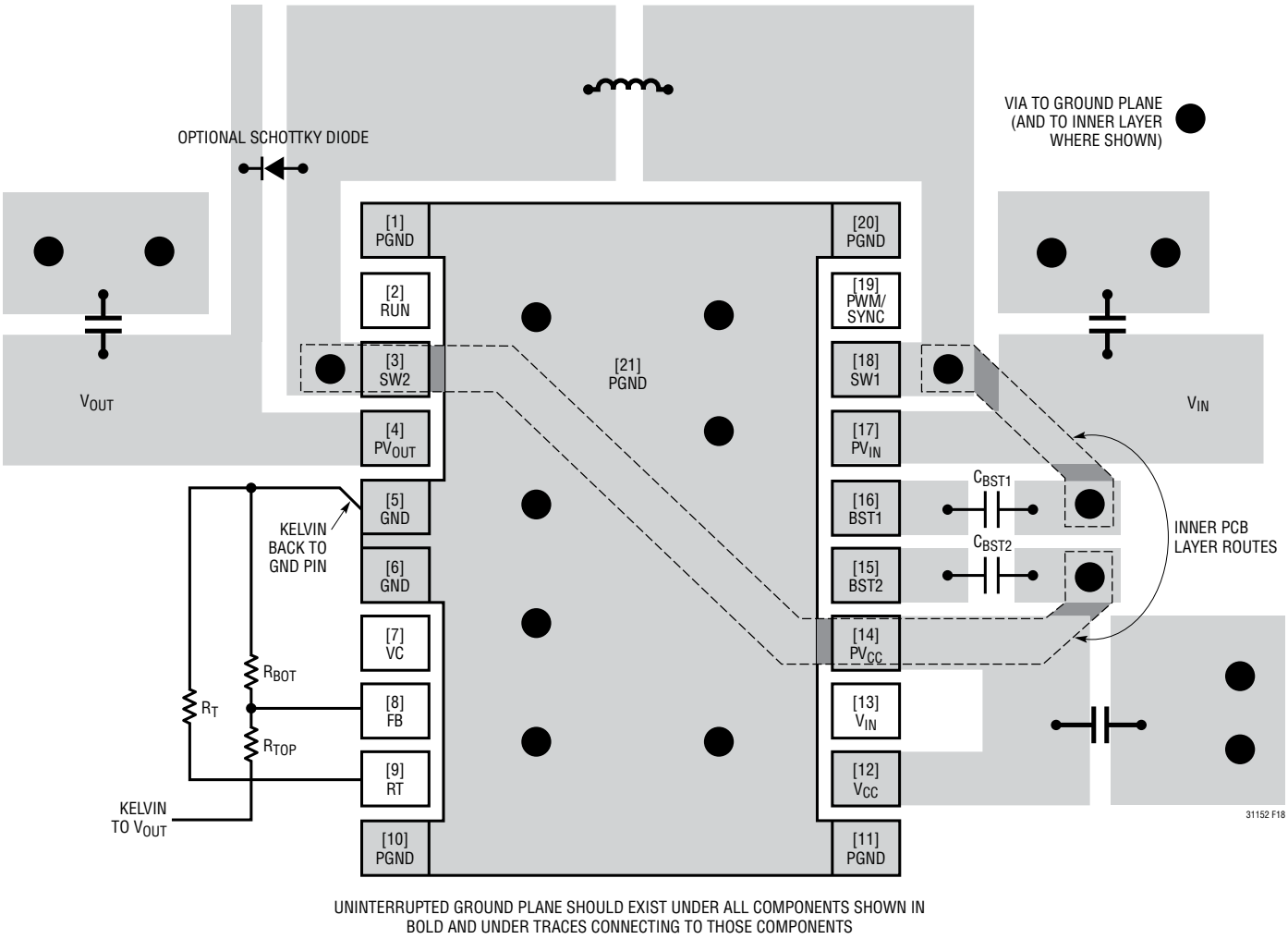
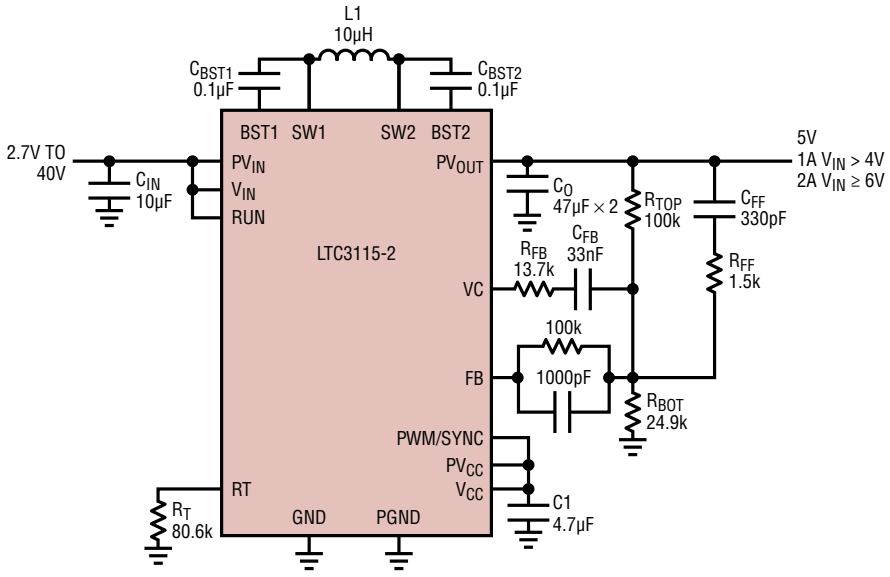


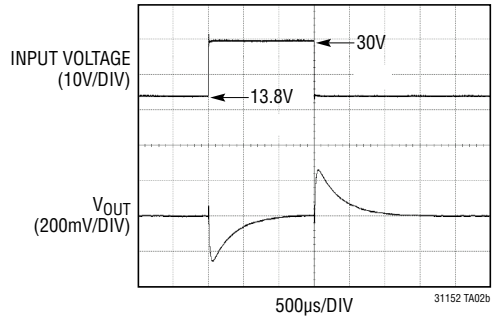
Figure 18. PCB Layout Recommended for the FE Package

TYPICAL APPLICATIONS

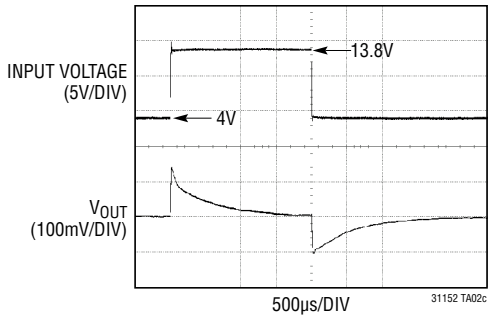
Automotive 450kHz Regulator with 100k Maximum Resistor Value



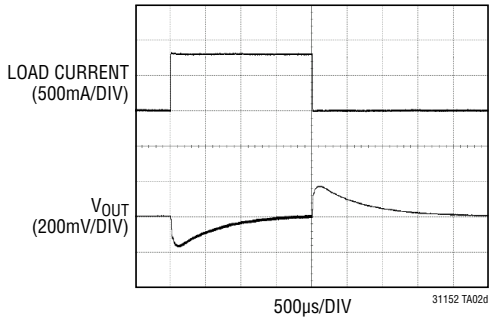
Fast (10µs) Line Transient from V_{IN} = 13.8V to 30V



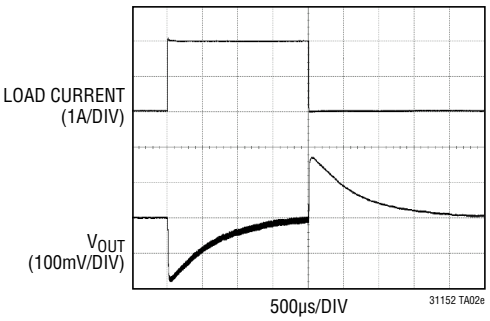
Fast (10µs) Line Transient from V_{IN} = 4V to 13.8V



0A to 800mA Load Step, V_{IN} = 3.6V

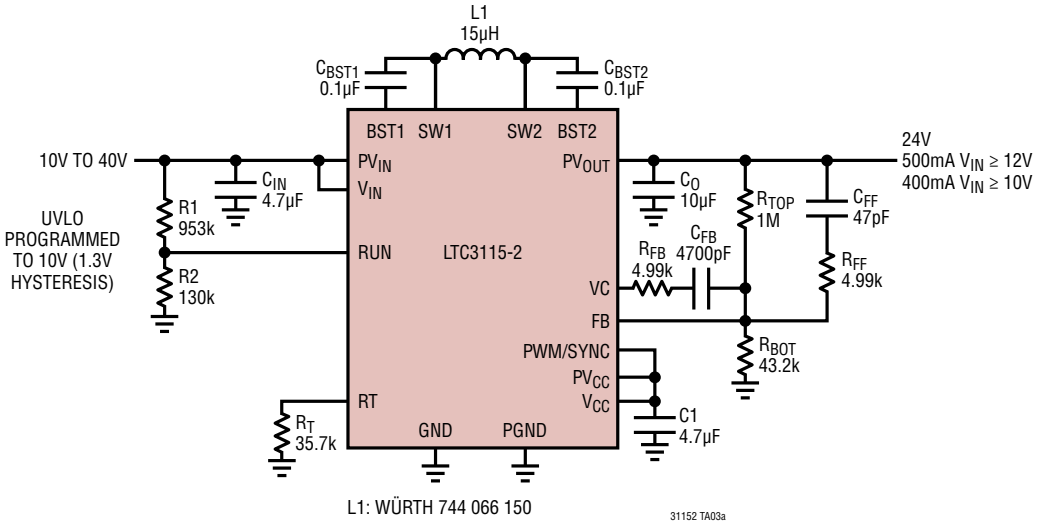


0A to 2A Load Step, V_{IN} = 13.8V

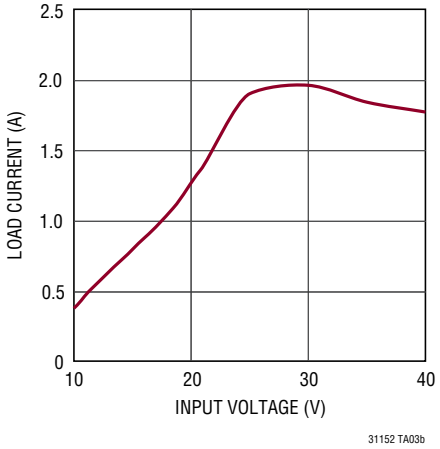


TYPICAL APPLICATIONS

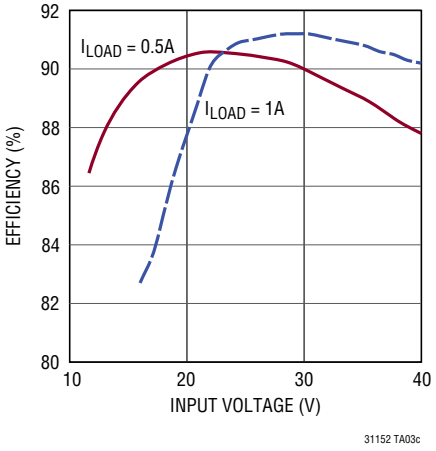
Wide Input Voltage Range (10V to 40V) 1MHz 24V Supply at 400mA



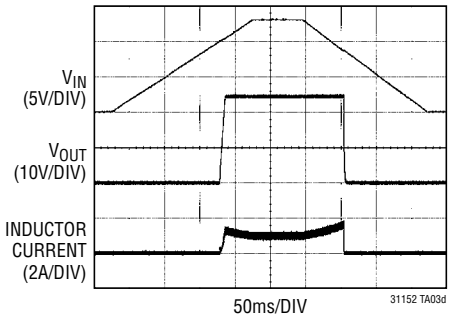
Maximum Load Current vs V_{IN}



Efficiency vs V_{IN}

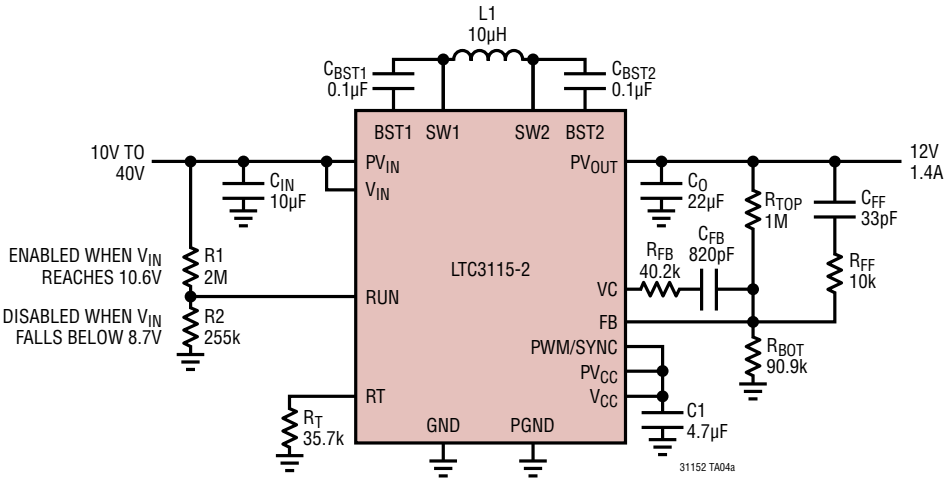


Power-Up/Down Waveforms, I_{LOAD} = 0.5A



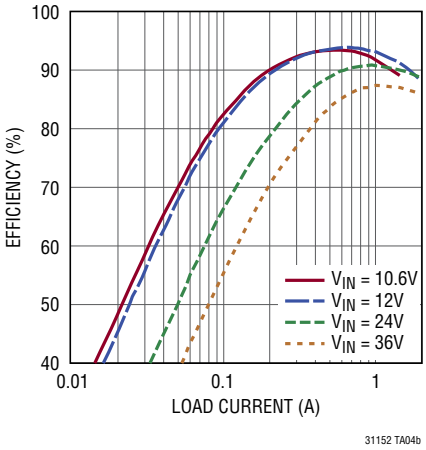
TYPICAL APPLICATIONS

Industrial 12V 1MHz Regulator with 10.6V Input Undervoltage Lockout Threshold

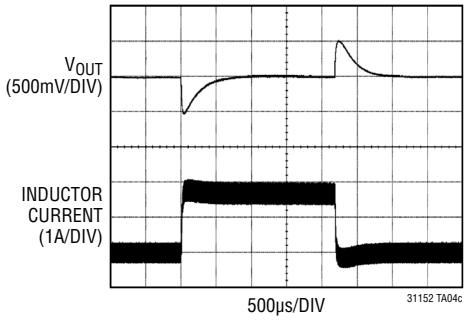


CIN: MURATA GRM55DR61H106K
CO: TDK CKG57NX5R1H226M
L1: WÜRTH 744 066 100

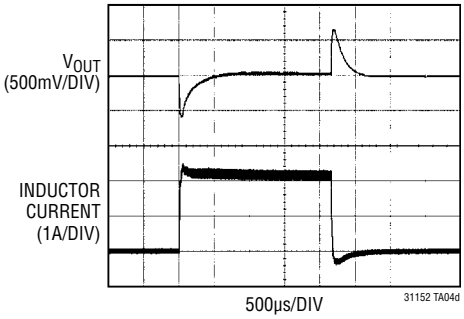
PWM Mode Efficiency vs Load Current



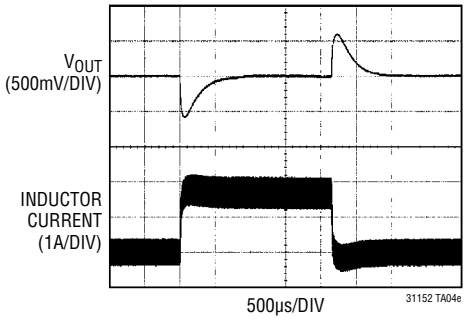
0A to 1.5A Load Step, V_{IN} = 24V



0A to 1.5A Load Step, V_{IN} = 10.6V

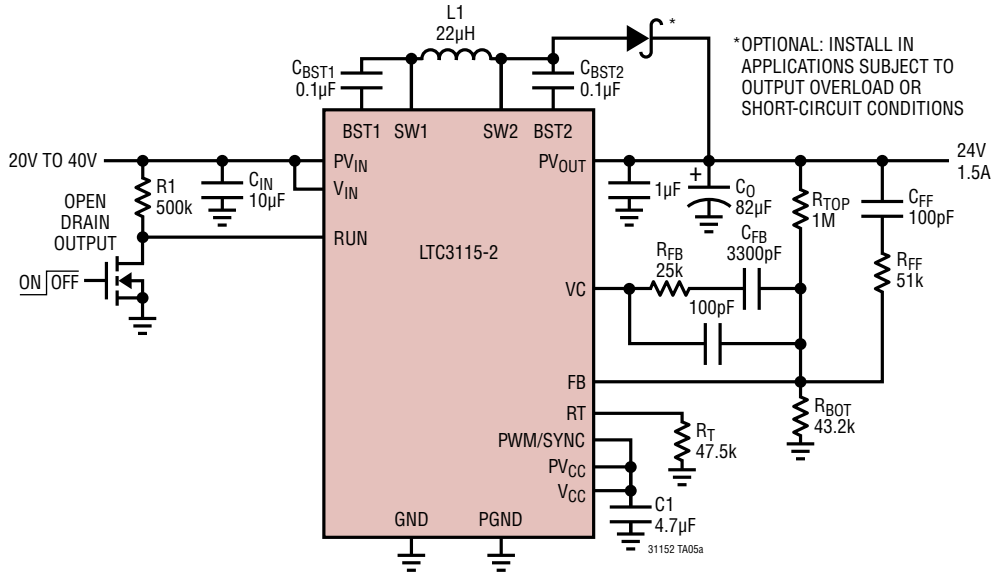


0A to 1.5A Load Step, V_{IN} = 40V



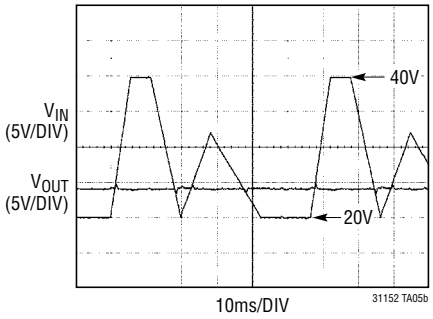
TYPICAL APPLICATIONS

24V 750kHz Industrial Power Rail from 20V to 40V Input

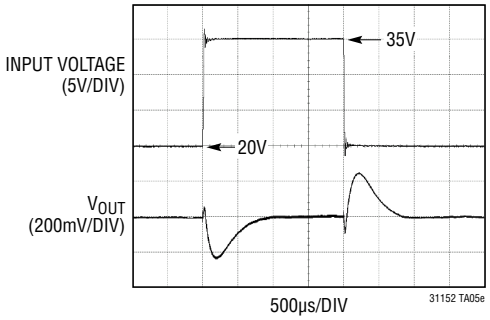


CO: OS-CON 35SVPF82M
WÜRTH: 744 066 220

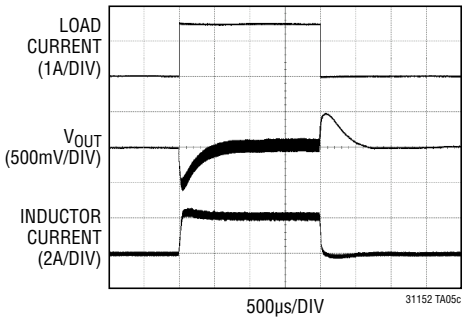
Regulated Output Voltage from a Time Varying Input Rail



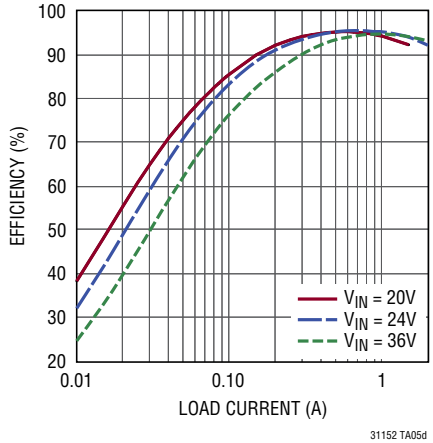
Fast (20µs) Input Voltage Transient, V_{IN} = 20V to 35V



0A to 1.5A Load Step, V_{IN} = 20V

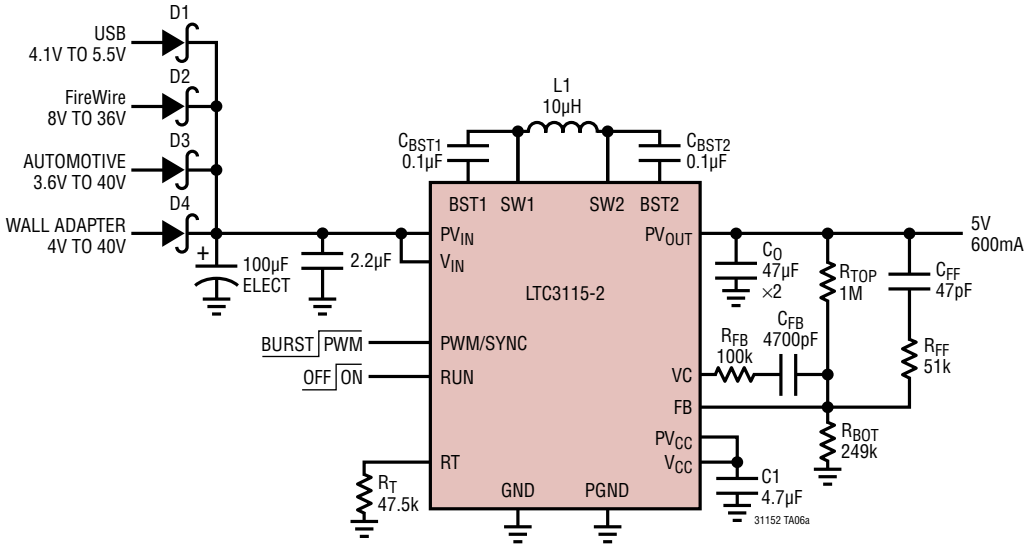


Efficiency vs Load Current



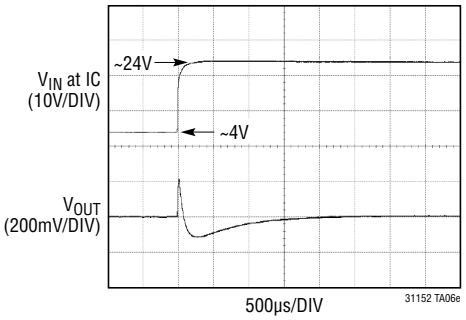
TYPICAL APPLICATIONS

USB, FireWire, Automotive and Unregulated Wall Adapter to Regulated 5V (750kHz)

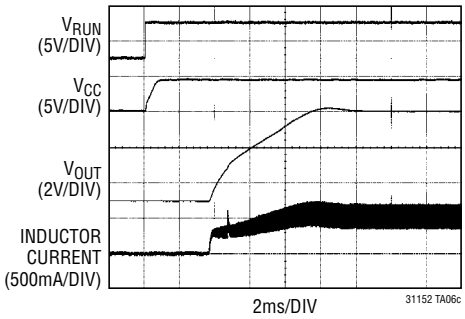


C_{IN}: MURATA GRM55DR61H106K
C_O: GRM43ER60J476
D1-D4: B360A-13-F
L1: COILCRAFT LPS6225

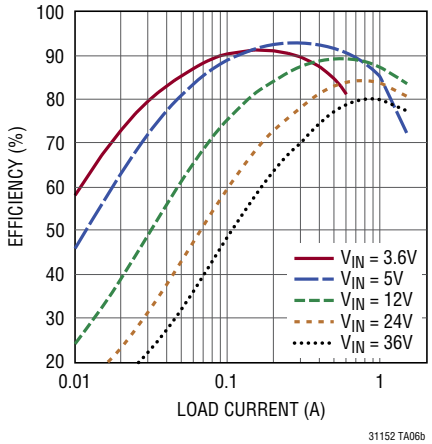
Hot Plug on Firewire Input from V_{IN} = 4V to 24V



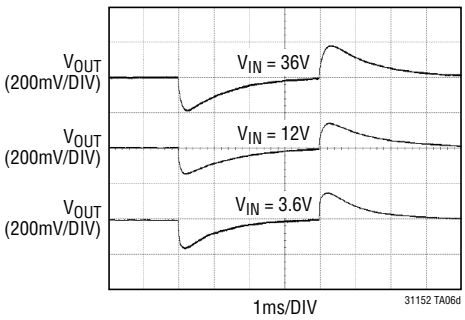
Soft-Start Waveform, V_{IN} = 24V, I_{LOAD} = 0.5A



Efficiency vs Load Current, from Automotive Input

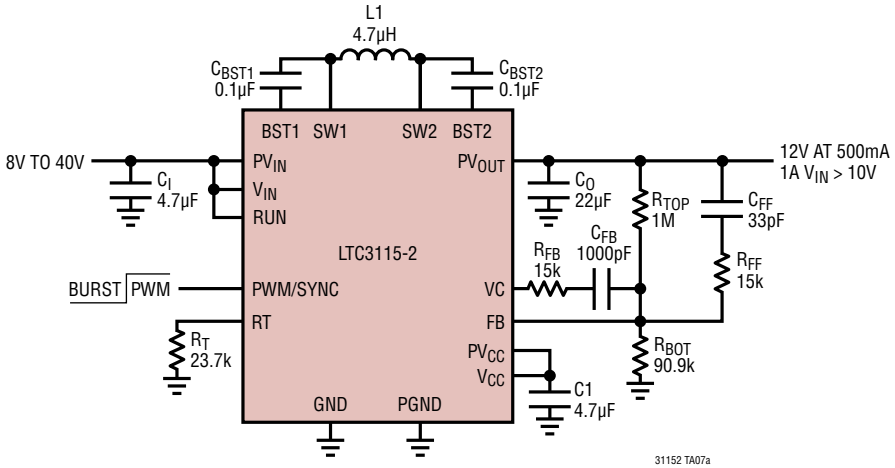


Output Voltage Transient Response, 600mA Load Step, Powered from Automotive Input



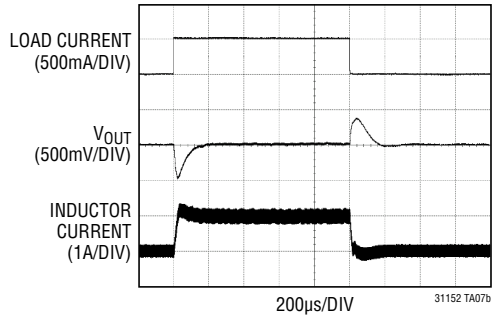
TYPICAL APPLICATIONS

1.5MHz, 12V Regulator with 8V to 40V Input Voltage Range

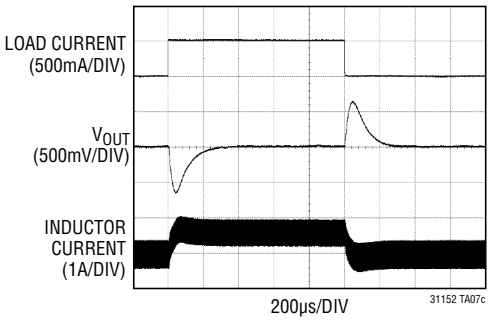


C_O: TDK C3225X7R1C226k
L1: COILCRAFT MOS6020-472MX

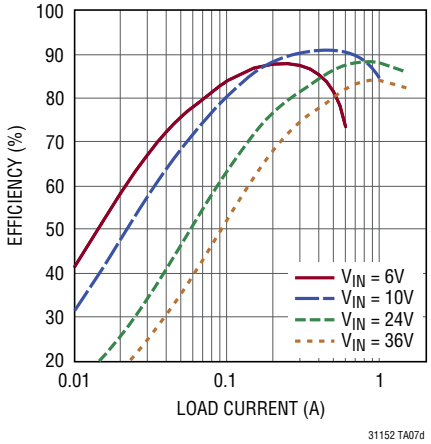
Load Step Transient Response, 0mA to 500mA, V_{IN} = 8V



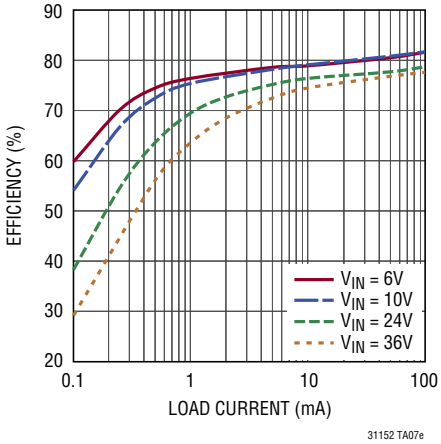
Load Step Transient Response, 0mA to 500mA, V_{IN} = 24V



Efficiency vs Load Current, PWM Mode



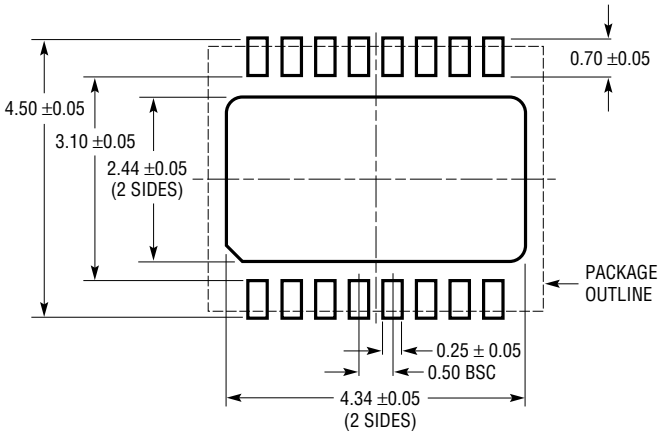
Efficiency vs Load Current, Burst Mode Operation



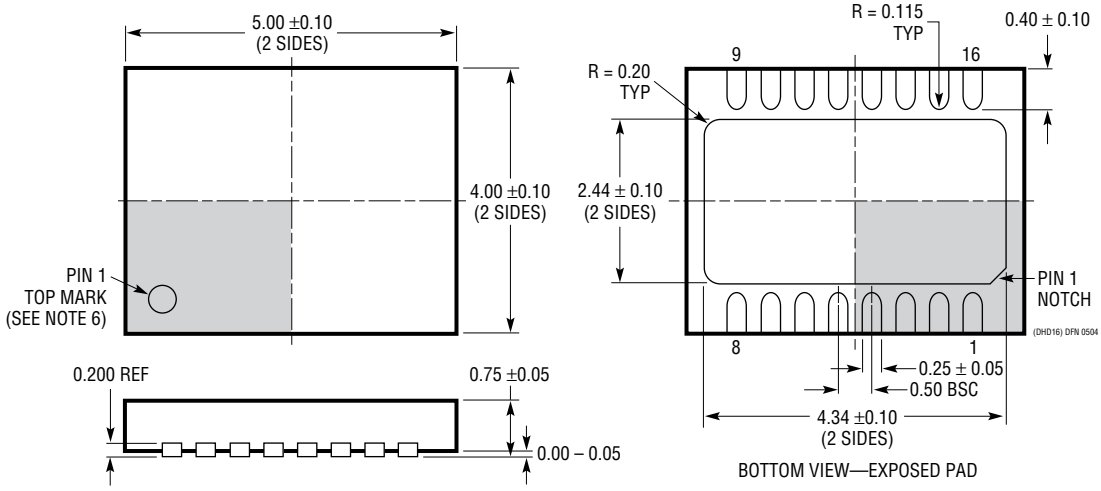
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DHD Package
16-Lead Plastic DFN (5mm × 4mm)
(Reference LTC DWG # 05-08-1707)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



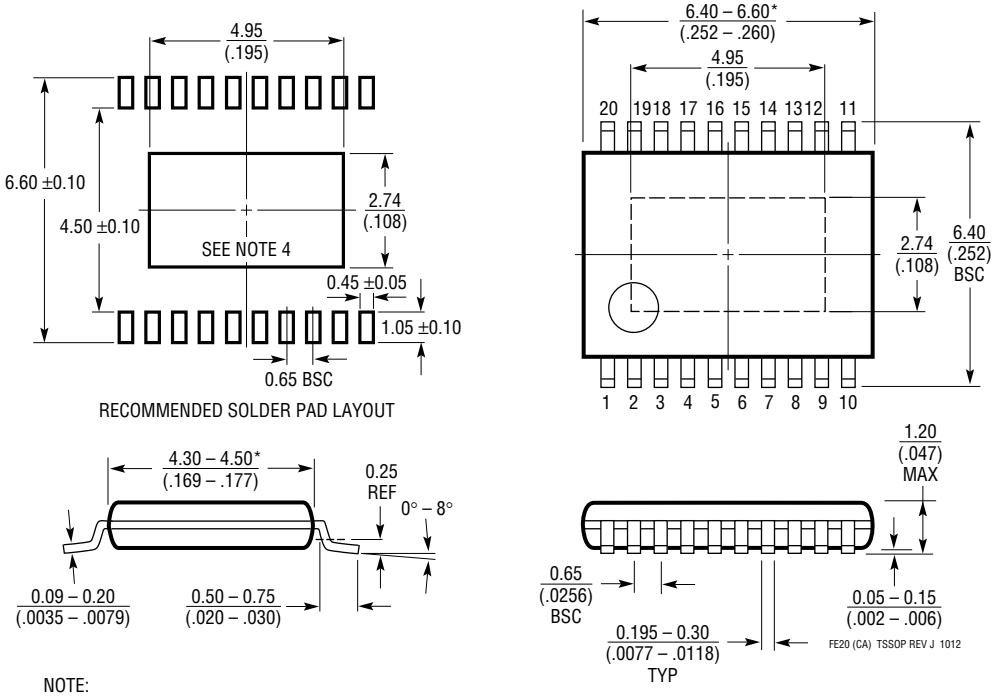
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJGD-2) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev J)
Exposed Pad Variation CA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

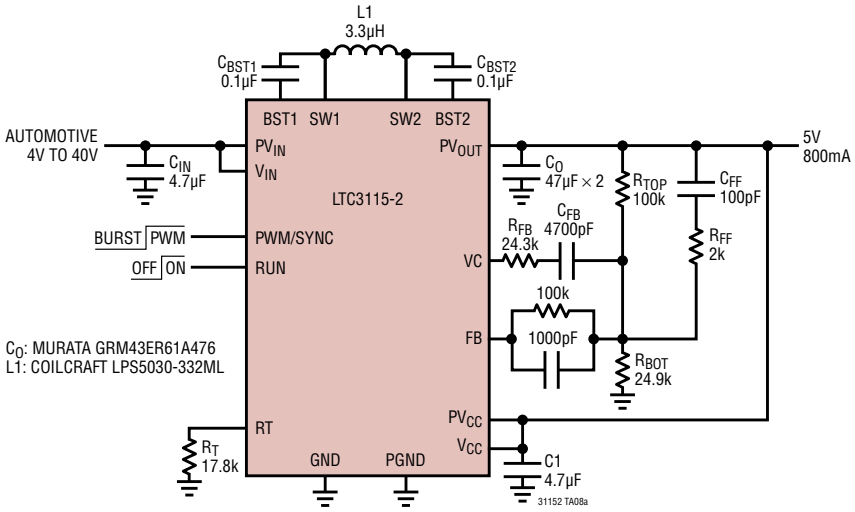
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

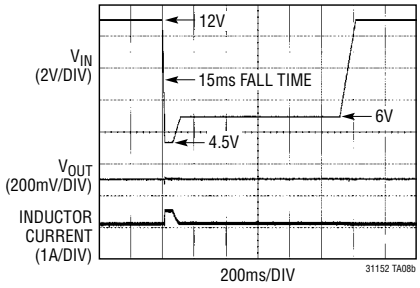
REV	DATE	DESCRIPTION	PAGE NUMBER
A	5/15	Clarified G_{BUCK} formula	22
		Clarified Loop Compensation Example	26
		Clarified PCB Layout Considerations	30, 31, 32
		Added LTC3114-1 to Related Parts list	42

TYPICAL APPLICATION

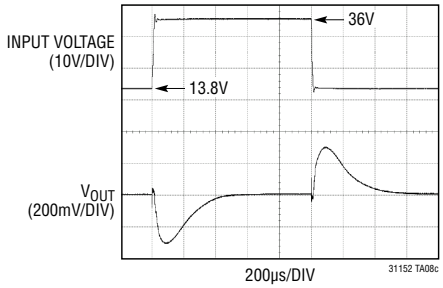
2MHz Automotive 5V Regulator with Cold Crank Capability



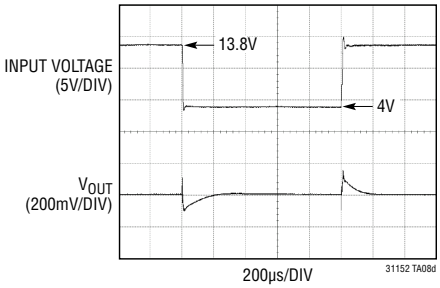
Cold Crank Line Transient with 800mA Load



Fast (10µs) Load Dump Line Transient, V_{IN} = 13.8V to 36V



Fast (10µs) Cold Crank Line Transient, V_{IN} = 13.8V to 4V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3115-1	2A (I_{OUT}), 40V Synchronous Buck-Boost Converter	V_{IN}: 2.7V to 40V, V_{OUT}: 2.7V to 40V, I_Q = 30µA, I_{SD} < 3µA, DFN and TSSOP Packages
LTC3114-1	1A (I_{OUT}), 40V Synchronous Buck-Boost DC/DC Converter	V_{IN} = 2.2V to 40V, V_{OUT}= 2.7V to 40V, I_Q = 30µA, I_{SD} < 3µA, DFN and TSSOP Packages
LTC3112	2.5A (I_{OUT}), 15V Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.7V to 15V, V_{OUT}: 2.5V to 14V, I_Q = 40µA, I_{SD} < 1µA, DFN and TSSOP Packages
LTC3113	3A (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.25V, I_Q = 30µA, ISD < 1µA, DFN and TSSOP Packages
LTC3127	1A (I_{OUT}), 1.2MHz Buck-Boost DC/DC Converter with Programmable Input Current Limit	96% Efficiency V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.25V, I_Q = 35µA, I_{SD} < 4µA, MSOP and DFN Packages
LTC3789	High Efficiency, Synchronous, 4-Switch Buck-Boost Controller	V_{IN}: 4V to 38V, V_{OUT}: 0.8V to 38V, I_Q = 3mA, I_{SD} < 60µA, SSOP-28, QFN-28 Packages
LTC3785	≤10A (I_{OUT}), High Efficiency, 1MHz Synchronous, No R_{SENSE}™ Buck-Boost Controller	V_{IN}: 2.7V to 10V, V_{OUT}: 2.7V to 10V, I_Q = 86µA, I_{SD} < 15µA, QFN Package
LTC3534	7V, 500mA (I_{OUT}), 1MHz Synchronous Buck-Boost DC/DC Converter	94% Efficiency, V_{IN}: 2.4V to 7V, V_{OUT}: 1.8V to 7V, I_Q = 25µA, I_{SD} < 1µA, DFN and GN Packages