File Number **2287**

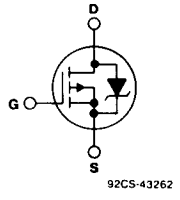
IRFF9120, IRFF9121
IRFF9122, IRFF9123

Avalanche-Energy-Rated P-Channel Power MOSFETs

-3.5 A and -4 A, -60 V, -100 V
$r_{DS(on)}$ = 0.60 Ω and 0.80 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

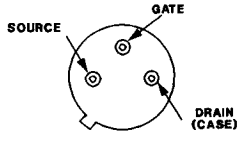


P-CHANNEL ENHANCEMENT MODE

The IRFF9120, IRFF9121, IRFF9122 and IRFF9123 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

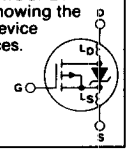
ABSOLUTE-MAXIMUM RATINGS

CHARACTERISTIC		IRFF9120	IRFF9121	IRFF9122	IRFF9123	UNITS
Drain-Source Voltage ①	V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20 kΩ) ①	V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current	I_D @ T_C = 25°C	-4	-4	-3.5	-3.5	A
Pulsed Drain Current ③	I_{DM}	-16	-16	-14	-14	A
Gate-Source Voltage	V_{GS}	±20				V
Maximum Power Dissipation	P_D @ T_C = 25°C	20 (See Fig. 14)				W
Linear Derating Factor		0.16 (See Fig. 14)				W/°C
Single-Pulse Avalanche Energy Rating ④	E_{as}	370				mJ
Operating Junction and Storage Temperature Range	T_J T_{stg}	-55 to +150				°C
Lead Temperature		300 (0.063 in. [1.6 mm] from case for 10 s)				°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFF9120 IRFF9122	-100	—	—	V	V_{GS} = 0 V
		IRFF9121 IRFF9123	-60	—	—	V	I_D = -250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	-100	nA	V_{GS} = -20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	100	nA	V_{GS} = 20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRFF9120 IRFF9121	-4	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRFF9122 IRFF9123	-3.5	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFF9120 IRFF9121	—	0.5	0.6	Ω	V_{GS} = -10 V, I_D = -2 A
		IRFF9122 IRFF9123	—	0.6	0.8	Ω	
Forward Transconductance ②	g_{fs}	ALL	1.25	2	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = -2 A
Input Capacitance	C_{iss}	ALL	—	300	—	pF	V_{GS} = 0 V, V_{DS} = -25 V, f = 1.0 MHz See Fig. 10
Output Capacitance	C_{oss}	ALL	—	200	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	50	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	25	50	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -2 A, Z_O = 50 Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	50	100	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	50	100	ns	
Fall Time	t_f	ALL	—	50	100	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	16	22	nC	V_{GS} = -15 V, I_D = -8 A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	9	13.5	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	7	10.5	nC	
Internal Drain Inductance	L_D	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
Internal Source Inductance	L_S	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

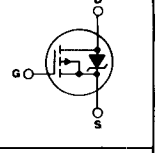


THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$	ALL	—	—	6.25	°C/W	
Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	175	°C/W	Typical socket mount.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFF9120 IRFF9121	—	—	-4	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF9122 IRFF9123	—	—	-3.5	A	
Pulse Source Current (Body Diode) ③	I_{SM}	IRFF9120 IRFF9121	—	—	-16	A	
		IRFF9122 IRFF9123	—	—	-14	A	
Diode Forward Voltage ②	V_{SD}	IRFF9120 IRFF9121	—	—	-1.5	V	T_C = 25°C, I_S = -4 A, V_{GS} = 0 V
		IRFF9122 IRFF9123	—	—	-1.5	V	T_C = 25°C, I_S = -3.5 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	230	—	ns	T_J = 150°C, I_F = -4 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	1.3	—	μC	T_J = 150°C, I_F = -4 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 25 V, Starting T_j = 25°C, L = 34.7 mH, R_G = 25 Ω, Peak I_L = 4 A (See Figs. 15 & 16).

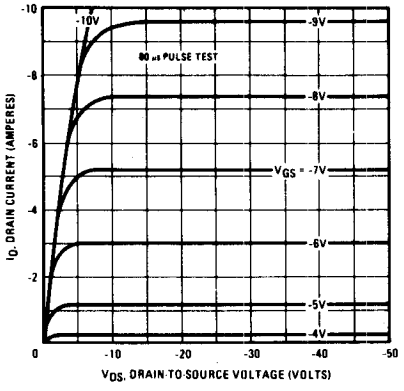


Fig. 1 - Typical output characteristics.

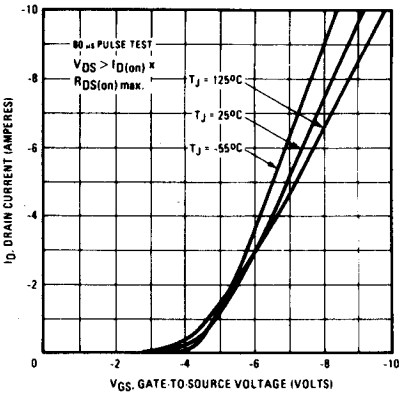


Fig. 2 - Typical transfer characteristics.

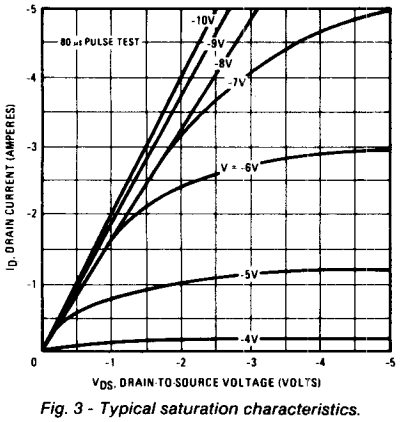


Fig. 3 - Typical saturation characteristics.

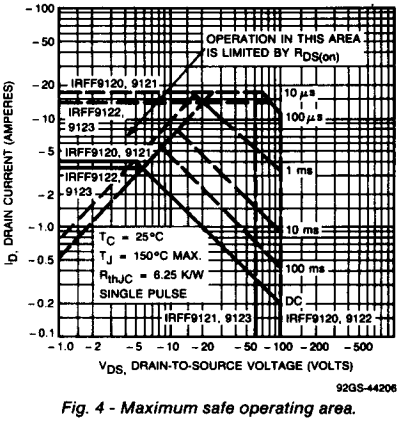


Fig. 4 - Maximum safe operating area.

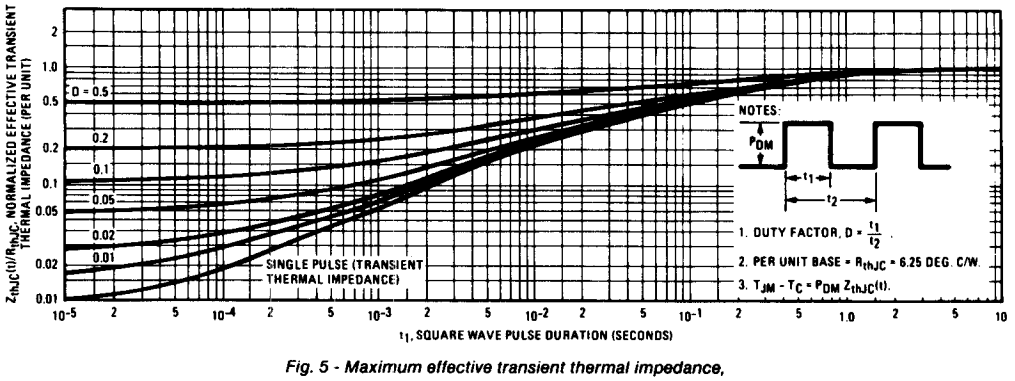


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

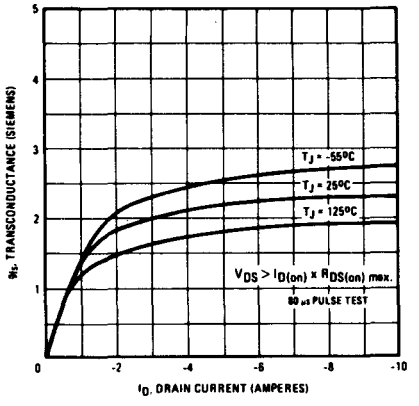


Fig. 6 - Typical transconductance vs. drain current.

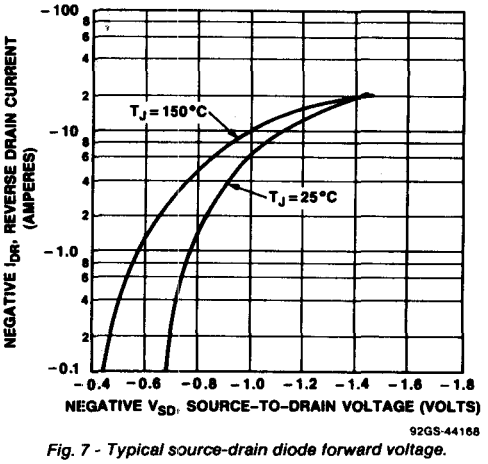


Fig. 7 - Typical source-drain diode forward voltage.

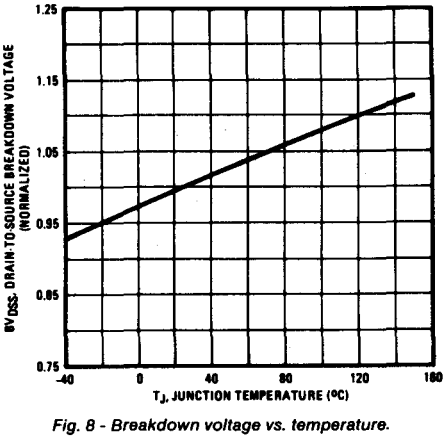


Fig. 8 - Breakdown voltage vs. temperature.

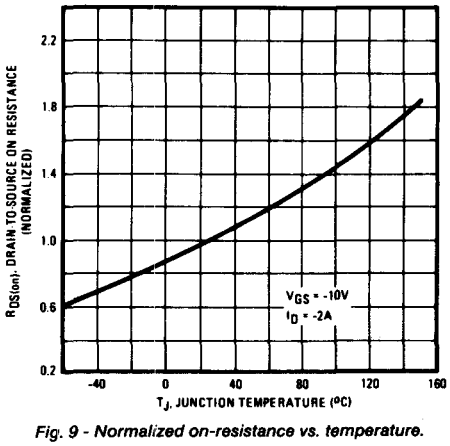


Fig. 9 - Normalized on-resistance vs. temperature.

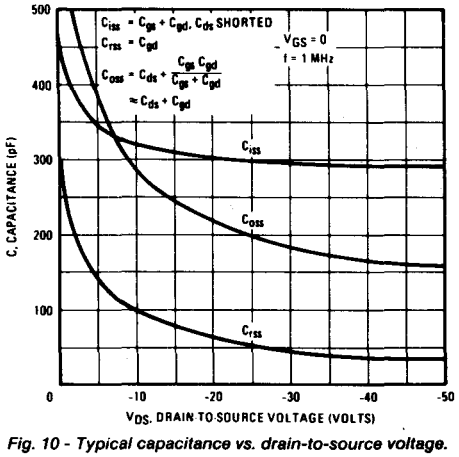


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

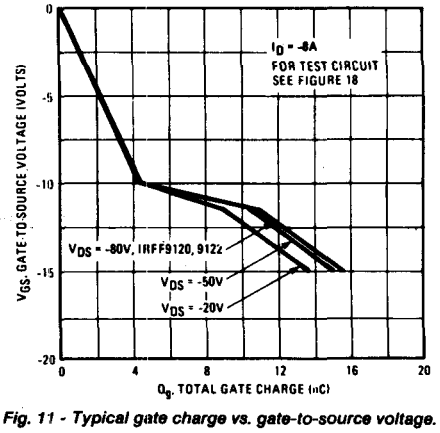


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

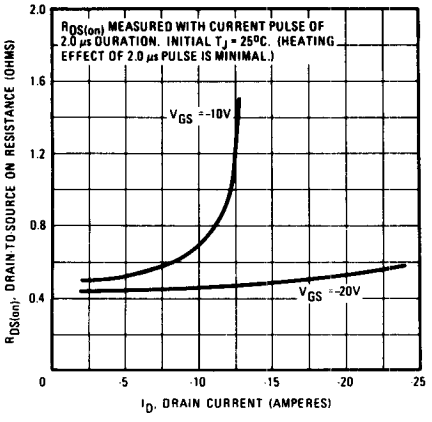


Fig. 12 - Typical on-resistance vs. drain current.

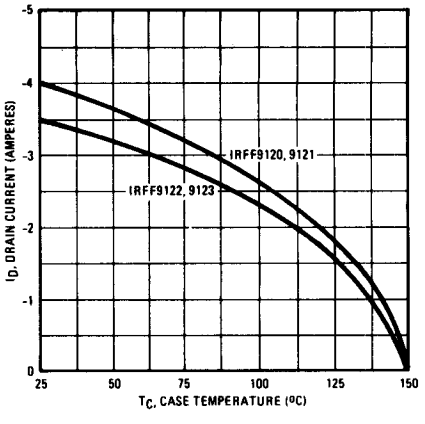


Fig. 13 - Maximum drain current vs. case temperature.

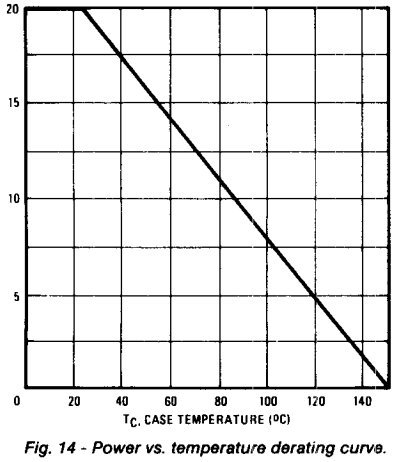


Fig. 14 - Power vs. temperature derating curve.

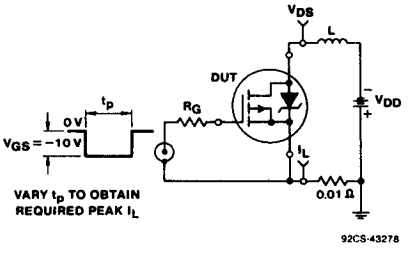


Fig. 15 - Unclamped inductive test circuit.

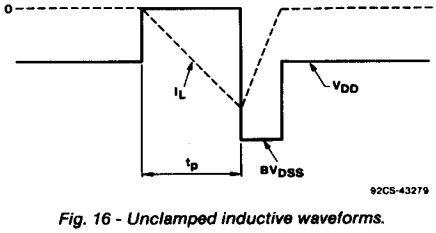


Fig. 16 - Unclamped inductive waveforms.

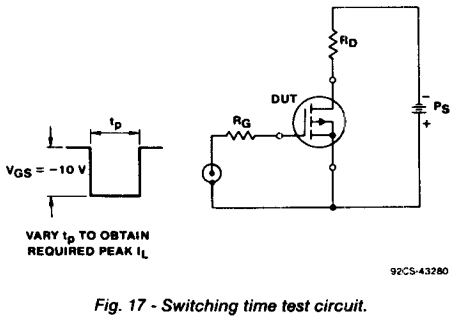


Fig. 17 - Switching time test circuit.

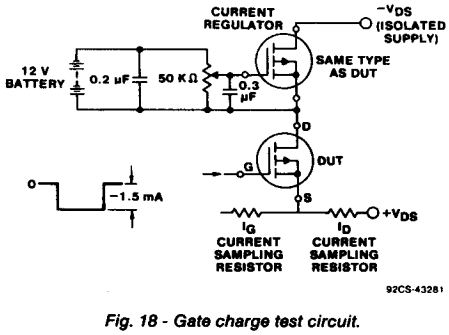


Fig. 18 - Gate charge test circuit.