12-Bit Successive-Approximation Integrated Circuit ADC

ADADC80

FEATURES

True 12-bit operation: maximum nonlinearity ±0.012%
Low gain temperature coefficient (TC): ±30 ppm/°C maximum
Low power: 800 mW
Fast conversion time: 25 µs
Precision 6.3 V reference for external application
Short-cycle capability
Parallel data output
Monolithic DAC with scaling resistors for stability
Low chip count, high reliability
Industry-standard pin configuration
"Z" models for ±12 V supplies

FUNCTIONAL BLOCK DIAGRAM

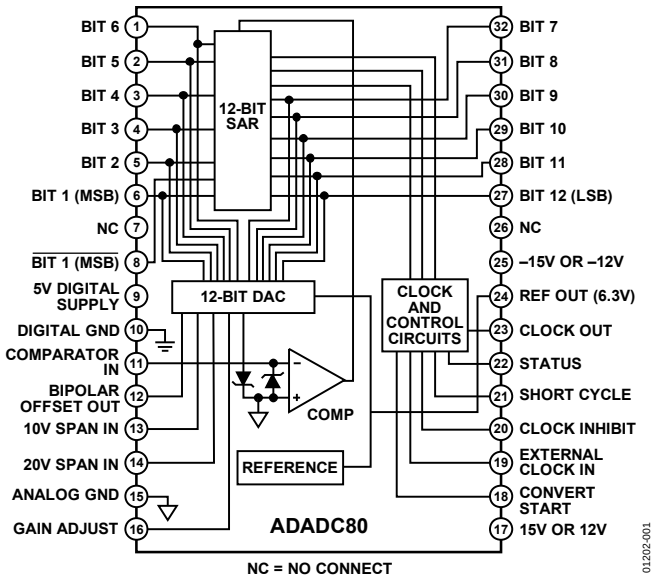

Figure 1.

PRODUCT DESCRIPTION

The ADADC80[1] is a complete 12-bit successive-approximation analog-to-digital converter (ADC) that includes an internal clock, reference, and comparator. Its hybrid IC design uses MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic digital-to-analog converter (DAC) to provide modular performance and versatility with IC size, price, and reliability.

Important performance characteristics of the ADADC80 include a maximum linearity error of ±0.012% at 25°C, maximum gain TC of 30 ppm/°C, typical power dissipation of 800 mW, and maximum conversion time of 25 µs. Monotonic operation of the feedback DAC guarantees no missing codes over the temperature range of −25°C to +85°C.

The design of the ADADC80 includes scaling resistors that provide an analog signal range of ±2.5 V, ±5.0 V, ±10 V, 0 V to +5.0 V, or 0 V to +10.0 V. The 6.3 V precision reference can be used for external applications. All digital signals are fully DTL and TTL compatible; output data is in parallel form.

The ADADC80 is available in grades specified for use over the −25°C to +85°C temperature range and is available in a 32-lead ceramic DIP.

PRODUCT HIGHLIGHTS

1. The ADADC80 is a complete 12-bit ADC. No external components are required to perform a conversion.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The internal buried Zener reference is laser trimmed to 6.3 V. The reference voltage is available externally and can supply up to 1.5 mA beyond the current required for the reference and bipolar offset.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. The ADADC80 directly replaces other devices of this type, providing significant increases in performance.
6. The fast conversion rate of the ADADC80 makes it an excellent choice for applications requiring high system throughput rates.
7. The short cycle and external clock options are provided for applications requiring faster conversion speed or lower resolution.

[1] The serial output function is no longer supported on this product after Date Code 9616.

Rev. E

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COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADADC80: 12-Bit Successive Approximation Integrated Circuit A/D Converter Scanned Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- Military Part Cross-Reference Guide
- Military Products by Function
- Military Products by GENERIC Part Number
- SMD to Generic Cross Reference

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- ADADC80 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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Pin 7 Changed to NC ..... Universal
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SPECIFICATIONS

Typical @ 25°C, ±15 V, and +5 V, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION		12		Bits
ANALOG INPUTS				
Voltage Ranges				
Bipolar		±2.5 or ±5 or ±10		V
Unipolar		0 to +5 or 0 to +10		V
Impedance (Direct Input)				
0 to +5, ±2.5 V		2.5		kΩ
0 to +10, ±5 V		5		kΩ
±10 V		10		kΩ
DIGITAL INPUTS[1]				
Positive Pulse During Conversion (CONVERT START)	100			ns
Logic Loading		1		TTL load
External Clock (EXTERNAL CLOCK IN)		1		TTL load
TRANSFER CHARACTERISTICS ERROR				
Gain Error[2]		±0.1		% of FSR[3]
Offset[2]				
Bipolar		±0.1		% of FSR
Unipolar		±0.05		% of FSR
Linearity Error[4]			±0.012	% of FSR
Inherent Quantization Error		±½		LSB
Differential Linearity Error		±½		LSB
No Missing Codes Temperature Range	−25		+85	°C
Power Supply Sensitivity				
±15 V		±0.0030		% of FSR/% V_S
+5 V		±0.0015		% of FSR/% V_S
DRIFT				
Specification Temperature Range[5]	−25		+85	°C
Gain			±30	ppm/°C
Offset				
Bipolar			±15	ppm of FSR/°C
Unipolar		±3		ppm of FSR/°C
Linearity			±3	ppm of FSR/°C
Monotonicity		Guaranteed		
CONVERSION SPEED[6]	17	22	25	µs
DIGITAL OUTPUTS (ALL CODES COMPLEMENTARY)				
Parallel, BIT 1 (MSB) to BIT 12 (LSB)				
Output Codes[7]				
Bipolar		COB, CTC		
Unipolar		CSB		
Output Drive		2		TTL loads
Status (STATUS)		Logic 1 during conversion		
Status Output Drive		2		TTL loads
Internal Clock (CLOCK OUT)				
Clock Output Drive		2		TTL loads
Frequency[8]		575		kHz

Parameter	Min	Typ	Max	Unit
INTERNAL REFERENCE VOLTAGE				
+6.3 V		±10		± mV
Maximum External Current				
(With No Degradation of Specifications)		1.5		mA
Temperature Coefficient of Drift[5]		±10	±20	ppm/°C
POWER REQUIREMENTS				
Rated Voltages		±15, +5		V
Range for Rated Accuracy[5]				
+5 V	+4.75		+5.25	V
±15 V	±14.0		±16.0	V
"Z" Models[5, 9]				
+5 V	+4.75		+5.25	V
±15 V	±11.4		±16.0	V
Supply Drain				
+15 V		+10		mA
−15 V		−20		mA
+5 V		+70		mA
TEMPERATURE RANGE				
Specification	−25		+85	°C
Operating (Derated Specifications)	−55		+100	°C
Storage	−55		+125	°C

[1] DTL/TTL compatible, that is, Logic 0 = 0.8 V maximum and Logic 1 = 2.0 V minimum for digital inputs, Logic 0 = 0.4 V maximum and Logic 1 = 2.4 V minimum for digital outputs.
[2] Adjustable to zero with external trimpots.
[3] FSR means full-scale range, that is, unit connected for ±10 V range has +20 V FSR.
[4] Error shown is the same as ±½ LSB maximum for resolution of analog-to-digital converter.
[5] Guaranteed by design. Not production tested.
[6] Conversion time with internal clock.
[7] See Table 4. Complementary offset binary is COB, complementary straight binary is CSB, and complementary twos complement is CTC.
[8] For conversion speeds specified.
[9] For "Z" models, order ADADC80-Z-12.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Logic Supply Voltage	7 V
Analog Ground to Digital Ground	±0.3 V
Analog Inputs (Pin 13, Pin 14)	$\pm V_S$
Digital Input	−0.3 V to V_{DD} + 0.3 V
Junction Temperature	175°C
Storage Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

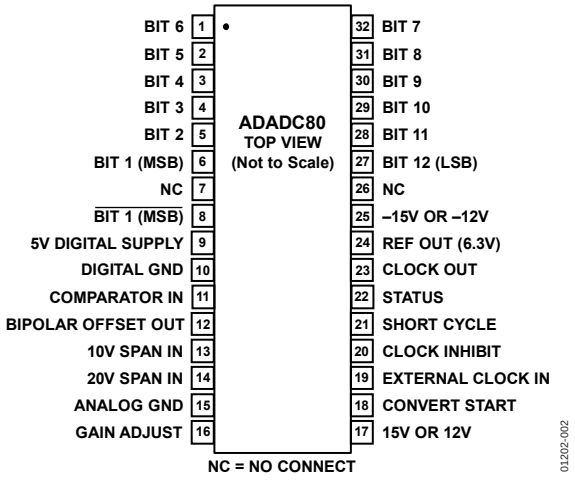


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1 to 6	BIT 6 to BIT 1 (MSB)	Digital Outputs.
7	NC	No Connection.
8	$\overline{\text{BIT 1 (MSB)}}$	$\overline{\text{MSB}}$ Inverted Digital Output.
9	5V DIGITAL SUPPLY	Digital Positive Supply (Nominally ±0.25 V).
10	DIGITAL GND	Digital Ground.
11	COMPARATOR IN	Offset Adjust.
12	BIPOLAR OFFSET OUT	Bipolar Offset Output.
13	10V SPAN IN	Analog Input 10 V Signal Range.
14	20V SPAN IN	Analog Input 20 V Signal Range.
15	ANALOG GND	Analog Ground.
16	GAIN ADJUST	Gain Adjust.
17	15V OR 12V	Analog Positive Supply (Nominally ±1.0 V for +15 V or ±0.6 V for +12 V).
18	CONVERT START	Enables Conversion.
19	EXTERNAL CLOCK IN	External Clock Input.
20	CLOCK INHIBIT	Clock Inhibit.
21	SHORT CYCLE	Shortens Conversion Cycle to Desired Resolution.
22	STATUS	Logic High, ADC Converting/Logic Low, ADC Data Valid.
23	CLOCK OUT	Internal Clock Output.
24	REF OUT (6.3V)	6.3 V Reference Output.
25	−15V OR −12V	Analog Negative Supply (Nominally ±1.0 V for −15 V or ±0.6 V for −12 V).
26	NC	No Connection.
27 to 32	BIT 12 (LSB) to BIT 7	Digital Outputs.

TYPICAL PERFORMANCE CHARACTERISTICS

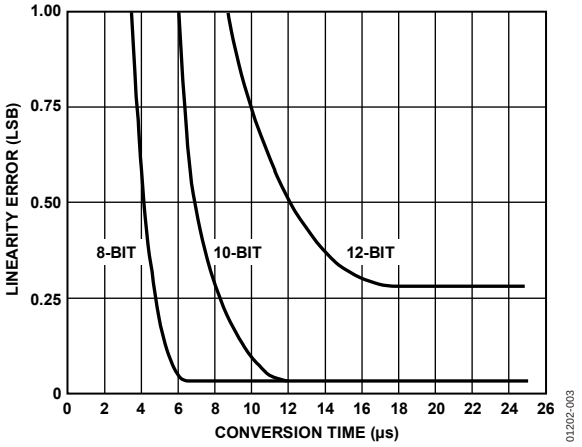


Figure 3. Linearity Error vs. Conversion Time (Normalized)

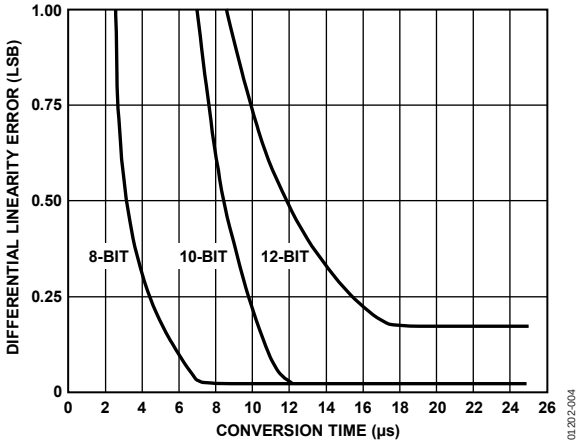


Figure 5. Differential Linearity Error vs. Conversion Time (Normalized)

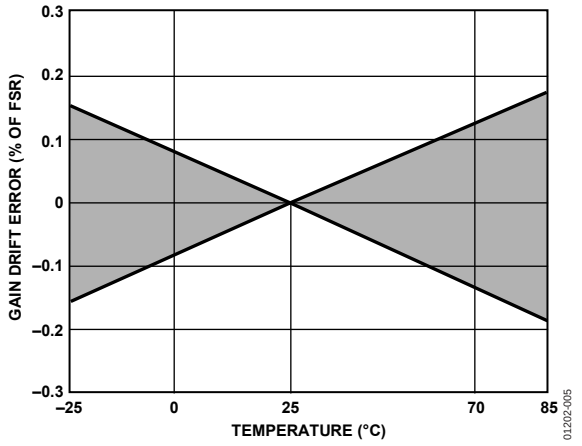


Figure 4. Gain Drift Error vs. Temperature

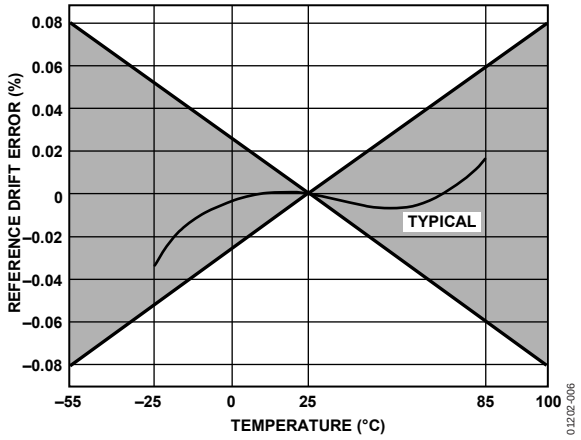


Figure 6. Reference Drift, Error vs. Temperature

THEORY OF OPERATION

Upon receipt of a CONVERT START command, the ADADC80 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows:

1. The 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC.
2. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last).
3. The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 7. Receipt of a CONVERT START signal sets the STATUS flag, indicating that a conversion is in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles.

All changes to the SAR parallel bit and to the STATUS bit are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, BIT 1 is reset and BIT 2 to BIT 12 are set unconditionally. At t_1, the BIT 1 decision is made (keep) and BIT 2 is unconditionally reset. At t_2, the BIT 2 decision is made (keep) and BIT 3 is reset unconditionally. This sequence continues until the BIT 12 (LSB) decision (keep) is made at t_{12}. After a 40 ns delay period, the STATUS flag is reset, indicating that the conversion is complete and the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic 0 state.

Parallel data bits become valid on the positive-going clock edge (see Figure 7).

Incorporation of this 40 ns delay guarantees that the parallel data is valid at the Logic l to Logic 0 transition of the STATUS flag, permitting a parallel data transfer to be initiated by the trailing edge of the STATUS signal.

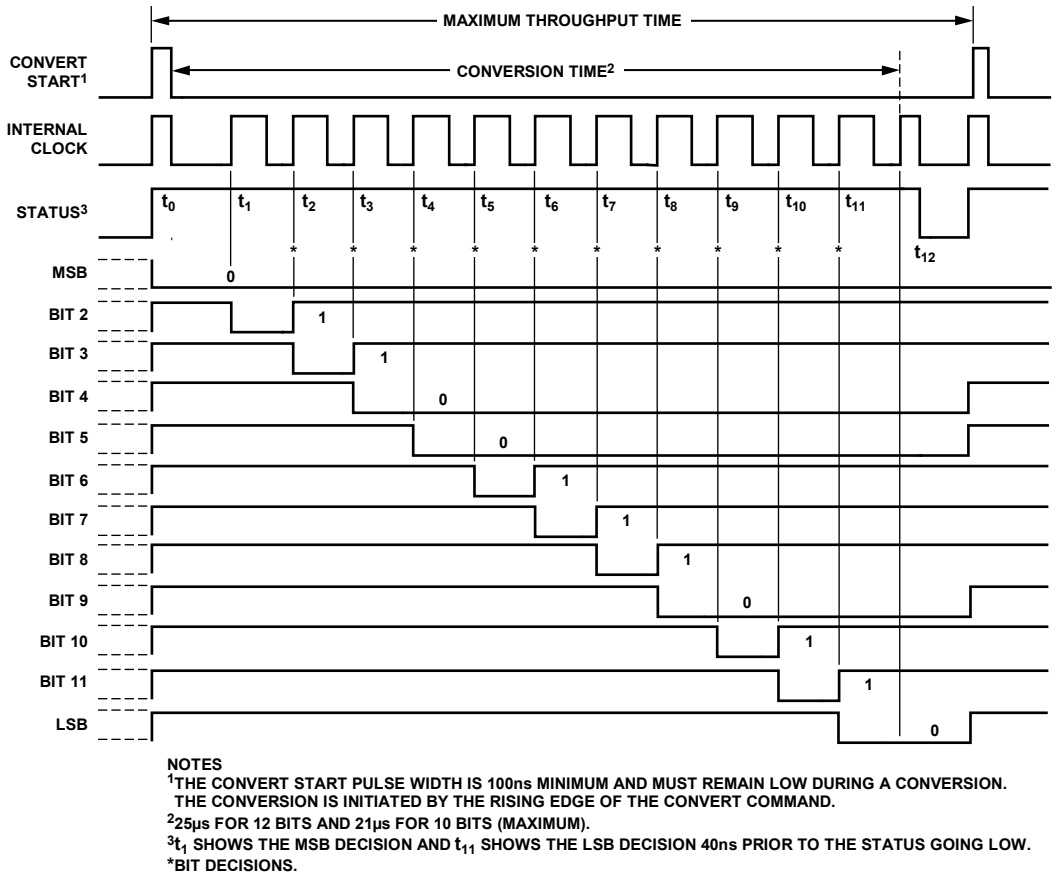


Figure 7. Timing Diagram (Binary Code 011001110110)

DIGITAL OUTPUT DATA

Parallel data from TTL storage registers is in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary twos complement binary for bipolar ranges, depending on whether BIT 1 (Pin 6) or its logical inverse BIT 1 (MSB) (Pin 8) is used as the MSB. Parallel data becomes valid approximately 40 ns before the STATUS flag returns to Logic 0, permitting parallel data transfer to be clocked on the 1 to 0 transition of the STATUS flag.

Parallel data outputs change state on positive-going clock edges. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 7. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge.

SHORT CYCLE Input

The SHORT CYCLE input (Pin 21) permits the timing cycle shown in Figure 7 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 10-bit resolution is desired, Pin 21 is connected to the BIT 11 output (Pin 28). The conversion cycle then terminates, and the STATUS flag resets after the BIT 10 decision (t_{10} + 40 ns in timing diagram of Figure 7). Short cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times are summarized in Table 4. When 12-bit resolution is required, SHORT CYCLE (Pin 21) is connected to 5V DIGITAL SUPPLY (Pin 9).

INPUT SCALING

The ADADC80 input should be scaled as close to the maximum input signal range as possible to use the maximum signal resolution of the ADC. Connect the input signal as shown in Table 5. See Figure 8 for circuit details.

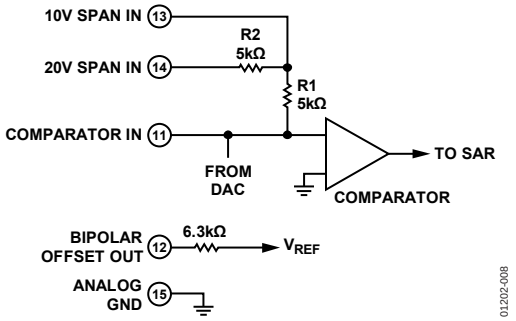


Figure 8. Input Scaling Circuit

Table 4. Short Cycle Connections

Connect SHORT CYCLE (Pin 21) to	Resolution (Bits)	(% FSR)	Maximum Conversion Time (µs)	STATUS Flag Reset
5V DIGITAL SUPPLY (Pin 9)	12	0.024	25	t_{12} + 40 ns
BIT 11 (Pin 28)	10	0.100	21	t_{10} + 40 ns
BIT 9 (Pin 30)	8	0.390	17	t_8 + 40 ns

Table 5. Input Scaling Connections

Input Signal Range	Output Code	Connect BIPOLAR OFFSET OUT (Pin 12) to	Connect 20V SPAN IN (Pin 14) to	Connect Input Signal to
±10 V	COB or CTC	COMPARATOR IN (Pin 11)	Input Signal	20V SPAN IN (Pin 14)
±5 V	COB or CTC	COMPARATOR IN (Pin 11)	Open	10V SPAN IN (Pin 13)
±2.5 V	COB or CTC	COMPARATOR IN (Pin 11)	COMPARATOR IN (Pin 11)	10V SPAN IN (Pin 13)
0 V to +5 V	CSB	ANALOG GND (Pin 15)	COMPARATOR IN (Pin 11)	10V SPAN IN (Pin 13)
0 V to +10 V	CSB	ANALOG GND (Pin 15)	Open	10V SPAN IN (Pin 13)

Table 6. Input Voltage Range and LSB Values

Binary Output Analog Input Voltage Range	Defined as	±10 V	±5 V	±2.5 V	0 V to +10 V	0 V to +5 V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	FSR 2^n n = 8 n = 10 n = 12	20 V 2^n 78.13 mV 19.53 mV 4.88 mV	10 V 2^n 39.06 mV 9.77 mV 2.44 mV	5 V 2^n 19.53 mV 4.88 mV 1.22 mV	10 V 2^n 39.06 mV 9.77 mV 2.44 mV	5 V 2^n 19.53 mV 4.88 mV 1.22 mV
Transition Values **MSB LSB**						
000. . . 000[4]	+Full scale	10 V − 3/2 LSB	5 V − 3/2 LSB	2.5 V − 3/2 LSB	10 V − 3/2 LSB	5 V − 3/2 LSB
011. . . 111	Midscale	0	0	0	5 V	2.5 V
111. . . 110	−Full scale	−10 V + 1/2 LSB	−5 V + 1/2 LSB	−2.5 V + 1/2 LSB	0 V + 1/2 LSB	0 V + 1/2 LSB

[1] COB = complementary offset binary.
[2] CTC = complementary twos complement; obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on Pin 8.
[3] CSB = complementary straight binary.
[4] Voltages given are the nominal value for transition to the code specified.

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8 MΩ resistor to COMPARATOR IN (Pin 11) for all ranges. As shown in Figure 9, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor with a −1200 ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ ppm/°C = 2.3 ppm/°C of FSR if the offset adjustment potentiometer is set at either end of its adjustment range. Because the maximum offset adjustment required is typically no more than ±4 LSB, use of a carbon composition offset summing resistor typically contributes no more than 1 ppm/°C of FSR offset tempco.

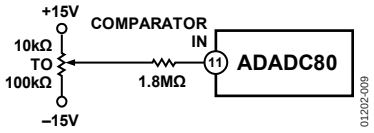


Figure 9. Offset Adjustment Circuit

An alternative offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco < 100 ppm/°C) are used, is shown in Figure 10. Note that the abbreviation MF in Figure 10 and Figure 12 refer to metal film resistors.

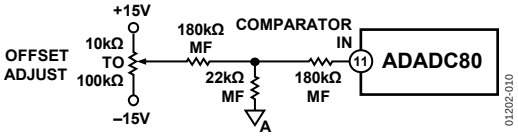


Figure 10. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to COMPARATOR IN (Pin 11) should be located close to this pin to keep the pin connection runs short. Pin 11 is quite sensitive to external noise pickup.

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10 MΩ resistor to the GAIN ADJUST (Pin 16), as shown in Figure 11.

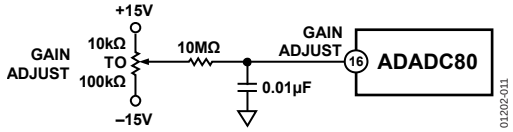


Figure 11. Gain Adjustment Circuit

An alternative gain adjust circuit, which contributes negligible gain tempco if metal film resistors (tempco < 100 ppm/°C) are used, is shown in Figure 12.

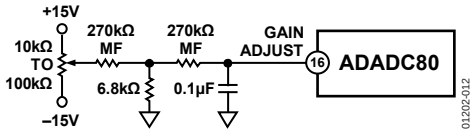


Figure 12. Low Tempco Gain Adjustment Circuit

CALIBRATION

External zero adjustment and gain adjustment potentiometers, connected as shown in Figure 13 and Figure 14, are used for device calibration. To prevent interaction of these two adjustments, zero is always adjusted first and gain second. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 V to 10 V Range

Set analog input to +1 LSB = 0.0024 V; adjust zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR − 2 LSB = 9.9952 V; adjust gain for 000000000001 digital output code. Full-scale gain is now calibrated. For half-scale calibration check, set analog input to 5.0000 V; digital output code should be 011111111111.

−10 V to +10 V Range

Set analog input to −9.9951 V; adjust zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902 V; adjust gain for 000000000001 digital output (complementary offset binary) code. For half-scale calibration check, set analog input to 0.0000 V; digital output (complementary offset binary) code should be 011111111111.

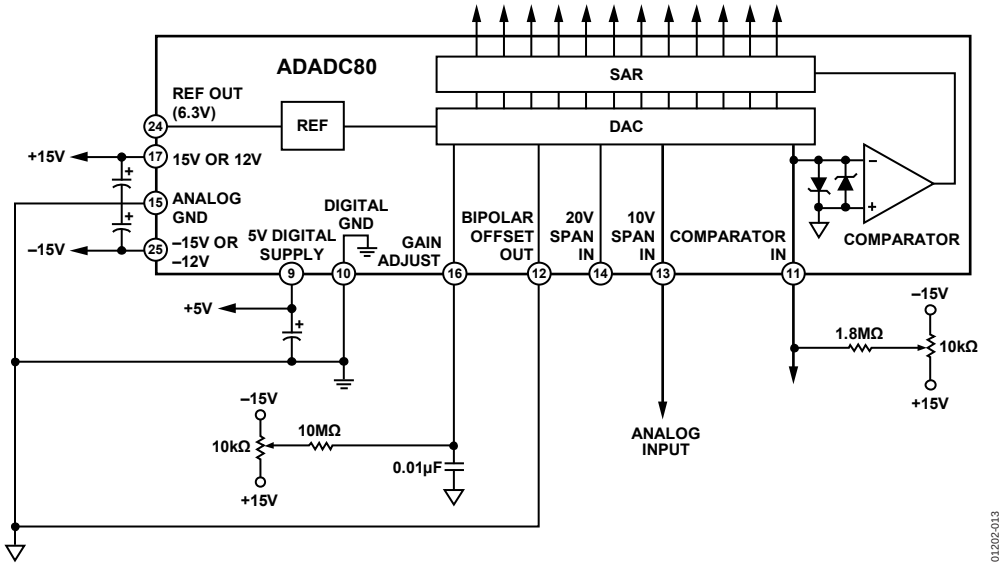


Figure 13. Analog and Power Connections for Unipolar 0 V to 10 V Input Range

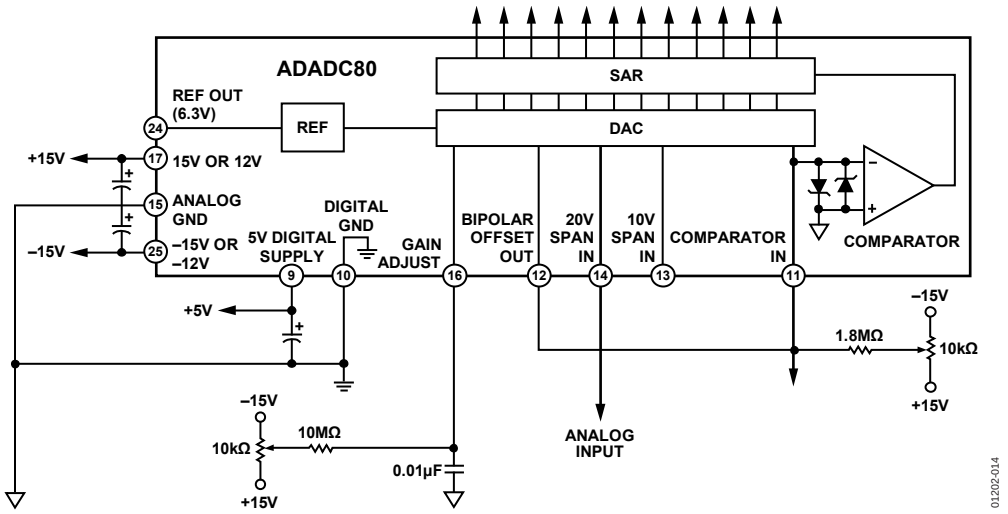


Figure 14. Analog and Power Connections for Bipolar ±10 V Input Range

Other Ranges

Coding relationships and calibration points for 0 V to +5 V, −2.5 V to +2.5 V, and −5 V to +5 V ranges can be found by halving the corresponding code equivalents listed for the 0 V to +10 V and −10 V to +10 V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4 LSB using the static adjustment procedure described previously. By summing a small sine- or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *A/D Conversion Notes*, D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 3.

GROUNDING

Many data-acquisition components have two or more ground pins that are not connected together within the device. These grounds are usually referred to as the logic power return, analog common (analog power return), and analog signal ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground is desirable. However, because current flows through the ground wires and etch stripes of the circuit cards, and because these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the ADADC80. Therefore, separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point, and the two device grounds should be tied together. In this way, supply currents and logic gate return currents are not summed into the same return path as analog signals, where they would cause measurement errors.

Each of the ADADC80 supply terminals should be capacitively decoupled as close to the ADADC80 as possible. A large value capacitor, such as 1 µF in parallel with a 0.1 µF capacitor, is usually sufficient. Analog supplies are bypassed to the analog power return pin, and the logic supply is bypassed to the logic power return pin.

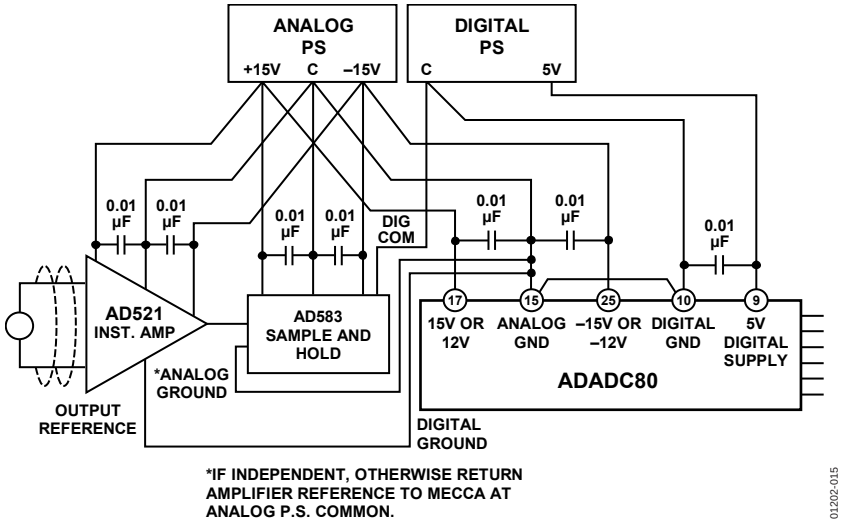


Figure 15. Basic Grounding Practice

CONTROL MODES

The timing sequence of the ADADC80 allows the device to be easily operated in a variety of systems with different control modes. The most common control modes are illustrated in Figure 16, Figure 17, and Figure 18.

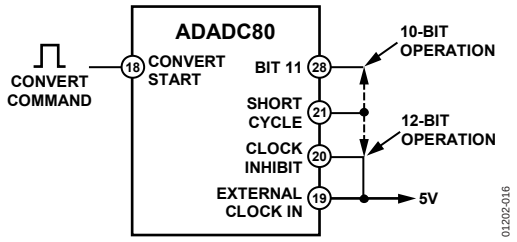


Figure 16. Internal Clock—Normal Operating Mode, Conversion Initiated by the Rising Edge of Convert Command (Internal Clock Runs Only During Conversion)

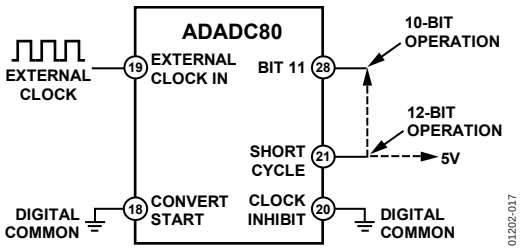


Figure 17. Continuation Conversion with External Clock Conversion Initiated by 14th Clock Pulse (Clock Runs Continuously)

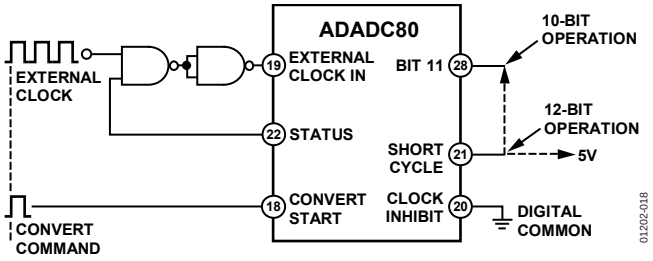
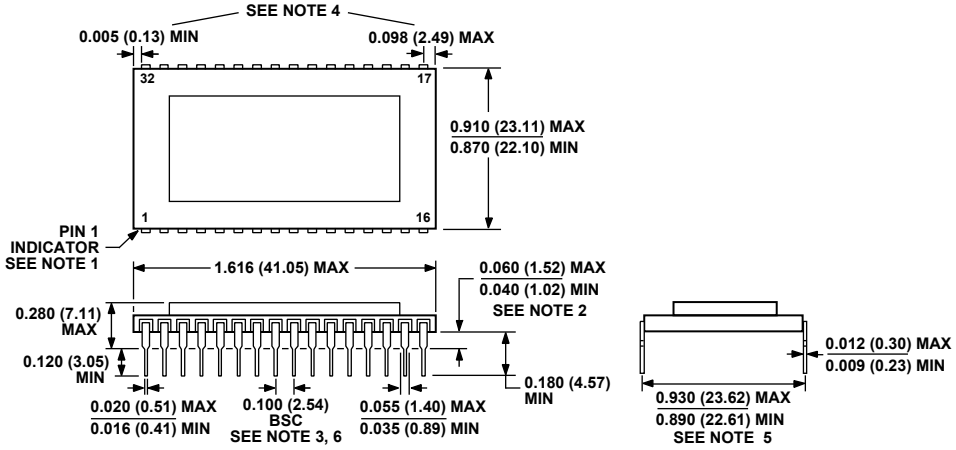


Figure 18. Continuous External Clock Conversion Initiated by Rising Edge of Convert Command (Convert Command Must Be Synchronized with Clock)

OUTLINE DIMENSIONS



NOTES:
1. INDEX AREA; A NOTCH OR A LEAD ONE IDENTIFICATION MARK IS LOCATED ADJACENT TO LEAD ONE.
2. DIMENSION SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. THE BASIC PIN SPACING IS 0.100" (2.54 mm) BETWEEN CENTERLINES.
4. APPLIES TO ALL FOUR CORNERS.
5. THE DIMENSION SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS.
6. THIRTY SPACES.
7. CONTROLLING DIMENSIONS ARE IN INCHES. MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 19. 32-Lead Side Brazed Ceramic DIP for Hybrid [SBDIP_H]
(DH-32D)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADADC80-12	−25°C to +85°C	32-Lead SBDIP_H	DH-32D
ADADC80-Z-12[1]	−25°C to +85°C	32-Lead SBDIP_H	DH-32D

[1] "Z "= Models for ±12 V supplies. This part is not RoHS compliant.

NOTES

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