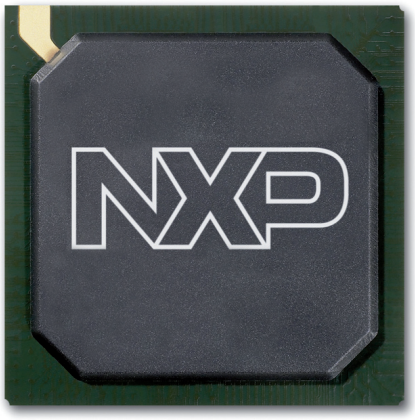


NXP MPEG-2 SD decoder CX24153/4/6

Highly integrated, cost efficient MPEG-2 SD decoder

NXP's interactive TV decoder products provide complete single IC system solutions for the core electronics of high performance set-top boxes (STB) deployed in digital satellite, cable or terrestrial TV networks.

Key features

- MPEG-2/DVB/DIRECTV® broadcast service decoder for worldwide markets
- Single IC STB solution with integrated NTSC Ch 3/4 RF modulator
- High-performance 32-bit 220 MIPS ARM920 CPU with 16KB I & D caches
- High-performance 2D graphics rendering acceleration
- Multiplane video/graphics compositing and display engine
- High-performance 16 or 32-bit unified memory controller architecture

The CX24153/4/6 IC family offers a high performance embedded 32-bit RISC CPU, a complete DVB/DIRECTV® broadcast service decoder system and advanced 2D graphics and display compositing performance. This combination enables consumer electronics manufacturers to build low-cost digital TV STBs to support a wide range of advanced, interactive, consumer services.

Advanced CPU and graphics performance

The CX24153/4/6's powerful ARM920 32-bit RISC processor and advanced video/graphics display controller provide a platform ideally suited to support advanced interactive middleware platforms including OpenTV, MHP, and Liberate. The embedded processor offers up to 224 Dhrystone 2.1 MIPS at a 200MHz clock speed. This CPU platform represents a major advance in capability for the low cost STB category and will enable complex, MIPS hungry, feature rich middleware platforms such as Multimedia Home Platform (MHP) to be adopted by broadcasters for low cost STBs.

NXP founded by Philips

The advanced CPU platform delivers performance that can be deployed by STB manufacturers in a variety of ways including improved interactive application loading and EPG scrolling performance, H/W feature differentiation via multimedia host signal processing and scalability to Linux based S/W platforms via MMU H/W support. A powerful video/graphics display compositing engine supports up to five independent image planes to enable the rich visual interface required for simultaneous TV viewing and application interaction. NXP's 2D graphics rendering engine can composite an unlimited number of graphics planes with transparency into a single displayable OSD plane. Additionally, the CX24153/4/6 provides ample CPU processing power to support implementation of a complete, low-speed modem datapump and controller in software.

NXP's interactive TV decoders feature an innovative, unified memory architecture that reduces memory costs by servicing all system requirements in a single x16 SDRAM IC. System hardware costs are further minimized by implementing analog modem return path functionality in software running on the ARM920 CPU. Additional contributions to system bill-of-materials cost reductions come from an integrated NTSC channel 3/4 RF modulator, integrated VCXO and system clock generation and an integrated DVB Common Interface Module Controller.

Common platform for satellite, cable, and terrestrial

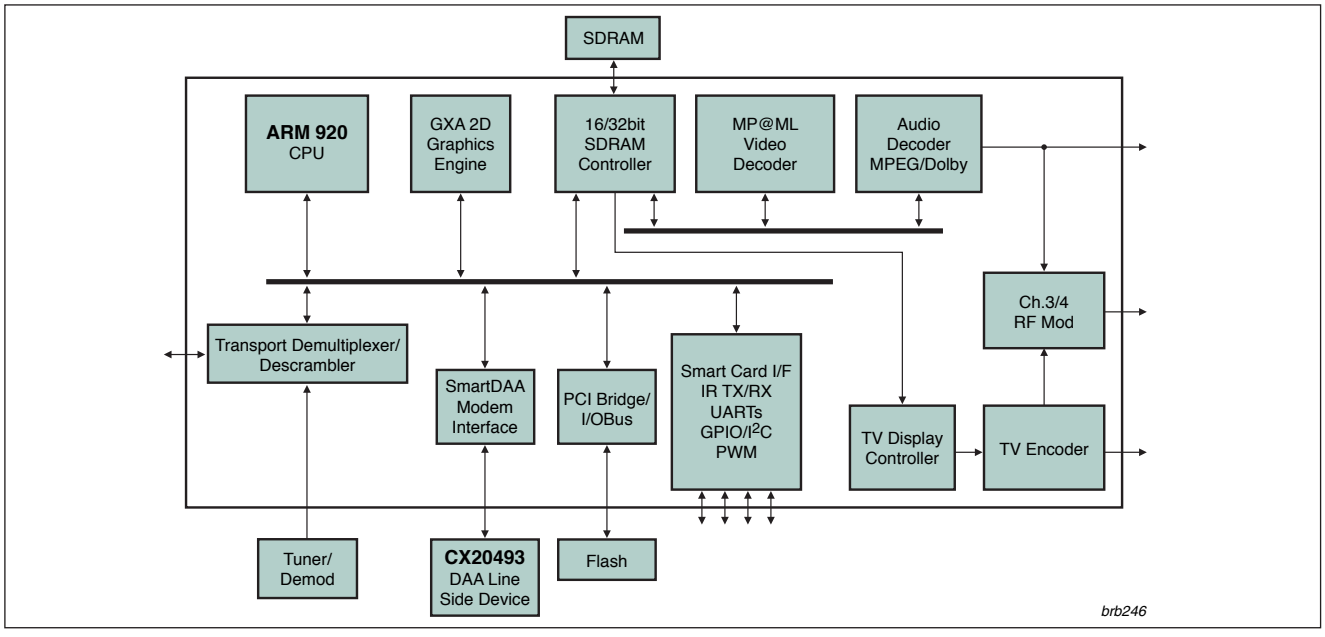
STB manufacturers increasingly look to leverage a common hardware platform that can be reused over various broadband networks including satellite, cable, terrestrial, DSL and Ethernet IP networks. NXP's CX24153/4/6 IC's can serve as a common back-end platform that easily interfaces to a variety of broadband front-ends, including QPSK, QAM, OFDM, VSB, ADSL/VDSL, 802.3, 802.11a/b/g, or IEEE 1394 through either transport stream or PCI interface. This provides a flexible STB solution that can be targeted to a variety of broadband operators while minimizing hardware/software development costs.

NXP also offers a variety of pin compatible CX24153/4/6 options to target network configurations for DVB-MHP, DVB-C, DVB-T, Free-To-Air, and FTA-CI.

Full-featured development platform

The CX24153/4/6 IC family is integrated into a fully engineered interactive TV STB reference development system that implements third-party interactive middleware/RTOS platforms and provides complete STB functionality. The hardware platform comes equipped with fully integrated OpenTV, Alticast, Nucleus+, pSOS and VxWorks runtime libraries and driver software components. A mature and robust hardware abstraction layer is assured by re-use of core driver libraries developed on early generation ICs. The development platform set-top box hardware is designed with a two-layer PCB configuration and a variety of PSTN modem options.

A choice of two robust tool chain development environments are supported for code developers including the ADS 1.2 from ARM, Inc. and Tornado 2.2 from WindRiver Systems, Inc. NXP offers a complete development code solution that has been tightly integrated with both third party tool chain environments.



CX24153 Block Diagram

CX24153/4/6 part number & feature selection guide

The CX24153/4/6 IC family includes three primary part numbers defined by different functionality combinations.

Table 1

CX" Part #	Demod	DACs	RF Mod	Still Plane	DRAM	DVB-CI	PCI note 1
CX24153	no	6	yes	yes	16/32-bit	yes	yes
CX24154	no	4	yes	no	16-bit	no	no
CX24156	no	6	no	yes	16/32-bit	yes	yes

DVB-CI not available simultaneously with PCI

License based features and CPU speed grade configurations are designated using a part number suffix or dash number.

Table 2

CX24153-mn CX24154-mn CX24156-mn										
	"-1n"	"-2n"	"-3n"	"-4n"	"-5n"	"-6n"	"-7n"	"-8n"	"-9n"	"-0n"
Macrovision		✓		✓	reserved	reserved		✓		✓
Dolby Digital			✓	✓					✓	✓
200 MHz CPU	✓	✓	✓	✓						
160 MHz CPU							✓	✓	✓	✓

m = License based feature and/or CPU speed designator (0 thru 9)
n = Die revision (e.g. n=1 for die rev A, 2 for die rev B etc.)

CX24153/4/6 features

- MPEG-2 MP@ML video decoder supporting NTSC and PAL CCIR601 image resolution
- MPEG-1/MPEG-2 and Dolby Digital (AC-3) audio decoder
- MPEG-2/DVB transport stream demultiplexing
- NTSC channel 3/4 RF modulator
- NTSC/PAL/SECAM TV encoder supporting simultaneous CVBS, YC & RGB/YPrPb analog video output signals
- 3DES ciphering engine & integrated OTP memory for unique, IC security personalization
- On-chip boot ROM for secure STB software authentication
- Integrated DVB common descrambler & DES ECB descrambler
- NDS Videoguard conditional access hardware support
- 200 MHz 224 MIPS 32-bit ARM920 CPU with 16KB I & D caches and MMU
- Advanced 2D graphics rendering engine for alphablt, bitblt, textblt, line draw and color expansion acceleration
- Unified memory architecture supporting 16 or 32-bit SDRAM
- MPEG picture and still plane upscaling and downscaling
- Multiplane video/graphics image compositing with color key or 256-level alpha blending
- Video-picture-in-graphics with flexible picture size and aspect ratio
- Flicker filtering, aspect ratio conversion and hardware cursor
- 4/8/16-bit ARGB/A YCrCb graphics
- Integrated 32-bit 33 MHz PCI 2.1 bus bridge controller

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