

20MHz, 650mA, X-EMI™-Enabled Synchronous Step-Down Regulator

Features

- Patented X-EMI™ Inductor Technology
 - Enables Trace Inductors in PC Board Material
 - Excellent EMI Performance
- Efficiency up to 90%
- 19µA Quiescent Current under Very Light Loads
- Wide Input Voltage Range — 2.7V to 5.5V
- Adjustable Output Voltage Down to 1.0V
- Output DC Current — up to 650mA
- High Light-load Efficiency via Automatic PSAVE Mode
- Ultra-fast Transient Response — <1µs
- Temperature Range — -40 to +85°C
- Shutdown Current — 0.1µA (typical)
- Requires Tiny 220nH Inductor
- Requires Only 1µF of Output Capacitance
- External Switching Frequency Synchronization
- Protection Features Including
 - Over-Current Protection
 - Output Short-Circuit Protection
 - Thermal Shutdown Protection
- Offered in SOIC 8 Lead Package
- Lead-free, Halogen-free, and RoHS/WEEE Compliant
- AEC-Q100 Qualified Version Available

Applications

- HDTV, Set Top Boxes, Gaming Consoles
- POL Applications
- White Goods
- Automotive AEC-Q100 Qualified Applications

Typical Application Circuit

Description

The SC220/Q is a 20MHz X-EMI™(1)-enabled step-down regulator optimized for power low voltage rails from 2.7 to 5.5V input voltage. X-EMI™ inductor technology enables inductors to be drawn directly on the PC board. This technology meets or exceeds the EMI performance of chip inductors and eliminates the need for discrete inductors.

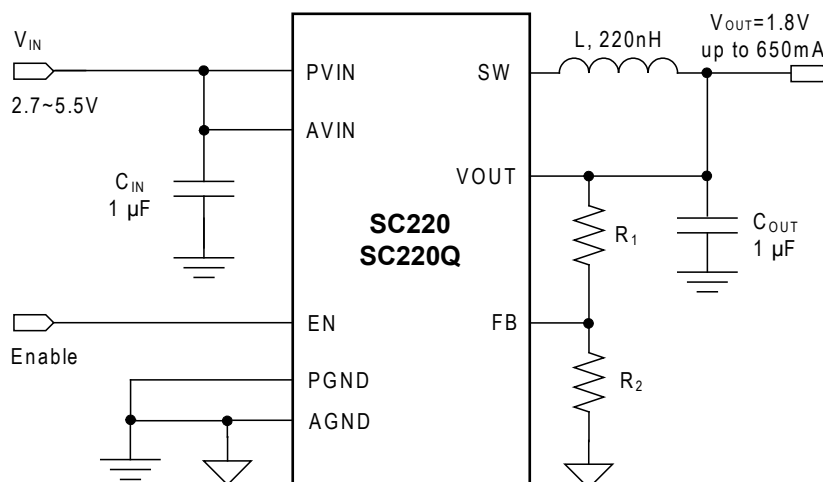
The SC220/Q uses a unique constant frequency, self-oscillating control loop architecture to provide excellent transient performance. Under light loads, the device operates in Power Save mode(PSAVE) maintaining a typical quiescent current of 19µA. At moderate to heavy loads, this part operates in PWM mode with a constant switching frequency of 20MHz. This high switching frequency offers the advantages of using small and low cost external components like a 1µF external capacitor and a small 220nH inductor (including X-EMI™ PCB trace inductors).

The device provides adjustable output voltages down to 1.0V and an output current up to 650mA. An EN pin can be used to synchronize to an external source and includes de-glitching to reduce noise sensitivity.

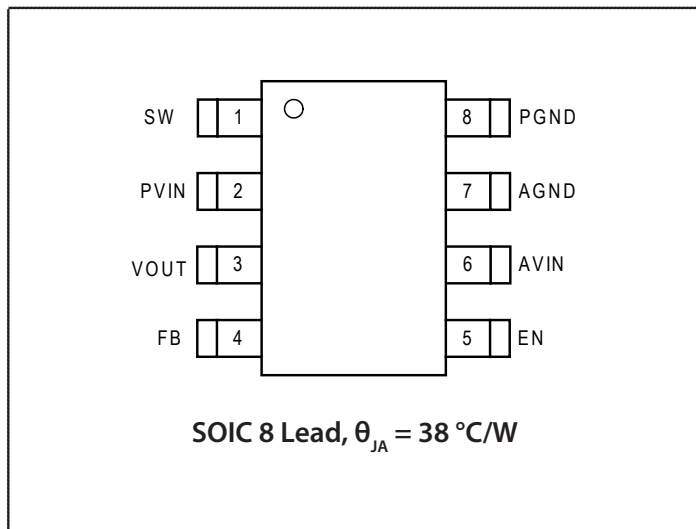
The SC220/Q is available in SOIC 8 lead package.

The SC220Q is an AEC-Q100 qualified version.

Note 1: Purchase of SC220/Q includes royalty-free right to use X-EMI™ inductor technology with no additional cost.



Pin Configuration



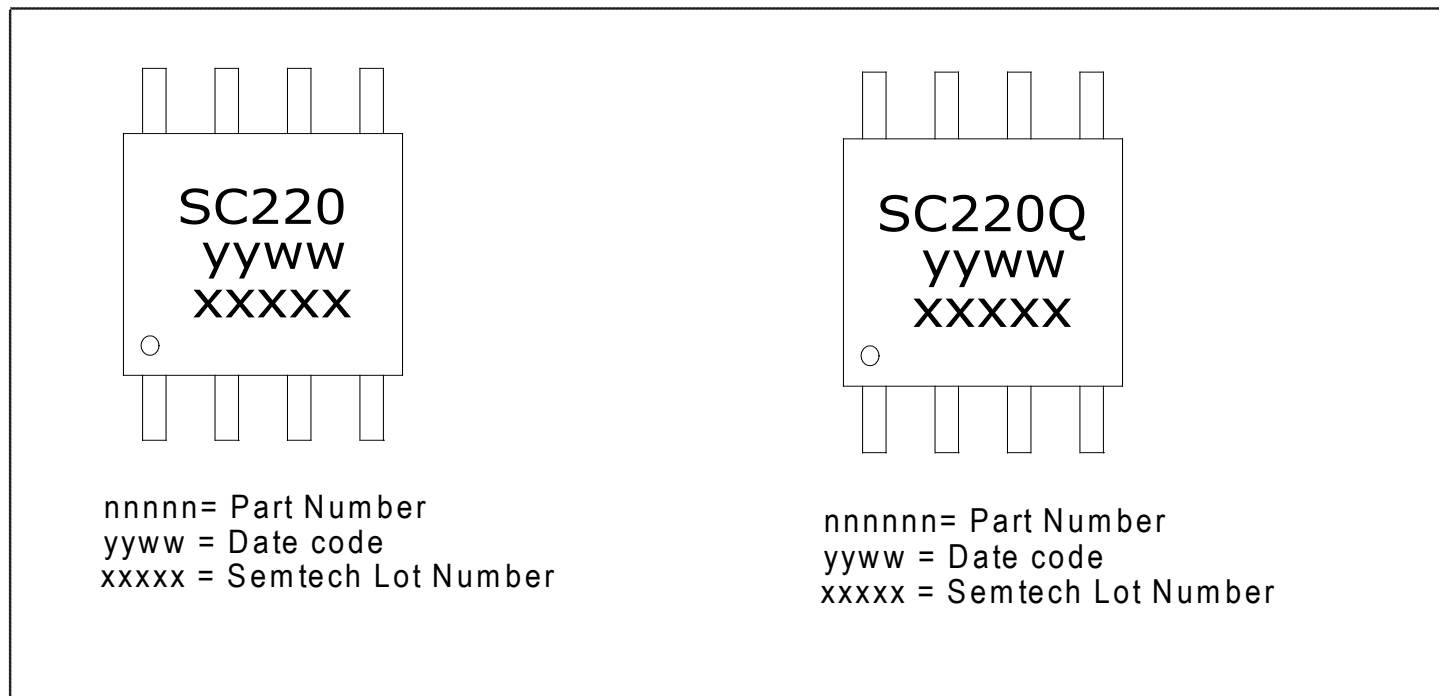
Ordering Information

Device	Package
SC220STRT ⁽¹⁾⁽²⁾	SOIC 8 Lead
SC220QSTRT ⁽¹⁾⁽²⁾⁽³⁾	SOIC 8 Lead
SC220EVB	Evaluation Board
SC220QEVB	Evaluation Board

Notes:

- (1) Available in tape and reel only. A reel contains 2,500 devices.
- (2) Device is lead-free, halogen-free, and RoHS/WEEE compliant.
- (3) Device is AEC-Q100 qualified.

Marking Information



Absolute Maximum Ratings

AVIN, PVIN (V).....	6.0
VOOUT, FB, EN, SW (V)	-0.3 to ($V_{IN} + 0.3$)
AGND (V)	-0.3 to +0.3
ESD Protection Level ⁽¹⁾ (kV)	3kV

Recommended Operating Conditions

Input Voltage Range (V)	+2.7 to +5.5
Output DC Current (mA).....	up to 650
Operating Temperature Range (°C)	-40 to +85

Thermal Information

Thermal Resistance, Junction to Ambient ⁽²⁾ (°C/W)....	38
Junction Temperature Range (°C)	-40 to +150
Storage Temperature Range (°C)	-65 to +150
Lead Temperature (soldering 10s (°C)	260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Notes:

- (1) All voltage values in this section are with respect to PGND pin voltage.
- (2) Tested according to JEDEC standard JESD22-A114-B.
- (3) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise specified: AVIN=PVIN = 3.6V, EN = AVIN = PVIN, $C_{IN}=C_{OUT}=1.0\mu F$, $L=220nH$. $T_A = 25^\circ C$ for typical values, $-40^\circ C < T_A = T_J < 85^\circ C$ for minimum and maximum values.

Parameter	Symbol	Condition	Min	Typ	Max	Units
POWER SUPPLY						
Input Voltage	V_{IN}		2.7		5.5	V
Input Quiescent Current	I_{VIN_Q}	No load, no switching		19	40	μA
Shutdown Current	I_{VIN_SD}	EN = 0V			1.0	μA
POWER SWITCH						
PMOS On Resistance				400		m Ω
NMOS On Resistance				360		m Ω
OSCILLATOR						
Switching Frequency	f_{OSC}	PWM Mode	16	20	24	MHz
REGULATION						
Output Voltage Tolerance ⁽¹⁾	V_{OUT_TOL}		-4.0		4.0	%
Current Limit	I_{LIMIT}		850		1300	mA
Soft-Start ⁽¹⁾	t_{SS}	EN pin low to high		40		μs
Feedback Voltage	V_{FB}	$2.7V \leq V_{IN} \leq 5.5V$	0.97	1.00	1.03	V

Electrical Characteristics (continued)

Unless otherwise specified: AVIN=PVIN = 3.6V, EN = AVIN = PVIN, $C_{IN}=C_{OUT}=1.0\mu F$, L=220nH. $T_A = 25^\circ C$ for typical values, $-40^\circ C < T_A = T_J < 85^\circ C$ for minimum and maximum values.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback Leakage Current	I_{FB}				1	μA
ENABLE						
EN Input High Voltage Threshold	V_{ENH}		1.2			V
EN Input "Low" Voltage Threshold	V_{ENL}				0.4	V
EN Input High Current	I_{ENH}	$V_{EN}=V_{IN}$	-1.0		1.0	μA
EN Input Low Current	I_{ENL}	$V_{EN}=AGND$	-1.0		1.0	μA
Minimum Synchronization Frequency	f_{SYN_MIN}	Square wave applied at EN pin			3	MHz
PROTECTION						
Over Temp Thermal Shutdown ⁽¹⁾	T_{OT}			150		$^\circ C$
Thermal Shutdown Hysteresis ⁽¹⁾	T_{HYST}			15		$^\circ C$

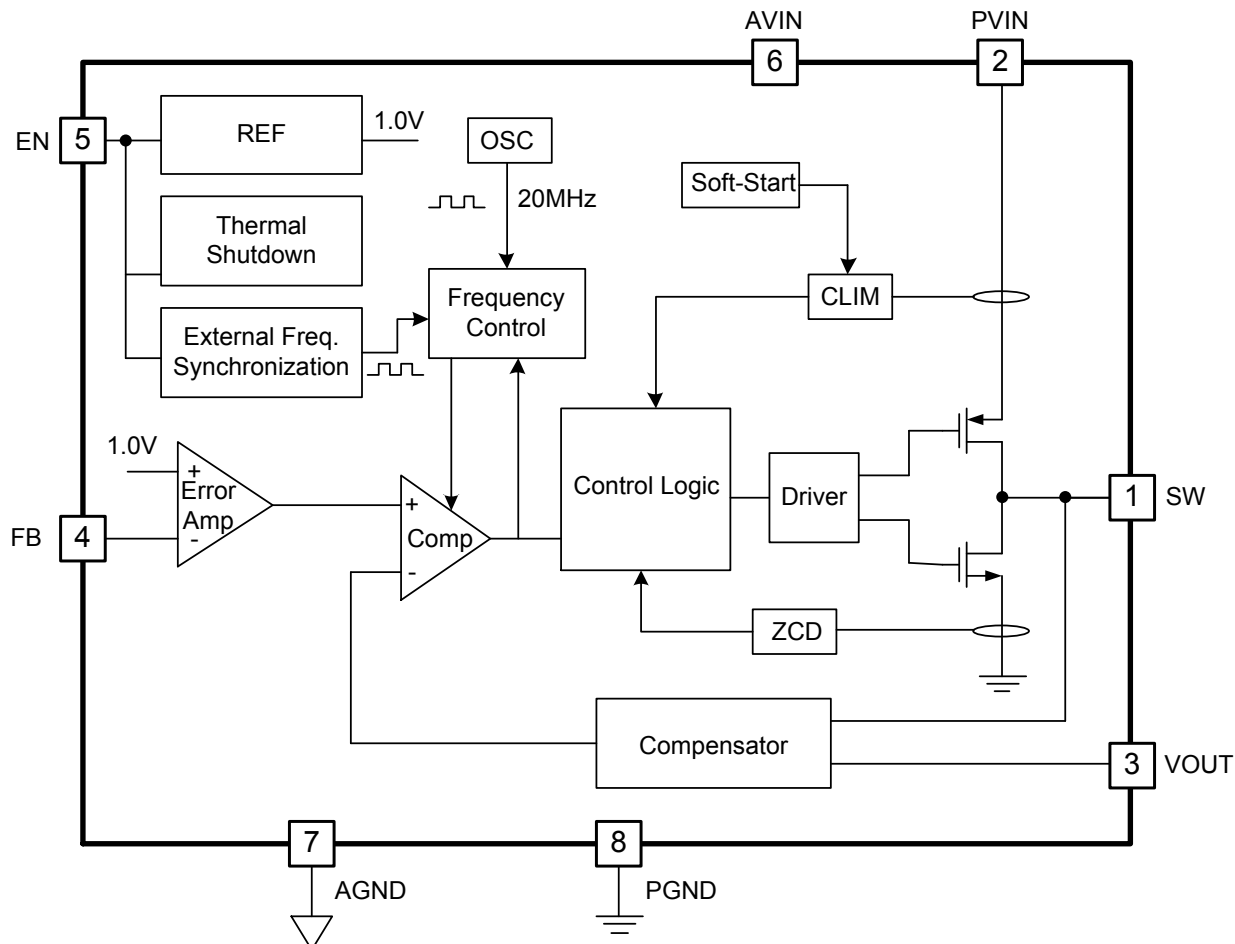
Notes

(1) Guaranteed by design. Not tested in production.

Pin Descriptions

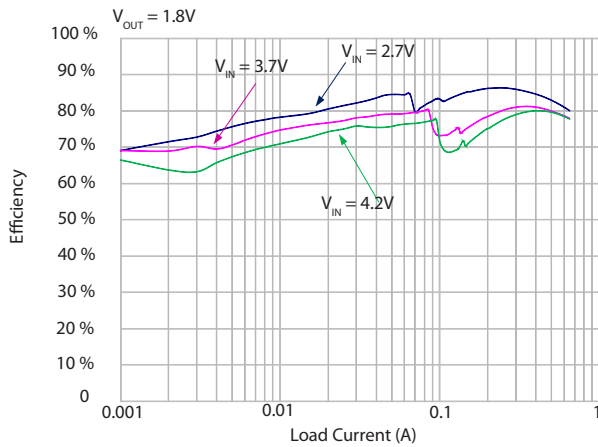
Pin #	Pin Name	Pin Function
1	SW	Switching output node — connect to the output LC filter.
2	PVIN	Power input supply voltage (2.7 to 5.5V).
3	VOUT	Input for sensing the output of LC filter.
4	FB	Input for regulation of output LC filter — Using R_1 and R_2 to set the output voltage, $V_{OUT} = V_{FB} \times (1 + R_1/R_2)$. (Please refer to the typical application circuit diagram on page 1).
5	EN	Enable Input — when low, circuit draws $<1\mu A$. Apply a square wave clock at EN to synchronize the switching frequency with an external clock. It is recommended that the externally applied clock frequency should not be above 20MHz.
6	AVIN	Input supply voltage
7	AGND	Analog ground
8	PGND	Power ground

Block Diagram

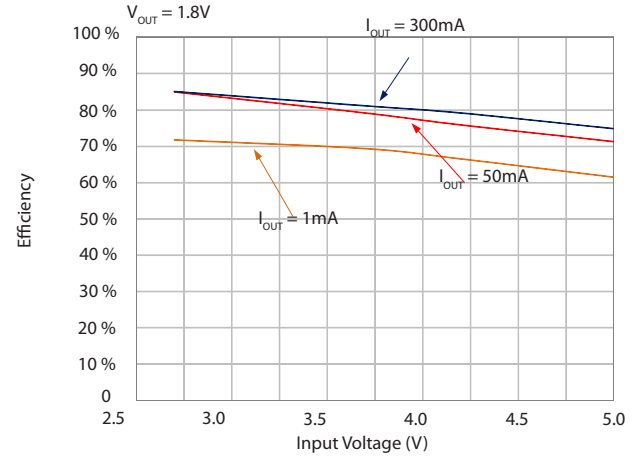


Typical Characteristics

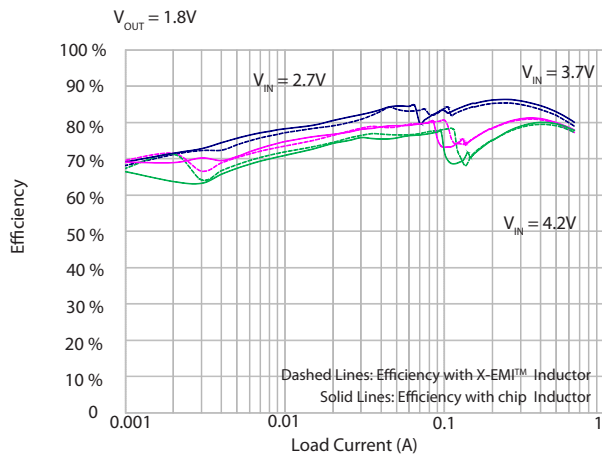
Efficiency vs. Load Current



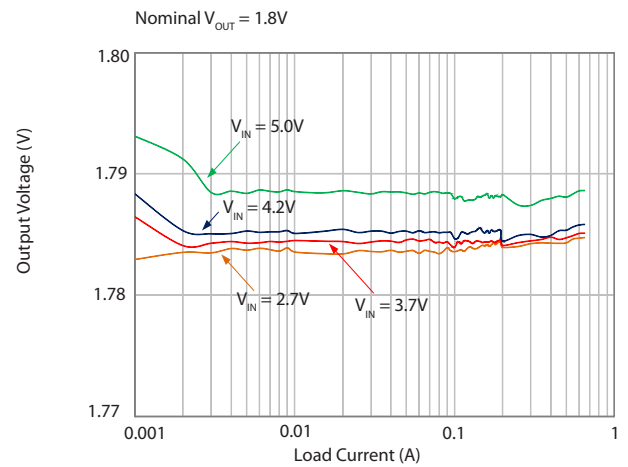
Efficiency vs. V_{IN}



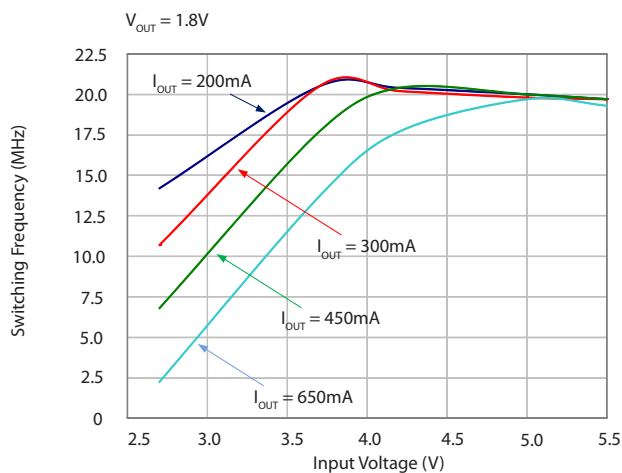
Efficiency vs. Load Current (Chip Inductor vs. X-EMI™ Inductor)



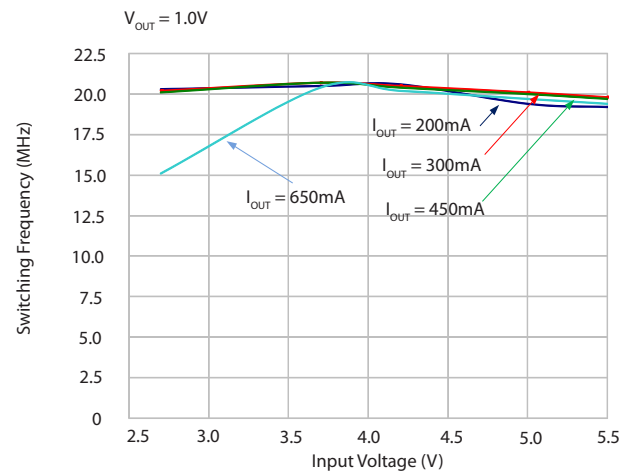
Load Regulation



Switching Frequency vs. V_{IN}

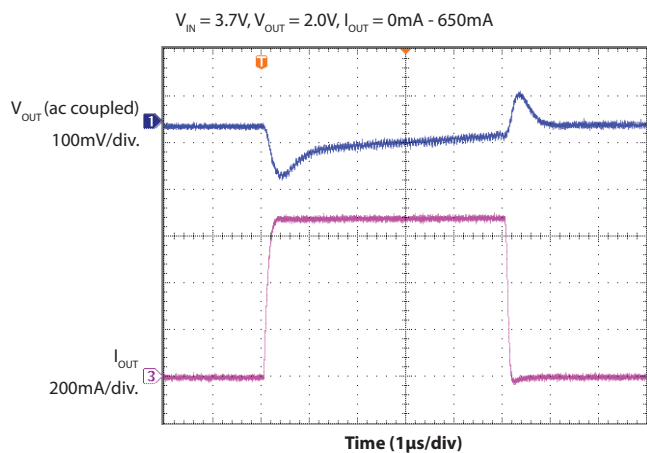


Switching Frequency vs. V_{IN}

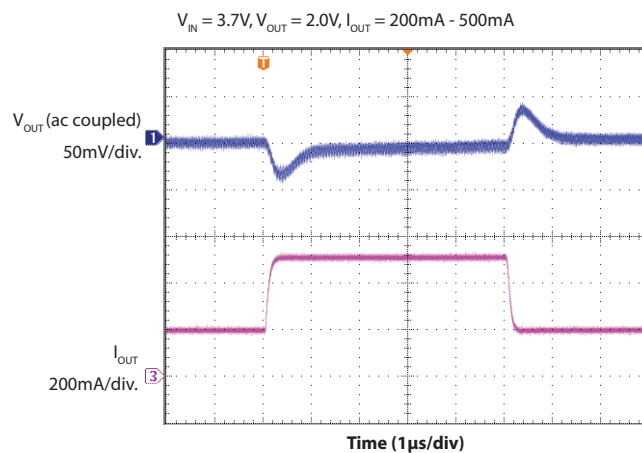


Typical Characteristics (Continuous)

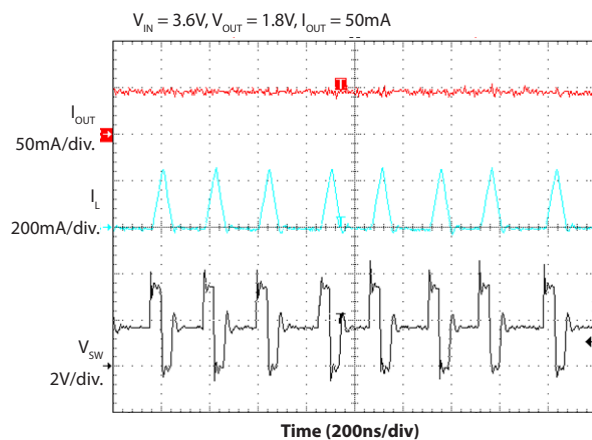
Load Transient Response



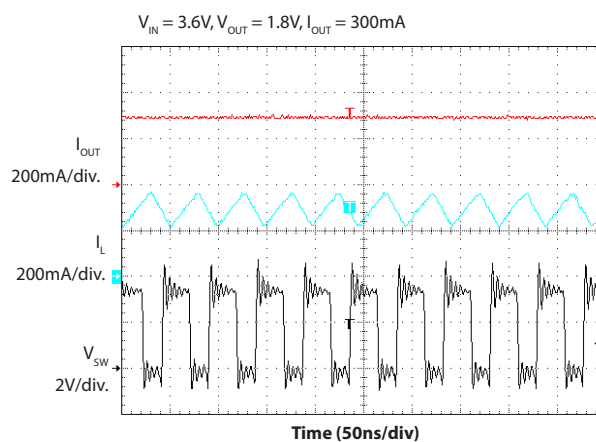
Load Transient Response



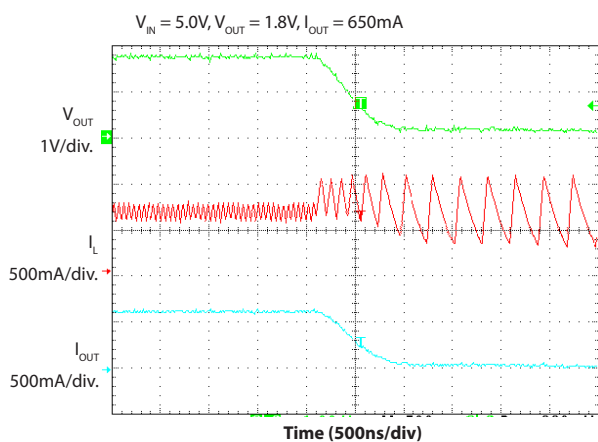
Steady State Operation ($I_{OUT} = 50mA$)



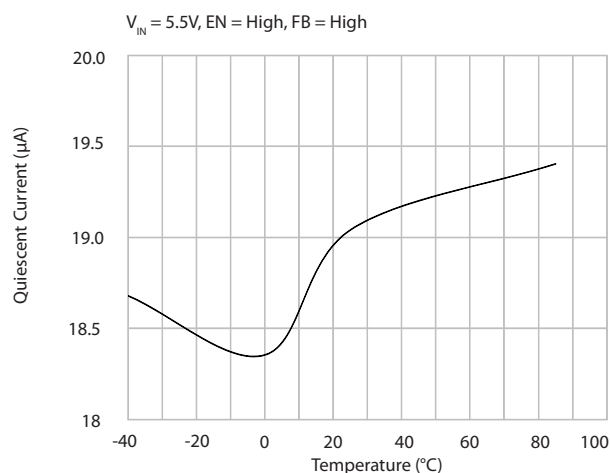
Steady State Operation ($I_{OUT} = 300mA$)



Output Hard Short

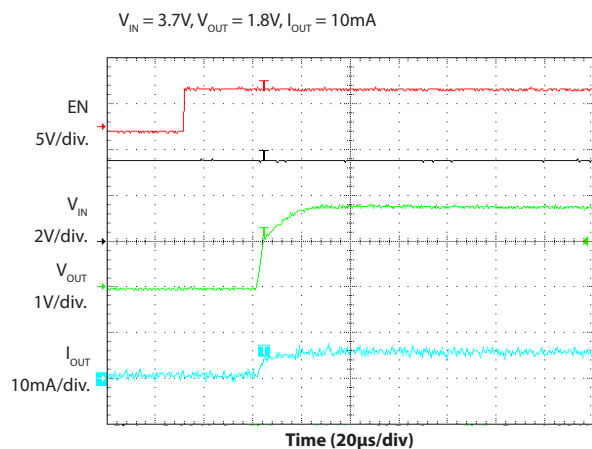


Input Quiescent Current vs. Temperature

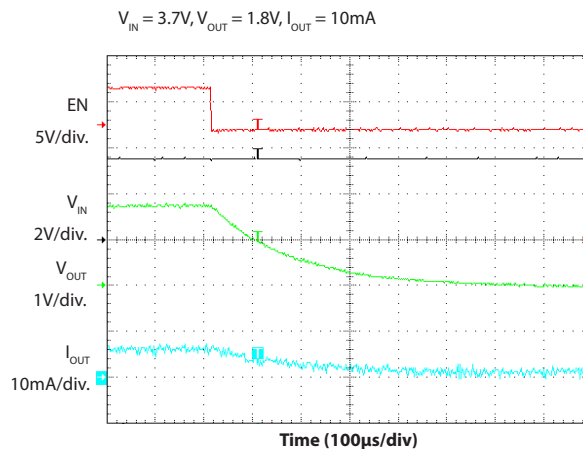


Typical Characteristics (Continuous)

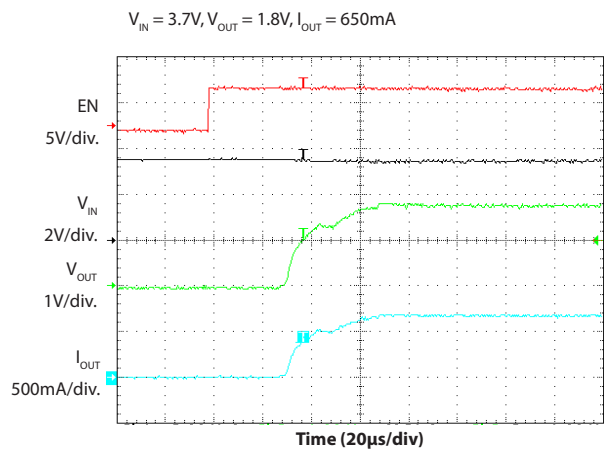
Start-up Operation



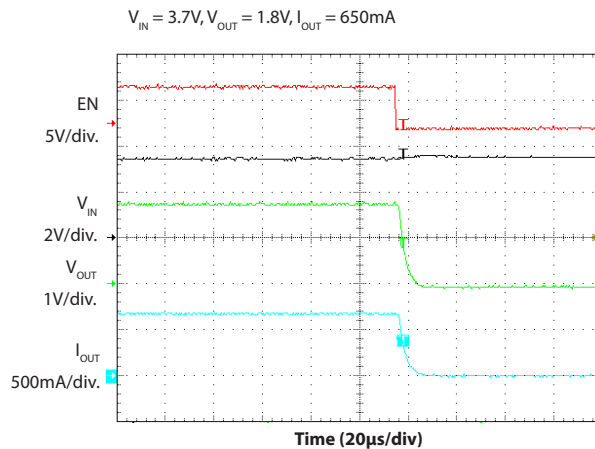
Disable Operation



Start-up Operation



Disable Operation



General Description

The SC220/Q is a step-down regulator capable of delivering a lower voltage from an input supply voltage of 2.7V to 5.5V with high efficiency. Using a unique control architecture, the SC220/Q is capable of delivering a peak efficiency of 90%, while maintaining efficiency over 80% during light load condition. The converter operates at 20MHz switching frequency with pulse width modulation (PWM) at moderate to heavy loads up to 650mA. Under light load, the converter operates in power save (PSAVE) mode.

Control Scheme

The SC220/Q operates with a self-oscillating control method based on the output voltage ripple. This control loop compares the output voltage to an internal 1V reference to regulate the output voltage directly, adjusting the turn-on and turn-off time of the power switches such that the output voltage at the load is held at a precise value. This architecture gives a single-cycle response to transient events.

To maintain constant frequency, a phase locked loop (PLL) is included to synchronize the switching with an internal clock. This PLL adjusts the effective upper and lower thresholds of the comparator, thus maintaining a constant frequency. Under transient conditions the voltage control loop determines the required switching pattern to best maintain the output voltage. After a short transient, the PLL will bring the switching frequency back to normal. At extreme duty cycles, where the frequency control loop may not be able to maintain frequency lock even under steady-state conditions, frequency may fall, but the output voltage regulation will be maintained by the main voltage control loop. This unique architecture helps to achieve the excellent line and load transient response.

Operating Modes

The SC220/Q operates in two modes over a wide range of load currents. At moderate to high load, it operates in PWM mode with its switching frequency held constant. Under light loads, the converter enters PSAVE mode automatically. With the typical 220nH inductor, the transition between PWM and PSAVE mode typically occurs in the

range of 100-200mA, depending on the input and output voltages. At very light loads, the SC220/Q maintains high efficiency by shutting down all but the most essential circuit blocks, maintaining a typical quiescent current of about 19 μ A. In this mode, some circuitry used to control absolute DC accuracy is turned off. In that case, there may be a small DC shift (tens of mV) between normal operation and this 'no-load' state. However, in the case of a load transient, the system will turn on the high-side FET within nanoseconds as a discontinuous pulse is issued. The transition to PWM mode can occur within that nominal on-time, giving superior no load to full load transient response.

The transition from PWM mode to PSAVE mode is controlled by sensing the minimum value of the ripple current. When it drops below a threshold level for 32 consecutive cycles, the transition to PSAVE mode is initiated. Once in PSAVE, the regulation is maintained by modulating the time between fixed current pulses. When a new pulse is required by the loop before the existing pulse has terminated, the loop determines that the load cannot be maintained in PSAVE mode. This prompts an instantaneous switch from PSAVE mode back to PWM mode.

Enable and Start-up

The SC220/Q is enabled by applying a voltage higher than 1.2V on EN pin, and it is disabled when the applied voltage is pulled below the logic low threshold. The EN pin can also be used to set the switching frequency: if a digital clock is fed to EN, the SC220/Q will sense this as a valid enable signal and the external clock will be used rather than the internal 20MHz oscillator.

The SC220/Q has an internal soft start circuit that limits the inrush current during start-up with a stepped current limit. Over the course of about 40 μ s, the SC220/Q is stepped in increments of one quarter of the nominal current limit to full current limit, thereby reducing the worst-case surge current that might otherwise be reflected to the input current.

Current Limit

The SC220/Q integrates a current limit feature to protect itself and the external components during over load condition. When the current in the high-side PMOS switch exceeds the current limit, the PMOS switch is turned off.

Applications Information (Cont.)

PCB Layout Considerations

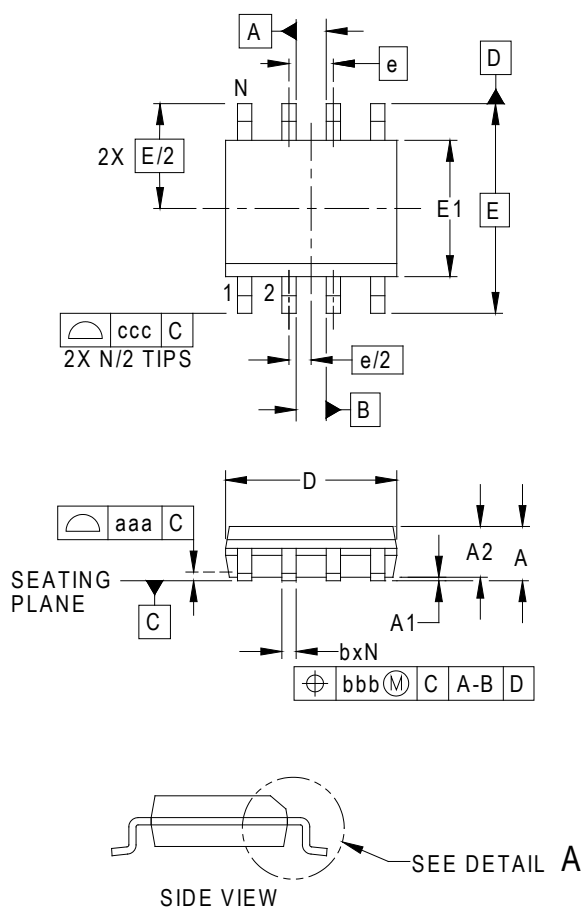
Fundamental layout rules must be followed since the layout is critical for achieving the desirable performance.

Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses, and possibly poor regulation and instability.

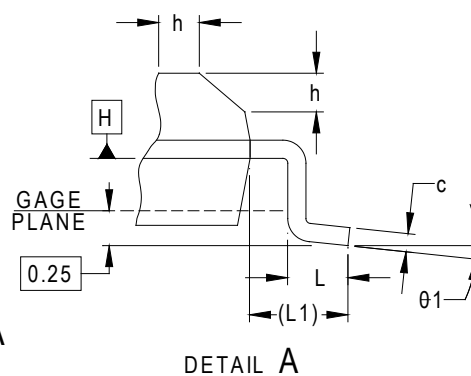
The following guidelines are recommended when developing a PCB layout:

1. The input capacitor, C_{IN} should be placed as close to the PVIN and PGND pins as possible. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to connect this capacitor as close to the IC as possible. This will minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. Keep the SW pin traces as short as possible to minimize pickup of high frequency switching edges to other parts of the circuit. C_{OUT} and L should be connected as close as possible between the SW and GND pins, with a direct return to the GND pin from C_{OUT} .
3. Route the output voltage feedback/sense path away from the inductor and SW node to minimize noise and magnetic interference to the output feedback/sense path.
4. Use a ground plane referenced to the PGND pin, and the ground connection of the input and output capacitors should be put on this plane and close to each other if possible, and as close to the PGND pin as possible. Use several vias to connect to the component side ground to further reduce noise and interference on sensitive circuit nodes.
5. If possible, minimize the resistance from the VOUT and AGND pin to the load. This will reduce the voltage drop on the ground plane and improve the load regulation. And it will also improve the overall efficiency by reducing the copper losses on the output and ground planes.

Outline Drawing — SOIC 8 Lead



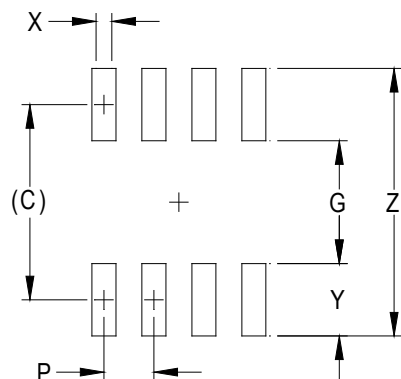
DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern —SOIC 8 Lead



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

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Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

www.semtech.com