ZiLOG
Totally Logical

Z86C34/C35/C36
Z86C44/C45/C46

CMOS Z8® MCUs WITH ASCI UART OFFER EFFICIENT, COST-EFFECTIVE DESIGN FLEXIBILITY

FEATURES

Device	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z86C34	16	237	16
Z86C35	32	237	16
Z86C36	64	237	16
Z86C44	16	236	16
Z86C45	32	236	16
Z86C46	64	236	16

Note: *General-Purpose.

- 28-Pin DIP, 28-Pin SOIC and PLCC Packages (C34, C35, C36)
- 40-Pin DIP, 44-Pin PLCC and QFP Packages (C44, C45, C46)
- 3.0- to 5.5-Volt Operating Range
- Clock Free Watch-Dog Timer (WDT) Reset
- Operating Temperature Ranges:
  Standard: 0 °C to 70 °C
  Extended: –40 °C to +105 °C
- Expanded Register File (ERF)
- Full-Duplex UART (ASCI)
- Dedicated 16-Bit Baud Rate Generator
- 32 Input/Output Lines (C44/C45/C46)
  24 Input/Output Lines (C34/C35/C36)
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and ROM Protect
- Optional 32-kHz Oscillator

GENERAL DESCRIPTION

ZiLOG's Z8® MCU single-chip family now includes the Z86C34/C35/C36/C44/C45/C46 product line, featuring enhanced wake-up circuitry, programmable Watch-Dog Timers (WDT), and low-noise/EMI options. Each of the new enhancements to the Z8 offer a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. The low-power consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z8 subfamily features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, Data Memory, and ERF. The Register File is composed of 236/237 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The ERF consists of twelve control registers.

For applications demanding powerful I/O capabilities, the Z86C34/C35/C36 offers 24 pins, and the Z86C44/C45/C46 offers 32 pins dedicated to input and output. These lines are

GENERAL DESCRIPTION (Continued)

configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and address/data bus for interfacing external memory.

To unburden the system from coping with real-time tasks such as counting/timing and data communication, the Z8 offer two on-chip counter/timers with a large number of user-selectable modes.

With ROM/ROMless selectivity, the Z86C44/C45/C46 provide both external memory and preprogrammed ROM, which enables this Z8® MCU to be used in high-volume applications, or where code flexibility is required.

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

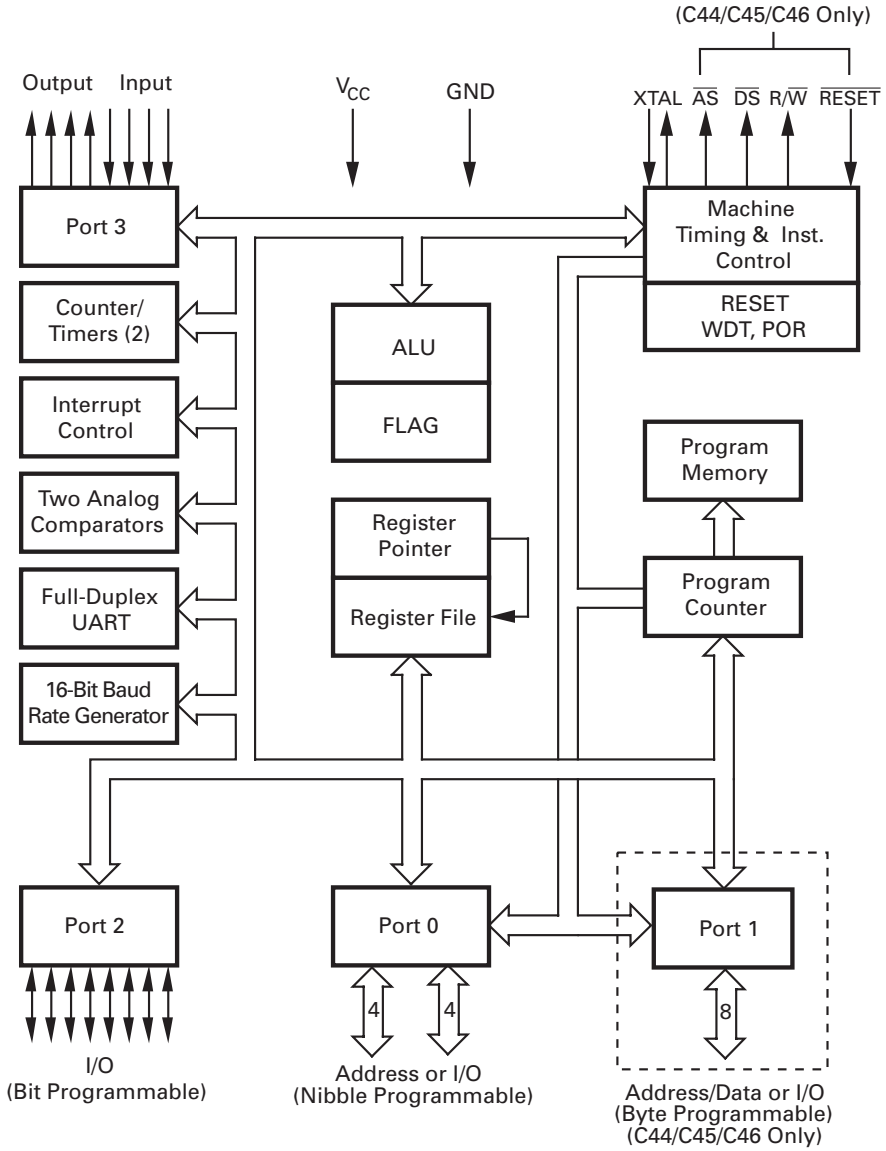


Figure 1. Functional Block Diagram

PIN DESCRIPTION

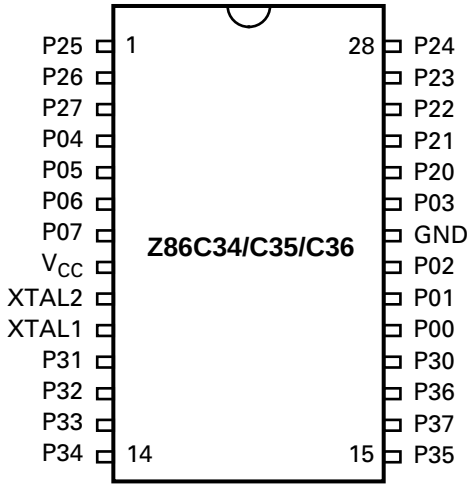


Figure 2. 28-Pin DIP/SOIC Pin Configuration

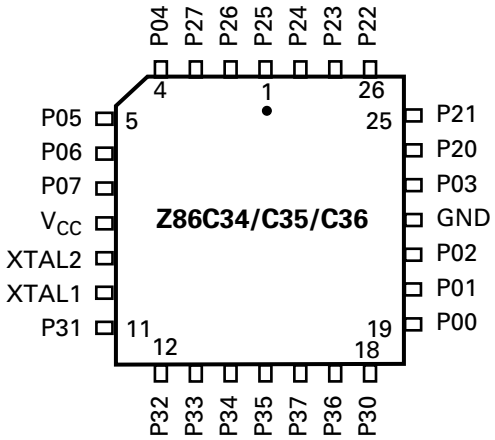


Figure 3. 28-Pin PLCC Pin Configuration

Table 1. 28-Pin DIP/SOIC/PLCC Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–27	Port 2, Bits 5,6,7	In/Output
4–7	P04–07	Port 0, Bits 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11–13	P31–33	Port 3, Bits 1,2,3	Fixed Input
14–15	P34–35	Port 3, Bits 4,5	Fixed Output
16	P37	Port 3, Bit 7	Fixed Output
17	P36	Port 3, Bit 6	Fixed Output
18	P30	Port 3, Bit 0	Fixed Input
19–21	P00–02	Port 0, Bits 0,1,2	In/Output
22	GND	Ground	
23	P03	Port 0, Bit 3	In/Output
24–28	P20–24	Port 2, Bits 0,1,2,3,4	In/Output

PIN DESCRIPTION (Continued)

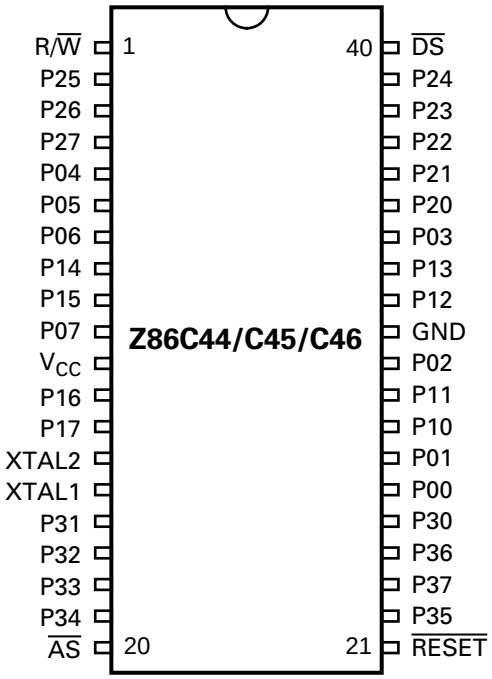


Figure 4. 40-Pin DIP Configuration

Table 2. 40-Pin Dual-In-Line Package Pin Identification

Pin #	Symbol	Function	Direction
1	R/$\overline{W}$	READ/WRITE	Output
2–4	P25–27	Port 2, Bits 5,6,7	In/Output
5–7	P04–06	Port 0, Bits 4,5,6	In/Output
8–9	P14–15	Port 1, Bits 4,5	In/Output
10	P07	Port 0, Bit 7	In/Output
11	V_{CC}	Power Supply	
12–13	P16–17	Port 1, Bits 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16–18	P31–33	Port 3, Bits 1,2,3	Input
19	P34	Port 3, Bit 4	Output
20	$\overline{AS}$	Address Strobe	Output

Table 2. 40-Pin Dual-In-Line Package Pin Identification

Pin #	Symbol	Function	Direction
21	$\overline{RESET}$	Reset	Input
22	P35	Port 3, Bit 5	Output
23	P37	Port 3, Bit 7	Output
24	P36	Port 3, Bit 6	Output
25	P30	Port 3, Bit 0	Input
26–27	P00–01	Port 0, Bit 0,1	In/Output
28–29	P10–11	Port 1, Bit 0,1	In/Output
30	P02	Port 0, Bit 2	In/Output
31	GND	Ground	
32–33	P12–13	Port 1, Bit 2,3	In/Output
34	P03	Port 0, Bit 3	In/Output
35–39	P20–24	Port 2, Bit 0,1,2,3,4	In/Output
40	$\overline{DS}$	Data Strobe	Output

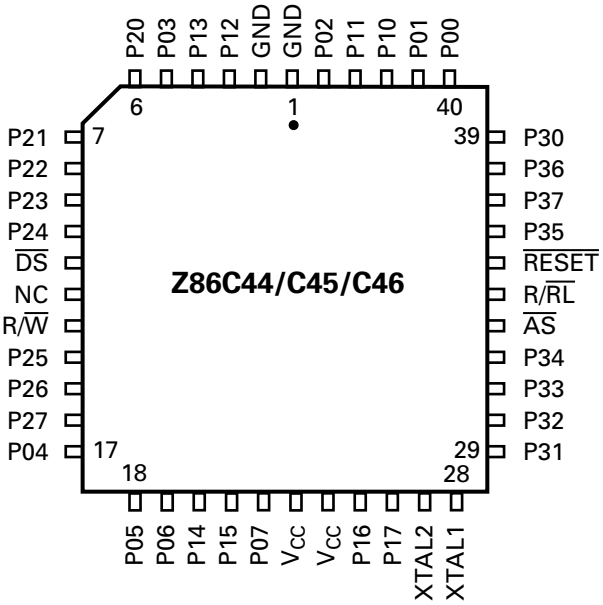


Figure 5. 44-Pin PLCC Pin Configuration

Table 3. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1–2	GND	Ground	
3–4	P12–13	Port 1, Bits 2,3	In/Output
5	P03	Port 0, Bit 3	In/Output
6–10	P20–24	Port 2, Bits 0,1,2,3,4	In/Output
11	$\overline{DS}$	Data Strobe	Output
12	NC	Not Connected	
13	R/$\overline{W}$	READ/WRITE	Output
14–16	P25–27	Port 2, Bits 5,6,7	In/Output
17–19	P04–06	Port 0, Bits 4,5,6	In/Output
20–21	P14–15	Port 1, Bits 4,5	In/Output
22	P07	Port 0, Bit 7	In/Output
23–24	V_{CC}	Power Supply	
25–26	P16–17	Port 1, Bits 6,7	In/Output

Table 3. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
27	XTAL2	Crystal Oscillator	Output
28	XTAL1	Crystal Oscillator	Input
29–31	P31–33	Port 3, Bits 1,2,3	Input
32	P34	Port 3, Bit 4	Output
33	$\overline{AS}$	Address Strobe	Output
34	R/$\overline{RL}$	ROM/ROMless Control	Input
35	$\overline{RESET}$	Reset	Input
36	P35	Port 3, Bit 5	Output
37	P37	Port 3, Bit 7	Output
38	P36	Port 3, Bit 6	Output
39	P30	Port 3, Bit 0	Input
40–41	P00–01	Port 0, Bits 0,1	In/Output
42–43	P10–11	Port 1, Bits 0,1	In/Output
44	P02	Port 0, Bit 2	In/Output

PIN DESCRIPTION (Continued)

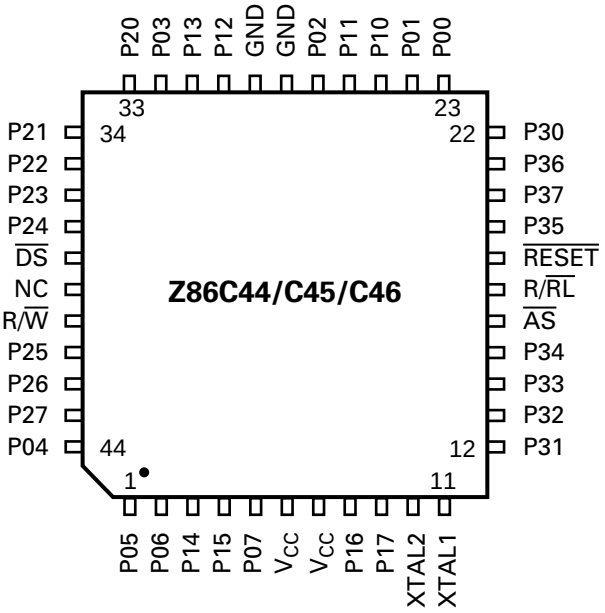


Figure 6. 44-Pin QFP Pin Configuration

Table 4. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
1–2	P05–06	Port 0, Bits 5,6	In/Output
3–4	P14–15	Port 1, Bits 4,5	In/Output
5	P07	Port 0, Bit 7	In/Output
6–7	V_{CC}	Power Supply	
8–9	P16–17	Port 1 Bits 6,7	In/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12–14	P31–33	Port 3, Bits 1,2,3	Input
15	P34	Port 3, Bit 4	Output
16	$\overline{AS}$	Address Strobe	Output
17	R/$\overline{RL}$	ROM/ROMless Control	Input
18	$\overline{RESET}$	Reset	Input
19	P35	Port 3, Bit 5	Output
20	P37	Port 3, Bit 7	Output

Table 4. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
21	P36	Port 3, Bit 6	Output
22	P30	Port 3, Bit 0	Input
23–24	P00–01	Port 0, Bits 0,1	In/Output
25–26	P10–11	Port 1, Bits 0,1	In/Output
27	P02	Port 0, Bit 2	In/Output
28–29	GND	Ground	
30–31	P12–13	Port 1, Bits 2,3	In/Output
32	P03	Port 0, Bit 3	In/Output
33–37	P20–24	Port 2, Bits 0,1,2,3,4	In/Output
38	$\overline{DS}$	Data Strobe	Output
39	NC	Not Connected	
40	R/$\overline{W}$	READ/WRITE	Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on XTAL1 and $\overline{\text{RESET}}$ Pins with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		1.21	W	
Maximum Allowable Current out of V_{SS}		220	mA	
Maximum Allowable Current into V_{DD}		180	mA	
Maximum Allowable Current into an Input Pin	–600	+600	µA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. Applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD} and current into pin is limited to ±600 µA.
3. Excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.21 W for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH}), + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

STANDARD TEST CONDITIONS

The characteristics listed in following pages apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7.)

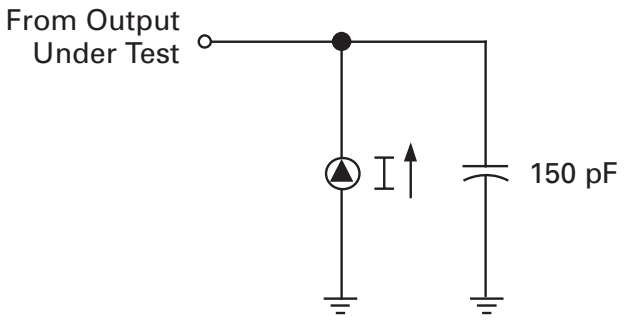


Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins to GND

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Table 5. DC Characteristics

			T_A = 0°C to +70°C		T_A = –40°C to +105°C					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Min**	**Max**	**Typical[2] @25°C**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.6	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND–0.3	0.2 V_{CC}	GND–0.3	0.2 V_{CC}	1.2	V	Driven by External Clock Generator	
		5.5V	GND–0.3	0.2 V_{CC}	GND–0.3	0.2 V_{CC}	2.1	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.6	V		
V_{IL}	Input Low Voltage	3.0V	GND–0.3	0.2 V_{CC}	GND–0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND–0.3	0.2 V_{CC}	GND–0.3	0.2 V_{CC}	1.6	V		
V_{OH}	Output High Voltage (Low-EMI Mode)	3.0V	V_{CC}–0.4		V_{CC}–0.4		3.1	V	I_{OH} = –0.5 mA	
		5.0V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	I_{OH} = –0.5 mA	
V_{OH1}	Output High Voltage	3.0V	V_{CC}–0.4		V_{CC}–0.4		3.1	V	I_{OH} = –2.0 mA	3
		5.5V	V_{CC}–0.4		V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	3
V_{OL}	Output Low Voltage (Low-EMI Mode)	3.0V		0.6		0.6	0.2	V	I_{OL} = 1.0 mA	
		5.0V		0.4		0.4	0.1	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	3.0V		0.6		0.6	0.2	V	I_{OL} = +4.0 mA	3
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	3

Notes:

1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typicals are at V_{CC} = 5.0V and 3.3V.
3. Standard Mode (not Low EMI).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
9. 0ºC to 70ºC (standard temperature).
10. Auto Latch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region.
12. –40˚C to 150˚C (extended temperature).

DC ELECTRICAL CHARACTERISTICS (Continued)

Table 5. DC Characteristics (Continued)

			T_A = 0°C to +70°C		T_A = –40°C to +105°C					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Min**	**Max**	**Typical[2] @25°C**	**Units**	**Conditions**	**Notes**
V_{OL2}	Output Low Voltage	3.0V		1.2		1.2	0.3	V	I_{OL} = +6 mA	3
		5.5V		1.2		1.2	0.4	V	I_{OL} = +12 mA	3
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.8	V		4
		5.5V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.6	V		4
V_{RI}	Reset Input Low Voltage	3.0V	GND–0.3	0.2 V_{CC}	GND–0.3	0.2 V_{CC}	1.1	V		4
		5.5V	GND–0.3	0.2 V_{CC}	GND–0.3	0.2 V_{CC}	1.6	V		4
V_{OLR}	Reset Output Low Voltage	3.0V		0.6		0.6	0.3	V	I_{OL} = +1.0 mA	4
		5.5V		0.6		0.6	0.3	V	I_{OL} = +1.0 mA	4
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		5
		5.5V		25		25	10	mV		5
I_{IL}	Input Leakage	3.0V	–1	2	–1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	2	–1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	–1	1	–1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	1	–1	2	0.004	µA	V_{IN} = 0V, V_{CC}	
IIR	Reset Input Current	3.0V	–20	–130	–18	–130	–60	µA		
		5.5V	–20	–180	–18	–180	–85	µA		
I_{CC}	Supply Current	3.0V		20		20	7	mA	@ 16 MHz	6
		5.5V		25		25	20	mA	@ 16 MHz	6
		3.0V		15		15	5	mA	@ 12 MHz	6
		5.5V		20		20	15	mA	@ 12 MHz	6

Notes:

1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typicals are at V_{CC} = 5.0V and 3.3V.
3. Standard Mode (not Low EMI).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
9. 0ºC to 70ºC (standard temperature).
10. Auto Latch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region.
12. –40˚C to 150˚C (extended temperature).

Table 5. DC Characteristics (Continued)

			T_A = 0°C to +70°C		T_A = –40°C to +105°C					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Min**	**Max**	**Typical[2] @25°C**	**Units**	**Conditions**	**Notes**
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	6
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	6
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	6
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	6
I_{CC2}	Standby Current (STOP Mode)	3.0V		8		8	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		5.5V		10		10	4	µA	V_{IN} = 0V, V_{CC} WDT is not Running	7,8
		3.0V		500		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	7,8,9
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	7,8,9
V_{ICR}	Input Common Mode Voltage Range	3.0V	0	V_{CC}–1.0V	0	V_{CC}–1.5V		V		5
		5.5V	0	V_{CC}–1.0V	0	V_{CC}–1.5V		V		5
I_{ALL}	Auto Latch Low Current	3.0V	0.7	8	0.7	10	3	µA	0V < V_{IN} < V_{CC}	10
		5.5V	1.4	15	1.4	20	5	µA	0V < V_{IN} < V_{CC}	10
I_{ALH}	Auto Latch High Current	3.0V	–0.6	–5	–0.6	–7	–3	µA	0V < V_{IN} < V_{CC}	10
		5.5V	–1.0	–8	–1.0	–10	–6	µA	0V < V_{IN} < V_{CC}	10

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typicals are at V_{CC} = 5.0V and 3.3V.
3. Standard Mode (not Low EMI).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
9. 0ºC to 70ºC (standard temperature).
10. Auto Latch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region.
12. –40˚C to 150˚C (extended temperature).

DC ELECTRICAL CHARACTERISTICS (Continued)

Table 5. DC Characteristics (Continued)

			T_A = 0°C to +70°C		T_A = –40°C to +105°C					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Min**	**Max**	**Typical[2] @25°C**	**Units**	**Conditions**	**Notes**
V_{LV}	V_{CC} Low Voltage Protection Voltage				2.0	3.3	2.8	V	4 MHz max Int. CLK Freq.	11,12
			2.2	3.1			2.8		6 MHz max Int. CLK Freq.	9,11

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V with typicals at V_{CC} = 3.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V with typicals at V_{CC} = 5.0V.
2. Typicals are at V_{CC} = 5.0V and 3.3V.
3. Standard Mode (not Low EMI).
4. Not applicable to devices in 28-pin packages.
5. For analog comparator, inputs when analog comparators are enabled.
6. All outputs unloaded, I/O pins floating, inputs at rail.
7. Same as note 6, except inputs at V_{CC}.
8. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
9. 0ºC to 70ºC (standard temperature).
10. Auto Latch (Mask Option) selected.
11. The V_{LV} voltage increases as the temperature decreases and overlaps lower V_{CC} operating region.
12. –40˚C to 150˚C (extended temperature).

AC ELECTRICAL CHARACTERISTICS

External I/O or Memory READ and WRITE Timing

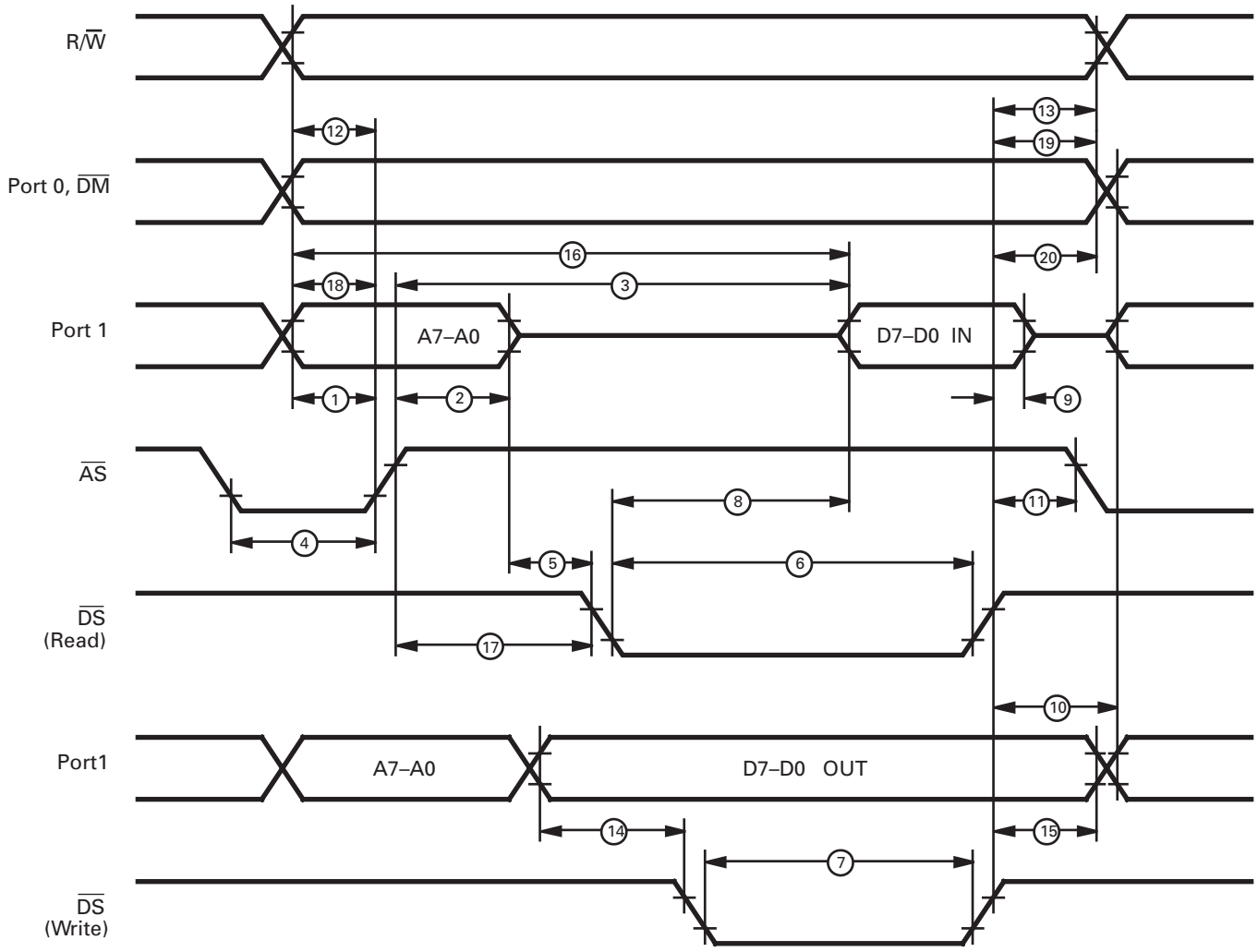


Figure 8. External I/O or Memory READ and WRITE Timing

AC ELECTRICAL CHARACTERISTICS (Continued)

Table 6. External I/O or Memory READ and WRITE Timing (C44/C45/C46 Only) (SCLK/TCLK = XTAL/2)

				T_A = –0°C to 70°C				T_A = –40°C to +105°C					
				12 MHz		16 MHz		12 MHz		16 MHz			
No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	3.0	35		25		35		25		ns	2
			5.5	35		25		35		25		ns	2
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid	3.0		250		180		250		180	ns	2,3
			5.5		250		180		250		180	ns	2
4	TwAS	$\overline{AS}$ Low Width	3.0	55		40		55		40		ns	2
			5.5	55		40		55		40		ns	2
5	TdAS(DS)	Address Float to $\overline{DS}$ Fall	3.0	0		0		0		0		ns	
			5.5	0		0		0		0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	3.0	200		135		200		135		ns	2,3
			5.5	200		135		200		135		ns	2,3
7	TwDSW	$\overline{DS}$ (WRITE) Low Width	3.0	110		80		110		80		ns	2,3
			5.5	110		80		110		80		ns	2,3
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid	3.0		150		75		150		75	ns	2,3
			5.5		150		75		150		75	ns	2,3
9	ThDR(DS)	Read Data to $\overline{DS}$ Rise Hold Time	3.0	0		0		0		0		ns	2
			5.5	0		0		0		0		ns	2
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	3.0	45		50		45		50		ns	2
			5.5	55		50		55		50		ns	2
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	3.0	30		35		30		35		ns	2
			5.5	45		35		45		55		ns	2
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rise Delay	3.0	45		25		45		25		ns	2
			5.5	45		25		45		25		ns	2
13	TdDS(R/W)	$\overline{DS}$ Rise to R/$\overline{W}$ Not Valid	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
14	TdDW(DSW)	WRITE Data Valid to $\overline{DS}$ Fall (WRITE) Delay	3.0	55		25		55		25		ns	2
			5.5	55		25		55		25		ns	2
15	TdDS(DW)	$\overline{DS}$ Rise to WRITE Data Not Valid Delay	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.0		310		230		310		230	ns	2,3
			5.5		310		230		310		230	ns	2,3

Notes:

1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
2. Timing numbers provided are for minimum TpC.
3. When using extended memory timing add 2 TpC.

Table 6. External I/O or Memory READ and WRITE Timing (C44/C45/C46 Only) (SCLK/TCLK = XTAL/2) (Continued)

				T_A = –0°C to 70°C				T_A = –40°C to +105°C					
				12 MHz		16 MHz		12 MHz		16 MHz			
No	**Symbol**	**Parameter**	V_{CC}[1]	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
17	TdAS(DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay	3.0	65		45		65		45		ns	2
			5.5	65		45		65		45		ns	2
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Fall Delay	3.0	35		30		35		30		ns	2
			5.5	35		30		35		30		ns	2
19	TdDs(DM)	$\overline{DS}$ Rise to DM Valid Delay	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2
20	ThDS(AS)	$\overline{DS}$ Valid to Address Valid Hold Time	3.0	45		35		45		35		ns	2
			5.5	45		35		45		35		ns	2

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
2. Timing numbers provided are for minimum TpC.
3. When using extended memory timing add 2 TpC.

AC ELECTRICAL CHARACTERISTICS (Continued)

Additional Timing Diagram

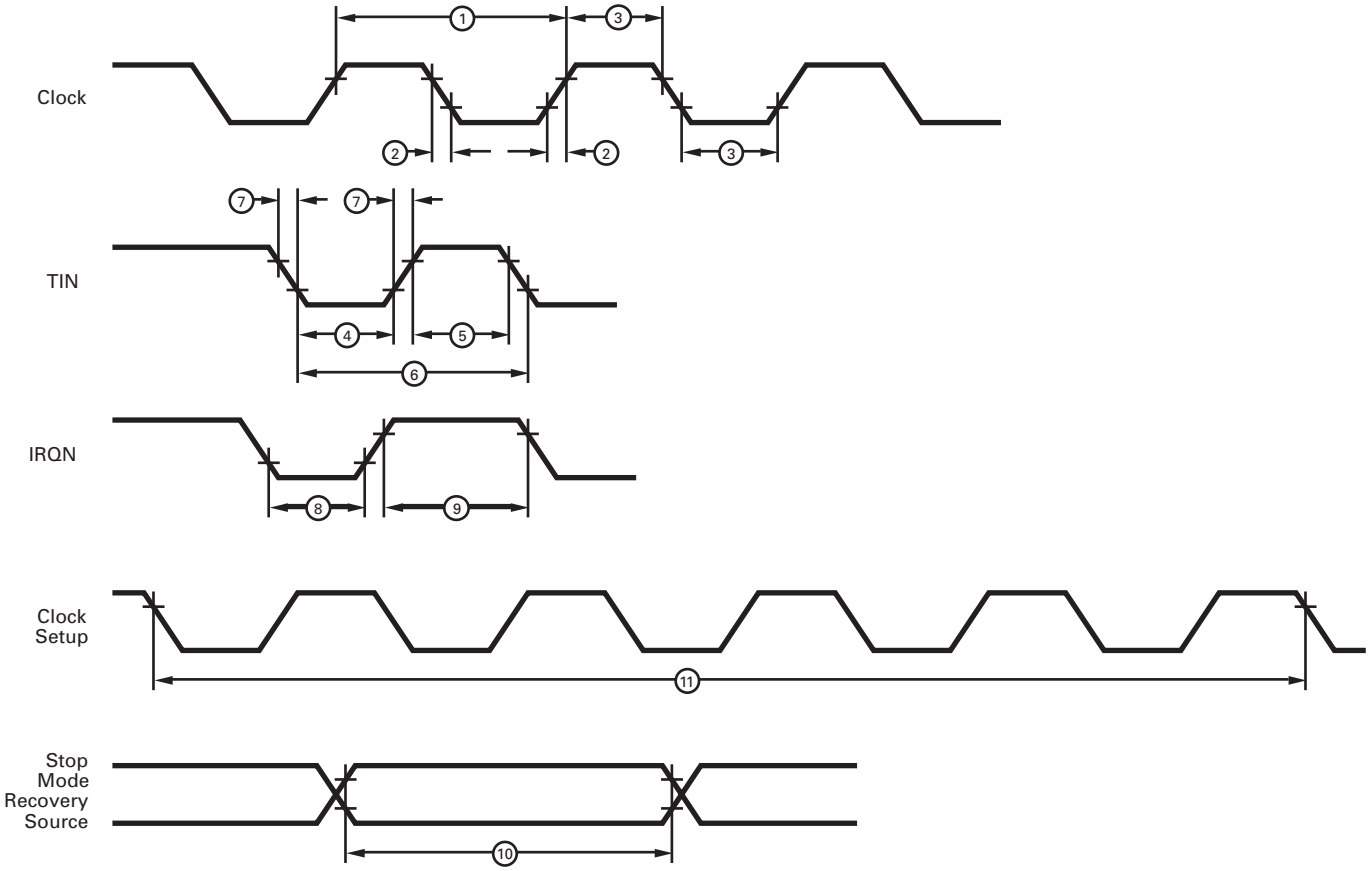


Figure 9. Additional Timing

Table 7. Additional Timing (SCLK/TCLK = XTAL/2)

				T_A = 0°C to +70°C				T_A = –40°C to +105°C						
				12 MHz		16 MHz		12 MHz		16 MHz				
No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes	D1,D0
1	TpC	Input Clock Period	3.0V	83	DC	62.5	DC	83	DC	62.5	DC	ns	2,3,4	
			5.5V	83	DC	62.5	DC	83	DC	62.5	DC	ns	2,3,4	
			3.0V	250	DC	250	DC	250	DC	250	DC	ns	2,3	
			5.5V	250	DC	250	DC	250	DC	250	DC	ns	2,3	
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		15		15		15		15	ns	2,3	
			5.5V		15		15		15		15	ns	2,3	
3	TwC	Input Clock Width	3.0V	41		31		41		31		ns	2,3,4	
			5.5V	41		31		41		31		ns	2,3,4	
			3.0V	125		125		125		125		ns	2,3	
			5.5V	125		125		125		125		ns	2,3	
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	2,3	
			5.5V	70		70		70		70		ns	2,3	
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			2,3	
			5.5V	5TpC		5TpC		5TpC		5TpC			2,3	
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			2,3	
			5.5V	8TpC		8TpC		8TpC		8TpC			2,3	
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100		100		100	ns	2,3	
			5.5V		100		100		100		100	ns	2,3	
8A	TwIL	Int. Request Low Time	3.0V	100		100		100		100		ns	2,3,5	
			5.5V	70		70		70		70		ns	2,3,5	
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC		5TpC		5TpC			2,3,6	
			5.5V	5TpC		5TpC		5TpC		5TpC			2,3,6	
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			2,3,5	
			5.5V	5TpC		5TpC		5TpC		5TpC			2,3,5	
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		12		12		ns	7	
			5.5V	12		12		12		12		ns	7	
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		5TpC		5TpC		7,8	
			5.5V		5TpC		5TpC		5TpC		5TpC		7,8	

Notes:

1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR D1 = 0.
4. Maximum frequency for external XTAL clock is 4 MHz when using low-EMI Oscillator mode PCON Reg.D7 = 0.
5. Interrupt request via Port 3 (P31–P33).
6. Interrupt request via Port 3 (P30).
7. SMR–D5 = 1, POR STOP Mode Delay is on.
8. For RC and LC oscillator, and for oscillator driven by clock driver.
9. Register WDTMR.

AC ELECTRICAL CHARACTERISTICS (Continued)

Table 7. Additional Timing (SCLK/TCLK = XTAL/2) (Continued)

				T_A = 0ºC to +70ºC				T_A = –40ºC to +105ºC						
				12 MHz		16 MHz		12 MHz		16 MHz				
No	Symbol	Parameter	V_{CC}[1]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes	D1,D0
12	Twdt	Watch-Dog Timer Delay Timer before time-out	3.0V	7		7		7		7		ms	9	0,0
			5.5V	3.5		3.5		3.5		3.5		ms	9	0,0
			3.0V	14		14		14		14		ms	9	0,1
			5.5V	7		7		7		7		ms	9	0,1
			3.0V	28		28		28		28		ms	9	1,0
			5.5V	14		14		14		14		ms	9	1,0
			3.0V	112		112		112		112		ms	9	1,1
			5.5V	56		56		56		56		ms	9	1,1
13	TPOR	Power-On Reset Delay	3.0V	3	24	3	24	3	25	3	25	ms		
			5.5V	1.5	13	1.5	13	1	14	1	14	ms		

Notes:

1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
3. SMR D1 = 0.
4. Maximum frequency for external XTAL clock is 4 MHz when using low-EMI Oscillator mode PCON Reg.D7 = 0.
5. Interrupt request via Port 3 (P31–P33).
6. Interrupt request via Port 3 (P30).
7. SMR–D5 = 1, POR STOP Mode Delay is on.
8. For RC and LC oscillator, and for oscillator driven by clock driver.
9. Register WDTMR.

Table 8. Additional Timing
(Divide-By-One Mode, SCLK/TCLK = XTAL)

				T_A = 0ºC to +70ºC		T_A = 40ºC to +105ºC			
			V_{CC}[1]	8 MHz		8 MHz			
No	Symbol	Parameter		Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	2,3,4
			5.5V	250	DC	250	DC	ns	2,3,4
			3.0V	125	DC	125	DC	ns	2,3
			5.5V	125	DC	125	DC	ns	2,3
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	2,3
			5.5V		25		25	ns	2,3
3	TwC	Input Clock Width	3.0V	125		125		ns	2,3,4
			5.5V	125		125		ns	2,3,4
			3.0V	62		62		ns	2,3
			5.5V	62		62		ns	2,3
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	2,3
			5.5V	70		70		ns	2,3
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC			2,3
			5.5V	3TpC		3TpC			2,3
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			2,3
			5.5V	4TpC		4TpC			2,3
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	2,3
			5.5V		100		100	ns	2,3
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	2,3,5
			5.5V	70		70		ns	2,3,5
8B	TwIL	Int. Request Low Time	3.0V	3TpC		3TpC			2,3,6
			5.5V	3TpC		3TpC			2,3,6
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC			2,3,5
			5.5V	3TpC		2TpC			2,3,5
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		ns	7
			5.5V	12		12		ns	7
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		7,8
			5.5V		5TpC		5TpC		7,8

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logic "1" and 0.2 V_{CC} for a logic "0".
3. SMR D1 = 0.
4. Maximum frequency for external XTAL clock is 4 MHz when using low-EMI Oscillator mode PCON Reg.D7 = 0.
5. Interrupt request via Port 3 (P31–P33).
6. Interrupt request via Port 3 (P30).
7. SMR–D5 = 1, POR STOP Mode Delay is on.
8. For RC and LC oscillator, and for oscillator driven by clock driver.

AC ELECTRICAL CHARACTERISTICS (Continued)

Handshake Timing Diagrams

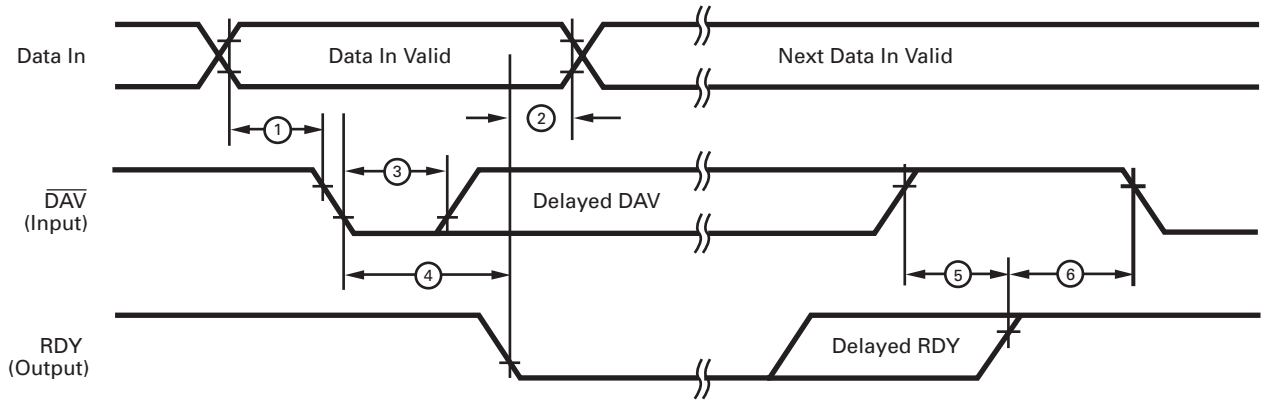


Figure 10. Input Handshake Timing

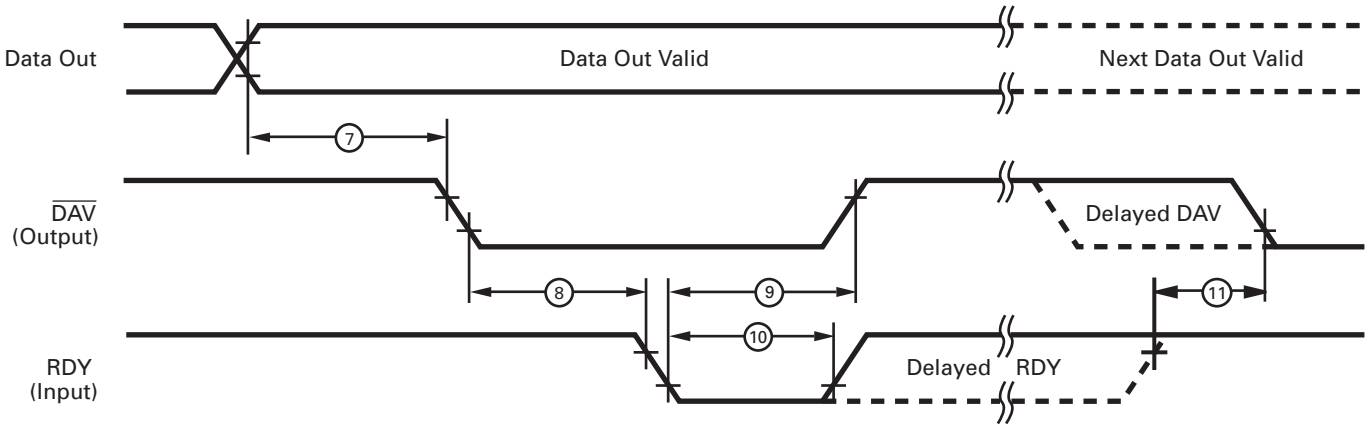


Figure 11. Output Handshake Timing

Table 9. Handshake Timing[1]

				T_A = 0°C to +70°C				T_A = –40°C to +105°C				
				12 MHz		16 MHz		12 MHz		16 MHz		
No	Symbol	Parameter	V_{CC}[2]	Min	Max	Min	Max	Min	Max	Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
2	ThDI(RDY)	Data In Hold Time	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
3	TwDAV	Data Available Width	3.0V	155		155		155		155		IN
			5.5V	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	3.0V		0		0		0		0	IN
			5.5V		0		0		0		0	IN
5	TdDAVId(RDY)	DAV Out to DAV Fall Delay	3.0V		120		120		120		120	IN
			5.5V		80		80		80		80	IN
6	RDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay	3.0V	42		31		42		31		OUT
			5.5V	42		31		42		31		OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	3.0V	0		0		0		0		OUT
			5.5V	0		0		0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	3.0V		160		160		160		160	OUT
			5.5V		115		115		115		115	OUT
10	TwRDY	RDY Width	3.0V	110		110		110		110		OUT
			5.5V	80		80		80		80		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V		110		110		110		110	OUT
			5.5V		80		80		80		80	OUT

Note:
1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. The V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.

PIN FUNCTIONS

R/$\overline{RL}$ (input, active Low). The ROM/ROMless pin, when connected to GND, disables the internal ROM and forces the device to function as a ROMless Z8. (Not available for devices in the 28-pin package.)

Notes: When left unconnected or pulled High to V_{CC}, the device functions normally as a Z8 ROM version.

When using in ROM Mode in a high-EMI (noisy) environment, the ROMless pins should be connected directly to V_{CC}.

$\overline{DS}$ (output, active Low). Data Strobe is activated one time for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{DS}$. For WRITE operations, the falling edge of $\overline{DS}$ indicates that output data is valid. (Not available for devices in the 28-pin package.)

$\overline{AS}$ (output, active Low). Address Strobe is pulsed one time at the beginning of each machine cycle for external memory transfer. Address output is from Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{AS}$. Under program control, $\overline{AS}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and READ/WRITE. (Not available for devices in the 28-pin package.)

XTAL1 Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network, or an external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R/$\overline{W}$ (output, WRITE Low). The READ/WRITE signal is Low when the Z8 is writing to the external program or data memory. (Not available for devices in the 28-pin package.)

Port 0 (P00–P07). Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03–P00 input/output and P07–P04 input/output), or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low-EMI output buffers can be globally programmed by the software. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control $\overline{\text{DAV0}}$ and RDY0. Handshake signal direction is dictated by the I/O direction (input or output) of Port 0 of the upper nibble P04–P07. The lower nibble must indicate the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are required for I/O operation, they are configured by writing to the Port 0 mode register.

In ROMless mode, after a hardware RESET, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. (In ROM mode, Port 0 is defined as input after RESET.)

Port 0 can be placed in a high-impedance state along with Port 1, $\overline{\text{AS}}$, $\overline{\text{DS}}$ and R/$\overline{\text{W}}$, allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 12).

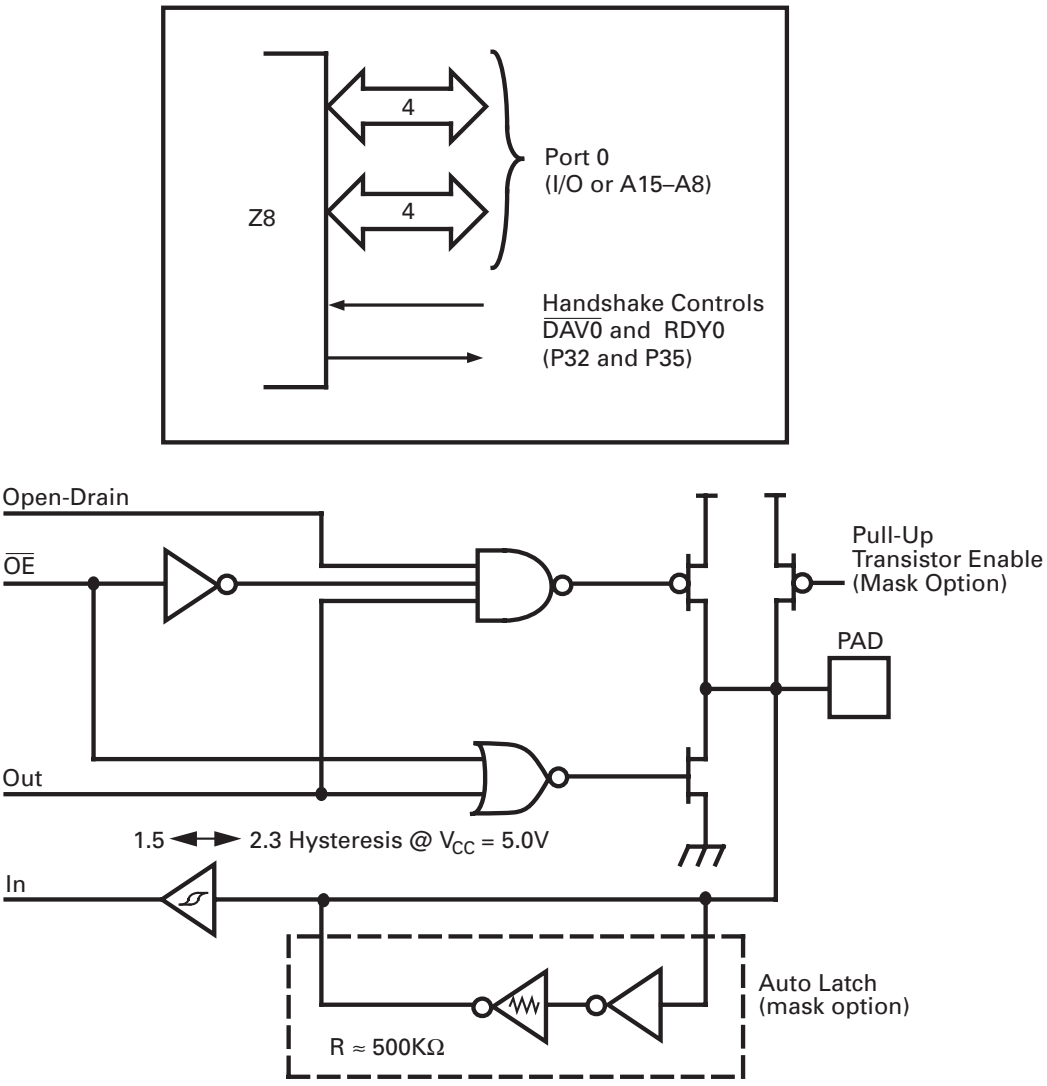


Figure 12. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17–P10). Port 1 is an 8-bit, bidirectional, CMOS-compatible port (Figure 13), with multiplexed Address (A7–A0) and Data (D7–D0) ports. For the ROM device, these eight I/O lines are programmed as inputs or outputs, or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and byte-programmed as outputs and can be globally programmed as either push-pull or open-drain. Low-EMI output buffers can be globally programmed by the software.

Note: Port 1 is not available on the devices in the 28-pin package, and P01M Register must set Bit D4,D3 as 00. Low-EMI mode is not supported on the emulator for Port1. PCON register D4 must be 1.

Port 1 may be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and $\overline{\text{DAV1}}$ (Ready and Data Available). Memory locations greater than the internal ROM address are referenced through Port 1, except for Z86C46. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{\text{AS}}$, $\overline{\text{DS}}$, and R/$\overline{\text{W}}$, allowing the Z8 to share common resources in multiprocessor and DMA applications.

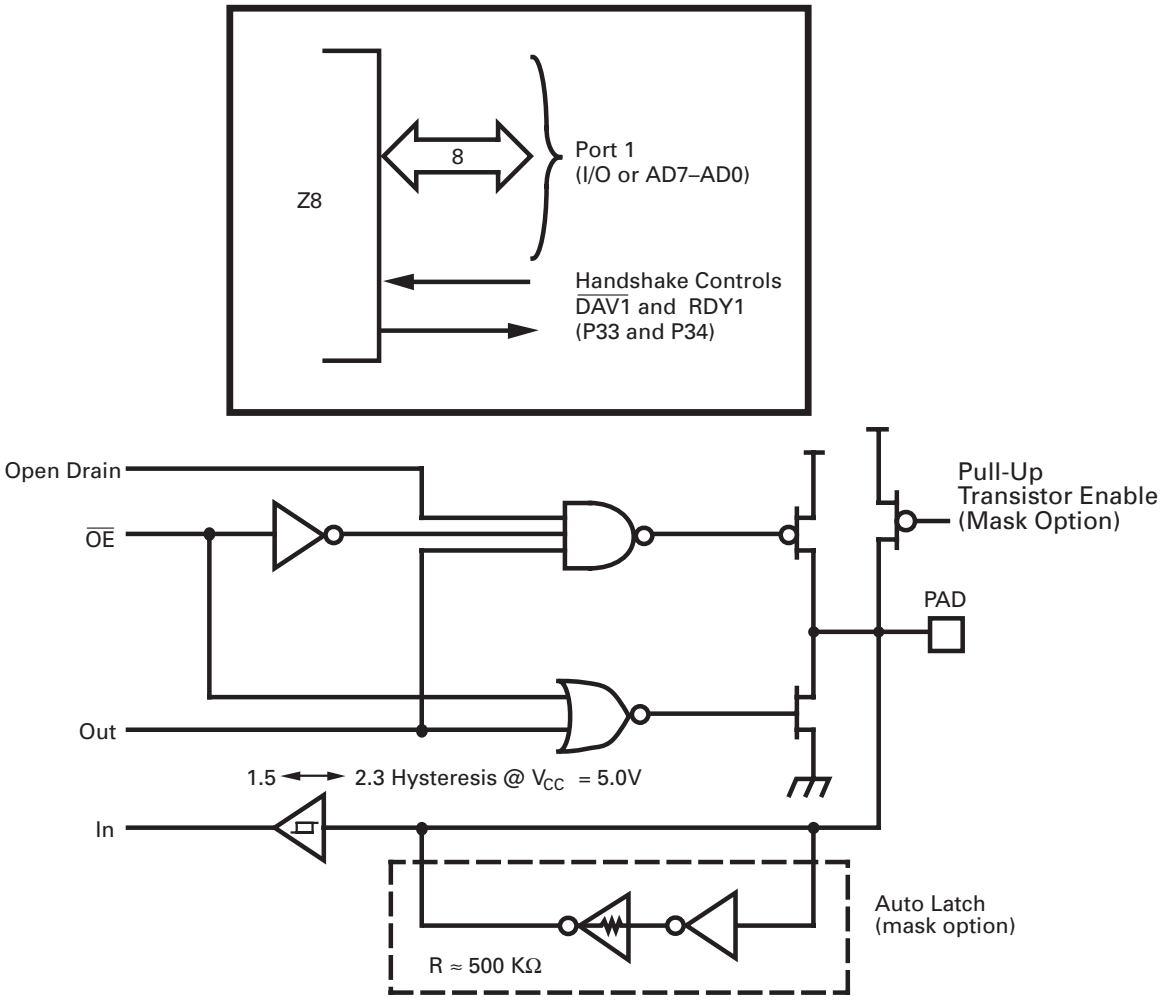


Figure 13. Port 1 Configuration

Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently. Port 2 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. Low-EMI output buffers can be globally programmed by the software.

Port 2 may be placed under handshake control. In this Handshake Mode, Port 3 lines P31 and P36 are used as the handshake controls lines $\overline{\text{DAV2}}$ and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to Bit 7, Port 2 (Figure 14).

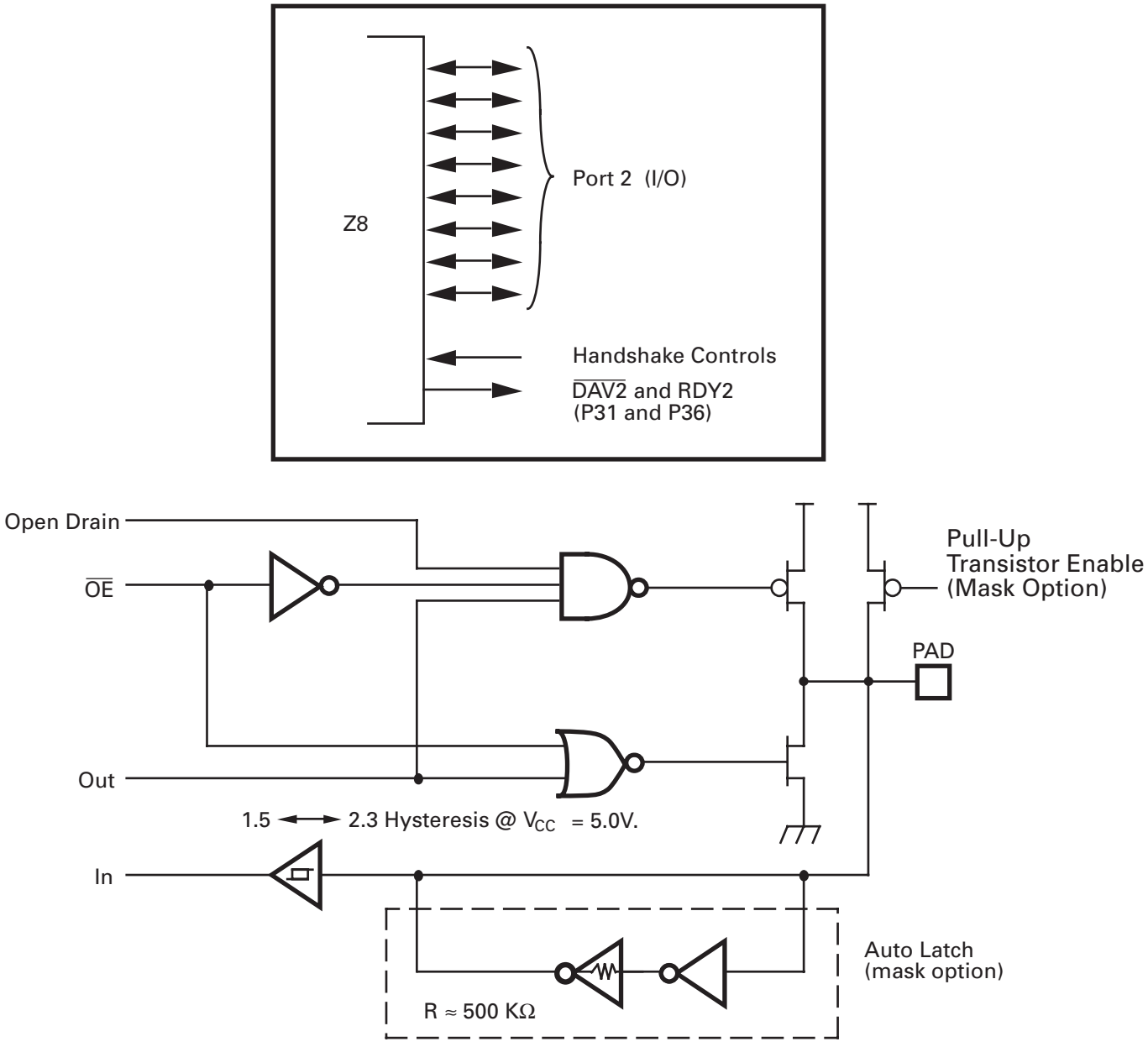


Figure 14. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37–P30). Port 3 is an 8-bit, CMOS-compatible port, with four fixed inputs (P33–P30) and four fixed outputs (P34–P37). It is configured under software control for Input/Output, Counter/Timers, interrupt, port handshake, and Data Memory functions. Port 3, bit 0 input is Schmitt-triggered, and pins P31, P32, and P33 are standard CMOS inputs (no Auto Latches). Pins P34, P35, P36, P37 are push-pull output lines. Low-EMI output buffers can be globally programmed by the software.

Two onboard comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M bit 1). For Interrupt functions, Port 3, bit 0 and pin 3 are falling edge interrupt inputs. P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register Bits 6 and 7). P33 is the comparator reference voltage input when in Analog mode. Access to Counter/Timers 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0, 1, and 2 are available on P31 through P36.

Port 3 also provides the following control functions: handshake for Ports 0, 1, and 2 ($\overline{DAV}$ and RDY); four external interrupt request signals (IRQ3–IRQ0); timer input and output signals (T_{IN} and T_{OUT}); Data Memory Select ($\overline{DM}$, see Table 10 and Figure 15).

P34 output can be software-programmed to function as a Data Memory Select (DM). The Port 3 mode register (P3M) Bit D3,D4 selects this function. When accessing external Data Memory, the P34 goes active Low; when accessing external Program Memory, the P34 goes High.

An onboard UART (ASCI) can be enabled by software by setting the RE and TE bits of the ASCI Control Register A (CNTLA). When enabled, P30 is the receive input and P37 is the transmit output.

Table 10. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Int.	P0 HS	P1 HS	P2 HS	Ext	UART
P30	IN			IRQ3					RX
P31	IN	T_{IN}	AN1	IRQ2			D/R		
P32	IN		AN2	IRQ0	D/R				
P33	IN		REF	IRQ1		D/R			
P34	OUT		AN1–OUT			R/D		$\overline{DM}$	
P35	OUT				R/D				
P36	OUT	T_{OUT}					R/D		
P37	OUT		AN2–OUT						TX

Notes:
HS = Handshake Signals
D = $\overline{DAV}$
R = RDY

Comparator Inputs and Outputs. Port 3, pins P31 and P32 each feature a comparator front end. The comparator reference voltage, pin P33, is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators and P33 is the reference voltage supplied to both comparators. In digital mode, pin P33 can be used as a P33 register input or IRQ1 source. P34 and P37 outputs the comparator outputs by software-programming the PCON Register Bit D0 to 1 (see Figure 16).

Note: The user must add a two-NOP delay after selecting the P3M bit D1 to 1 before the comparator output is valid. IRQ0, IRQ1, and IRQ2 should be cleared in the IRQ register when the comparator is enabled or disabled.

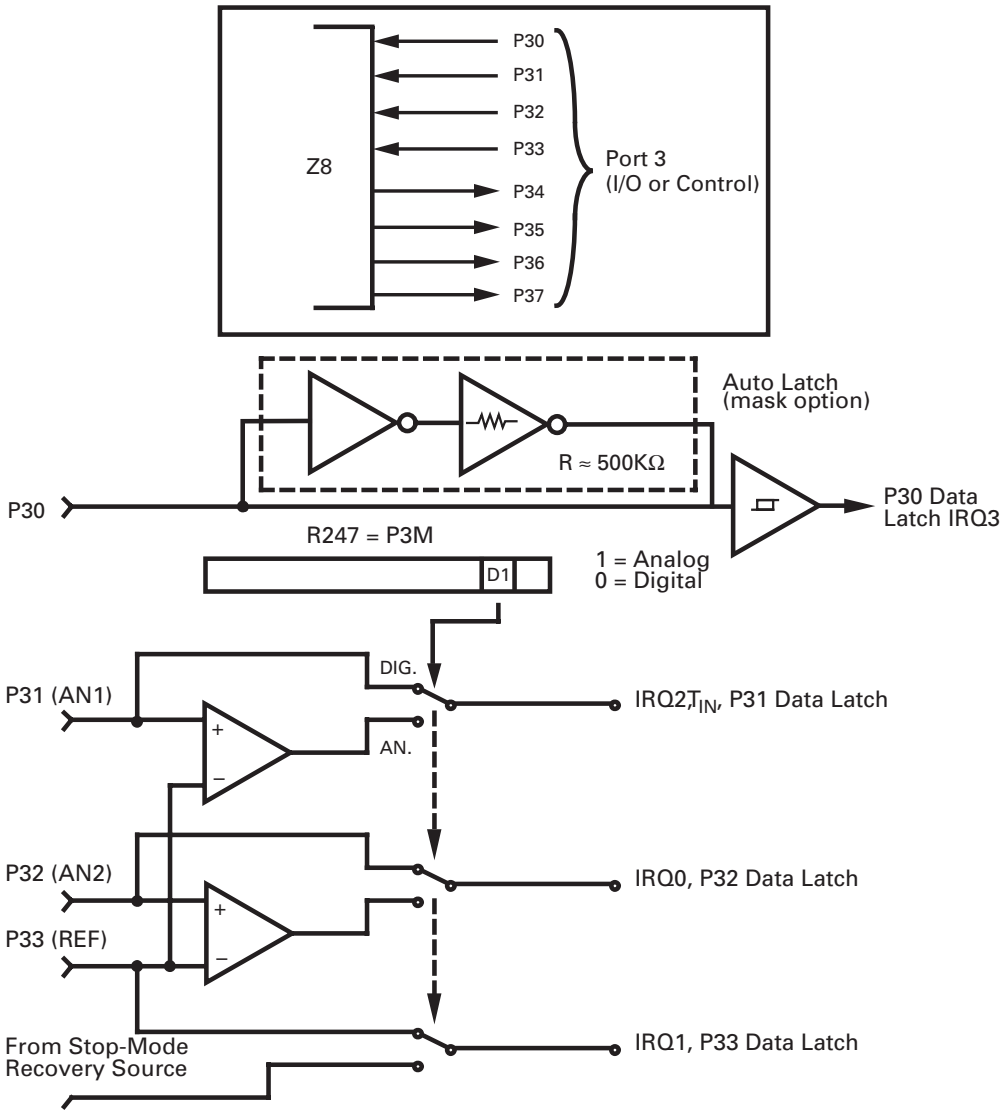


Figure 15. Port 3 Configuration

PIN FUNCTIONS (Continued)

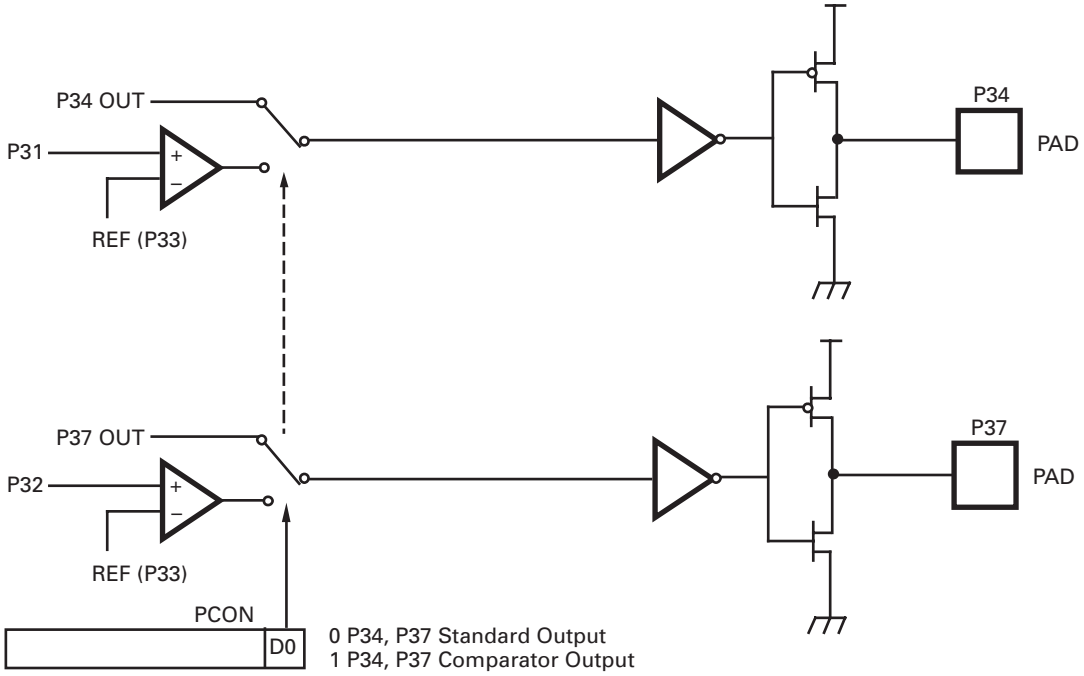


Figure 16. Port 3 Configuration

Auto Latch. The Auto Latch places valid CMOS levels on all CMOS inputs (except P33–P31) that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Auto Latches are available on Port 0, Port 1, Port 2, and P30. There are no Auto Latches on P31, P32, and P33.

Note: Deletion of all Port Auto Latches is available as a ROM Mask option. The Auto Latch Delete option is selected by the customer when the ROM code is submitted.

$\overline{\text{RESET}}$ (input, active Low). Initializes the MCU. Reset is accomplished either through Power-On Reset, Watch-Dog Timer reset, Stop-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Reset, the internally-generated reset is driving the RESET pin Low for the POR time. *Any devices driving the* RESET *line must be open-drain to avoid damage from a possible conflict during* RESET *conditions.* RESET *depends on oscillator operation to achieve full reset conditions, except for conditions wherein a* WDT *reset is permanently enabled.* Pull-up is provided internally.

Note: The $\overline{\text{RESET}}$ pin is not available on devices in the 28-pin package.

After the POR time, $\overline{\text{RESET}}$ is a Schmitt-triggered input. During the RESET cycle, $\overline{\text{DS}}$ is held active Low while $\overline{\text{AS}}$ cycles at a rate of $T_PC/2$. Program execution begins at location 000Ch, after the $\overline{\text{RESET}}$ is released. For Power-On Reset, the reset output time is T_{POR} ms.

When program execution begins, $\overline{\text{AS}}$ and $\overline{\text{DS}}$ toggles only for external memory accesses. The Z8 does not reset WDTMR, SMR, P2M, PCON, and P3M registers on a Stop-Mode Recovery operation or from a WDT reset out of STOP mode.

FUNCTIONAL DESCRIPTION

The Z8 MCU incorporates the following special functions to enhance the standard Z8® architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- External Reset
- Low Voltage Recovery

Auto Power-On Reset circuitry is built into the Z8, eliminating the requirement for an external reset circuit to reset upon power-up. The internal pull-up resistor is on the Reset pin, so a pull-up resistor is not required; however, in a high-EMI (noisy) environment, it is recommended that a small value pull-up resistor be used.

Note: The $\overline{\text{RESET}}$ pin is not available on devices in the 28-pin package.

Program Memory. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, address 12 to address 65535 (C36/C46)/32767 (C35/C45)/16383 (C34/C44) consists of on-chip mask-programmed ROM. The Z86C44/C45 can access external program and data memory from addresses 16384/32768 to 65535.

The 65535 (C36/C46)/32767 (C35/C45)/16383 (C34/C44) program memory is mask programmable. *A ROM protect feature prevents dumping of the ROM contents by inhibiting execution of* LDC, LDCI, LDE, *and* LDEI *instructions to Program Memory in external program mode*. ROM look-up tables can be used with this feature.

The ROM Protect option is mask-programmable, to be selected by the customer when the ROM code is submitted.

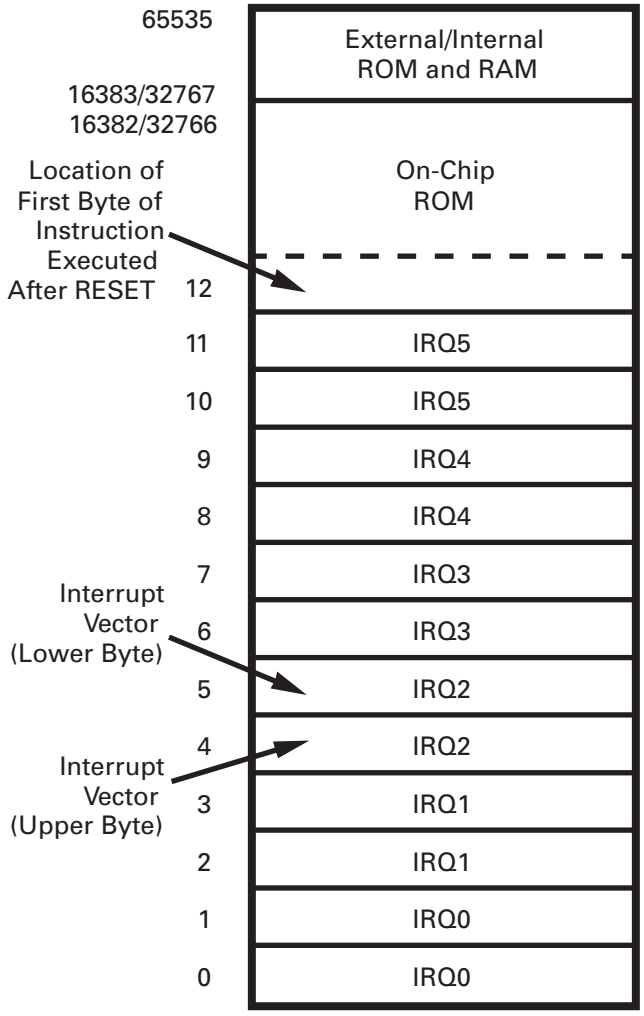


Figure 17. Program Memory Map for Z86C34/35/44/45

Data Memory ($\overline{\text{DM}}$). The ROMless version can address up to 64 KB of external data memory. External data memory may be included with, or separated from, the external program memory space. $\overline{\text{DM}}$, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 18). The state of the $\overline{\text{DM}}$ signal is controlled by the type of instruction being executed. An LDC Op Code references PROGRAM ($\overline{\text{DM}}$ inactive) memory, and an LDE instruction references data ($\overline{\text{DM}}$ active Low) memory. The user must configure Port 3 Mode Register (P3M) bits D3 and D4 for this mode. This feature is not usable for devices in 28-pin package. *When used in ROM mode, the Z86C46 cannot access any external data memory.* The Z86C44/C45 can access exter-

FUNCTIONAL DESCRIPTION (Continued)

nal program and data memory from addresses 16384/32768 to 65535.

Expanded Register File (ERF). The Z8 register file is expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 19). These register groups are known as the Expanded Register File (ERF). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register group. Three system configuration registers reside in the Expanded Register File at Bank F (PCON, SMR, WDTMR). The rest of the Expanded Register is not physically implemented, and is open for future expansion.

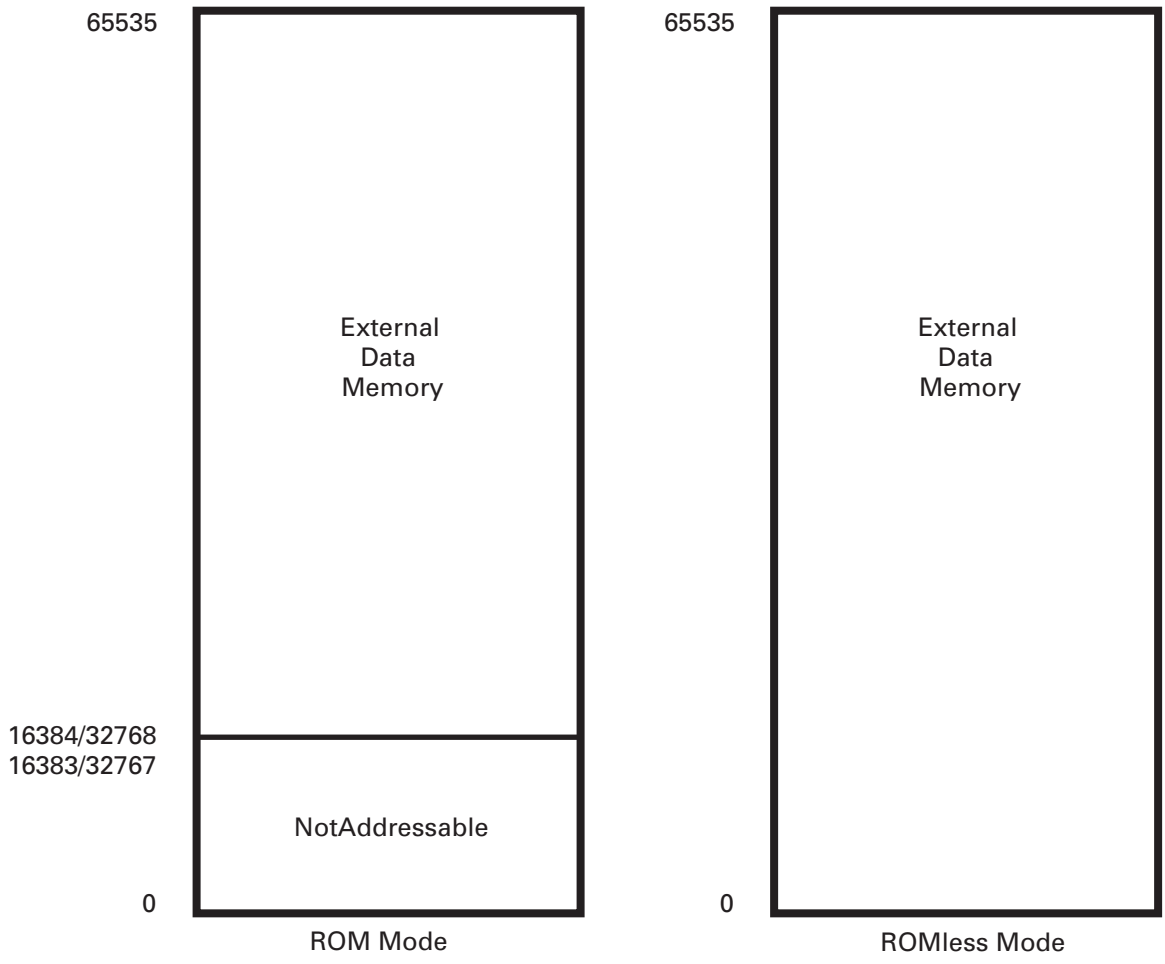


Figure 18. Data Memory Map

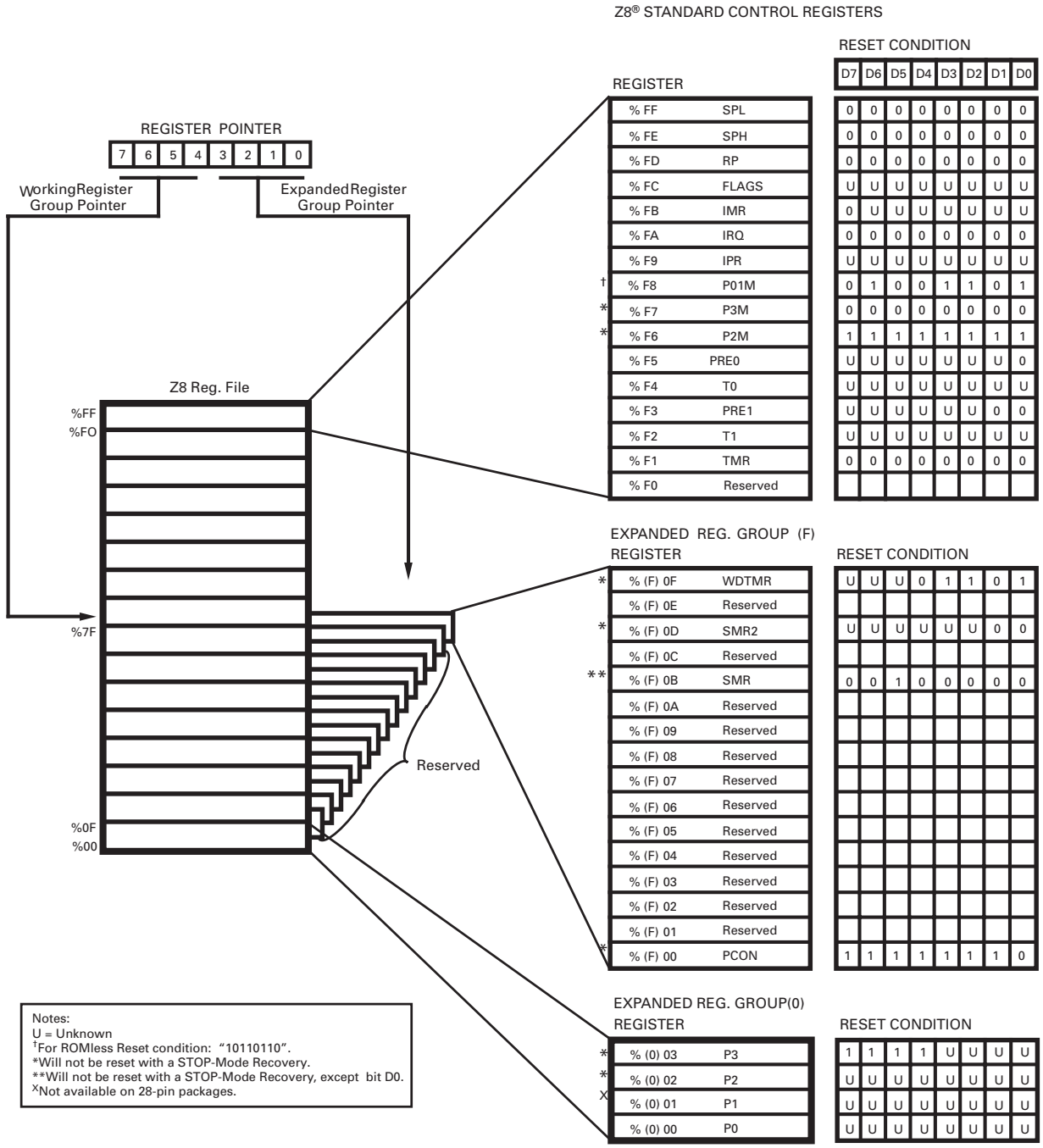


Figure 19. Expanded Register File Architecture

Register File. The register file consists of four I/O port registers, 236 general-purpose registers and 15 control and status registers (R0–R3, R4–R239 and R240–R255, respectively), plus three system configuration registers in the expanded register group. The instructions access registers directly or indirectly through an 8-bit address field. As a result, a short, 4-bit register address can use the Register Pointer (Figure 20). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16

FUNCTIONAL DESCRIPTION (Continued)

continuous locations. The Register Pointer addresses the starting location of the active working register group.

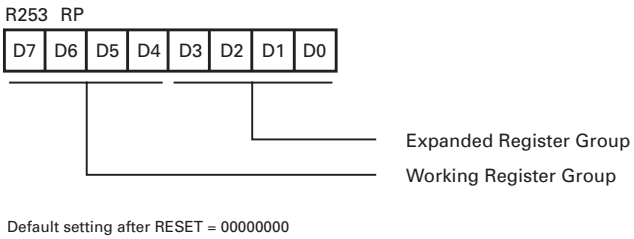


Figure 20. Register Pointer

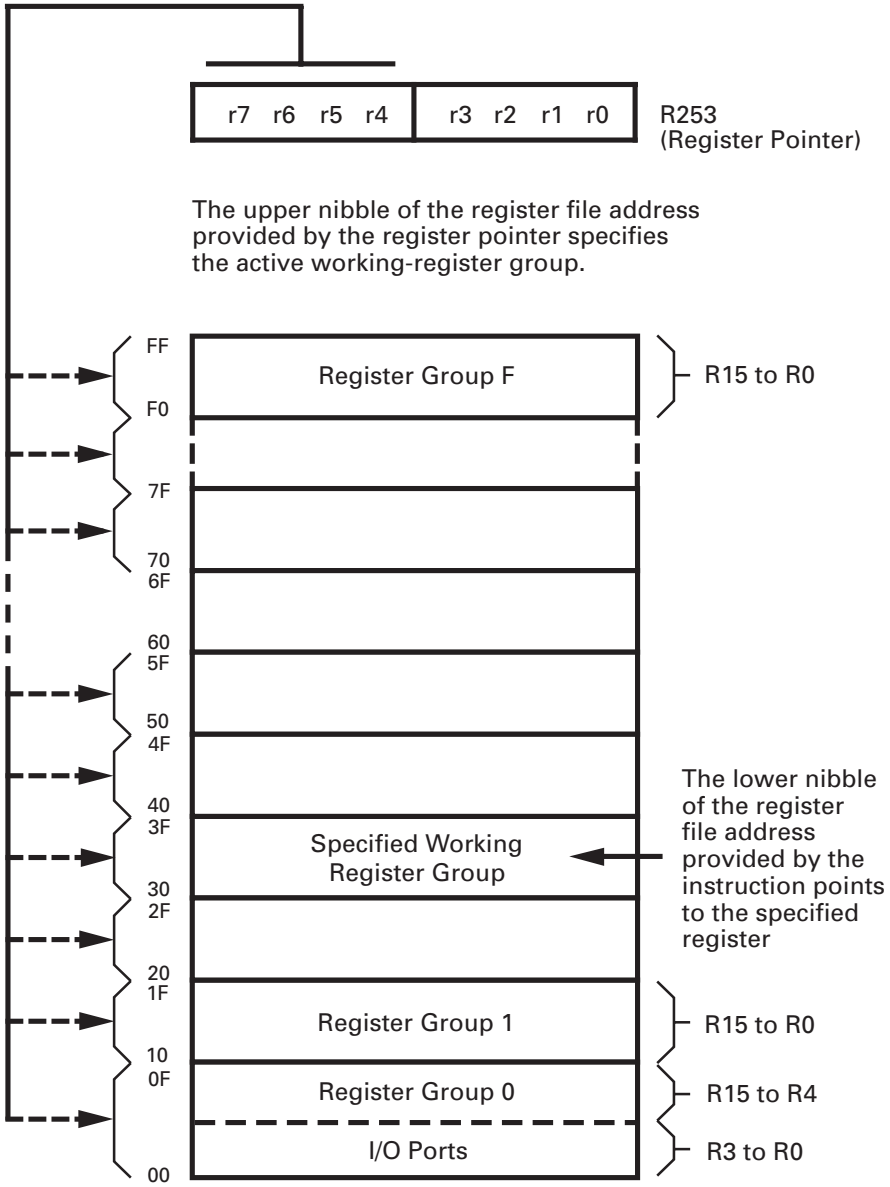


Figure 21. Register Pointer—Detail

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their most recent value after any RESET, as long as the RESET occurs in the V_{CC} voltage-specified operating range. These do not keep their most recent state from a Low Voltage Protection (V_{LV}) RESET if the V_{CC} drops below 1.8V.

Note: Register Bank E0–EF is only accessed through working register and indirect addressing modes.

RAM Protect. The upper portion of the RAM's address spaces %80F to %EF (excluding the control registers) are protected from writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or 1 into the IMR register, bit D6. A 1 in D6 enables RAM Protect.

Stack. The Z8 internal register file is used for the stack. The 16-bit Stack Pointer (R254–R255) is used for the external stack, which can reside anywhere in the data memory for ROMless mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4–R239). Stack Pointer High (SPH) is used as a general-purpose register when using internal stack only. The devices in 28-pin packages use the 8-bit stack pointer (R255) for internal stack only.

Note: R254 and R255 are set to 00h after any RESET or Stop-Mode Recovery.

Counter/Timers. There are two 8-bit programmable counter/timers (T0–T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 22).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that is loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to START, STOP, restart to CONTINUE, or restart from the initial value. The counters can also be programmed to STOP upon reaching 0 (single pass mode) or to automatically reload the initial value and continue counting (modulo–n continuous mode).

The counters, *but not the prescalers*, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divide-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or nonretriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1. T_{IN} Mode is enabled by setting R243 PRE1 bit D1 to 0.

FUNCTIONAL DESCRIPTION (Continued)

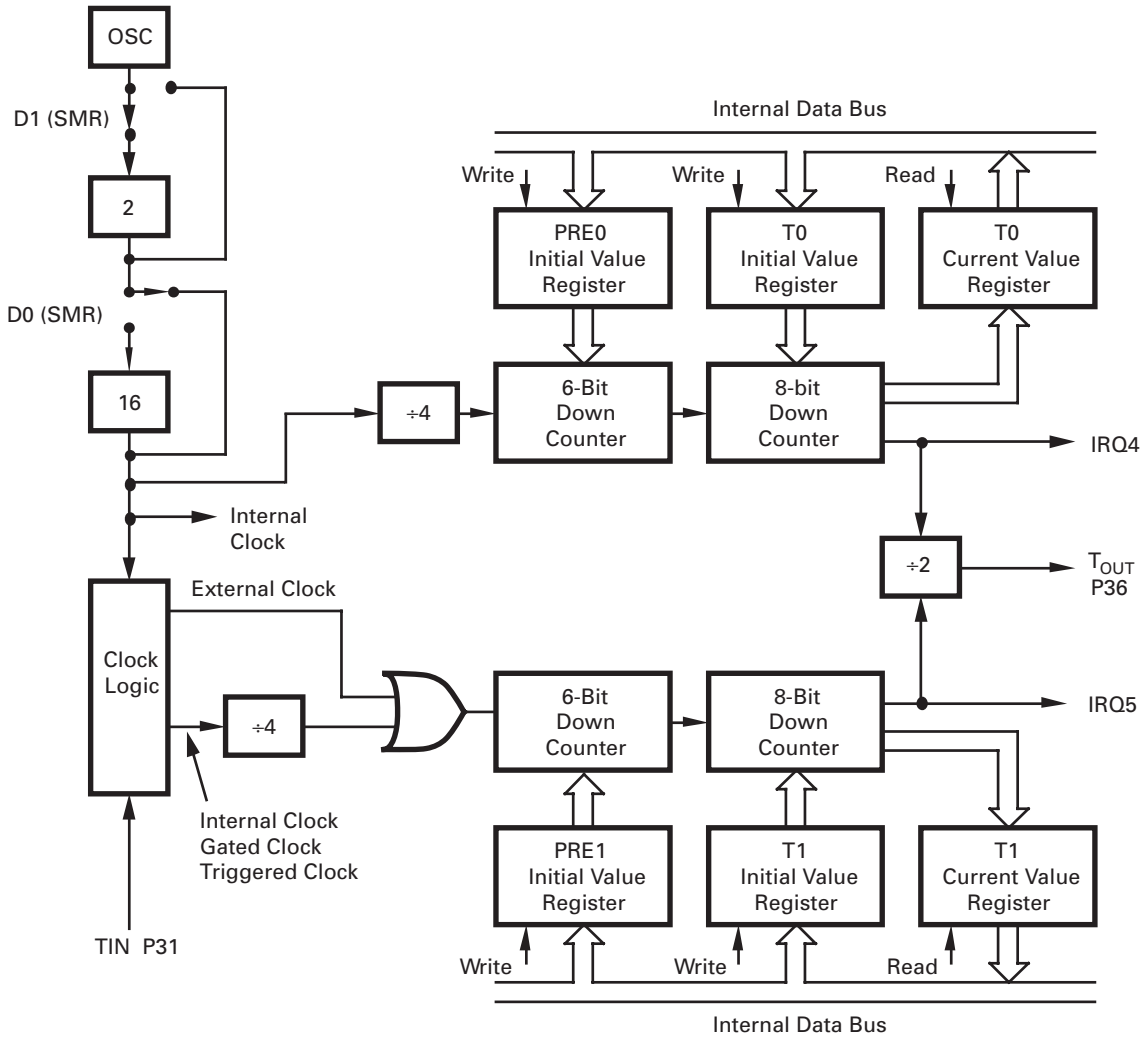


Figure 22. Counter/Timer Block Diagram

Interrupts. The Z8 features six different interrupts from six different sources. These interrupts are maskable, prioritized (Figure 23) and the six sources are divided as follows: four sources are claimed by Port 3 lines P33–P30, and two in counter/timers (Table 11). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

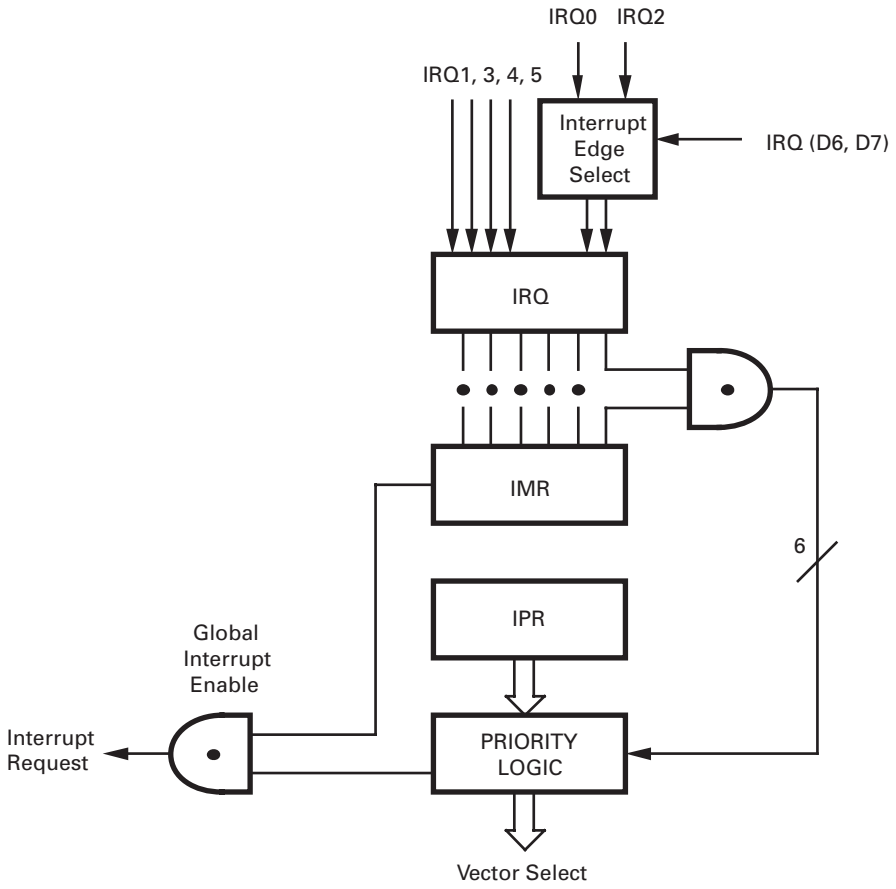


Figure 23. Interrupt Block Diagram

Table 11. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{DAV0}$, IRQ0	0, 1	External (P32), Rise Fall Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Fall Edge Triggered
IRQ2	$\overline{DAV2}$, IRQ2, T_{IN}	4, 5	External (P31), Rise Fall Edge Triggered
IRQ3	UART (ASCI)	6, 7	External (P30), Fall Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle activates when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests require service.

FUNCTIONAL DESCRIPTION (Continued)

An interrupt resulting from AN1 maps to IRQ2, and an interrupt from AN2 maps to IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge-triggered, and are programmable by the user. The software may poll to identify the state of the pin. When in analog mode, the IRQ1 generates by the Stop-Mode Recovery source selected by SMR Reg. bits D4, D3, D2, or SMR2 D1 or D0.

Programming bits for the Interrupt Edge Select are located in the IRQ register (R250), bits D7 and D6. The configuration is indicated in Table 12.

Table 12. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

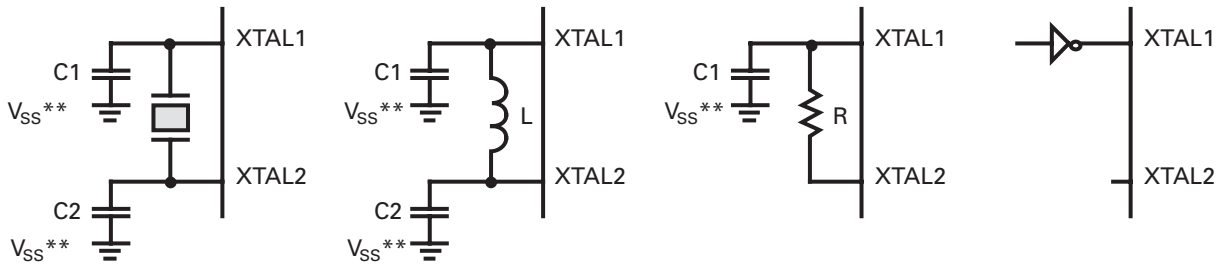
Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z8 on-chip oscillator features a high-gain, parallel-resonant amplifier for connection to a crystal, LC, RC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT-cut, 16 MHz maximum, with a series resistance (RS) of less than or equal to 100 Ohms when counting from 1 MHz to 16 MHz.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to the device Ground pin to reduce ground-noise injection into the oscillator. The RC oscillator option is mask-programmable on the Z8 and is selected by the customer at the time when the ROM code is submitted.

Notes: The RC option is available up to 8 MHz. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 24).

For better noise immunity, the capacitors should be tied directly to the device Ground pin (V_{SS}).



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
f = 8 MHz

LC
C1, C2 = 22 pF

L = 130 uH *
f = 3 MHz *

RC
@ 5V V_{CC} (TYP)

C1 = 33 pF *
R = 1K *
f = 6 MHz *

External Clock

*Preliminary value including pin parasitics
**Device ground pin

Figure 24. Oscillator Configuration

Power-On-Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status.
2. Stop-Mode Recovery (if D5 of SMR = 1).
3. WDT time-out.

The POR time is specified as T_{POR}. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC/LC oscillators).

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts and are either externally or internally generated. An interrupt request must be enabled and executed to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. Therefore, the user must execute a NOP (Op Code = FFH) immediately before the appropriate sleep instruction. For example:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP mode
                  or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation. It also reduces the standby current to 10 µA or less. The STOP mode is terminated by a RESET only, either by WDT time-out, POR, SMR recovery, or external reset. As a result, the processor restarts the application program at address 000Ch. A WDT time-out in STOP mode affects all registers the same as if a Stop-Mode Recovery occurred via a selected Stop-Mode Recovery source except that the POR delay is enabled even if the delay is selected for disable.

Note: If a permanent WDT is selected, the WDT runs in all modes and cannot be stopped or disabled if the onboard RC oscillator is selected to drive the WDT.

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports

FUNCTIONAL DESCRIPTION (Continued)

0, 1, 2, and 3, and low-EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00h (Figure 25).

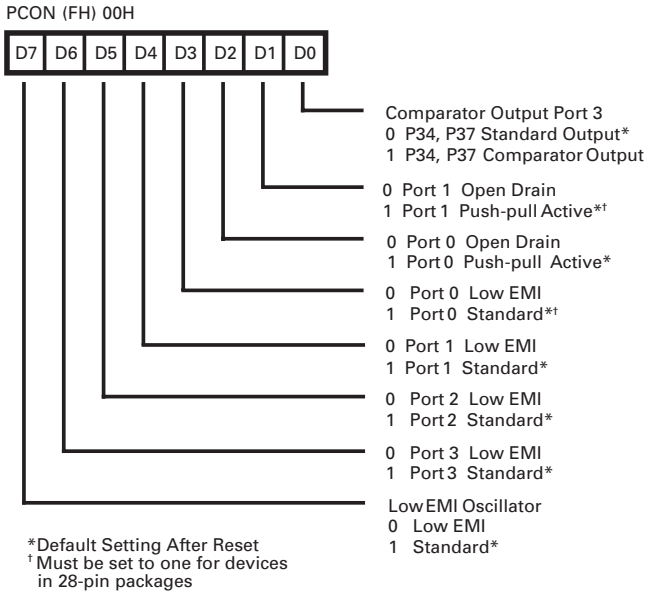


Figure 25. Port Configuration Register (PCON) (WRITE ONLY)

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration. The default value is 0.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1 = 0) or configured as push-pull active by setting this bit (D1 = 1). The default value is 1. The user must set D1 = 1 for devices in 28-pin packages.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2 = 0) or configured as push-pull active by setting this bit (D2 = 1). The default value is 1.

Low-EMI Port 0 (D3). Port 0 can be configured as a low-EMI port by resetting this bit (D3 = 0) or configured as a Standard Port by setting this bit (D3 = 1). The default value is 1.

Low-EMI Port 1 (D4). Port 1 can be configured as a low-EMI port by resetting this bit (D4 = 0) or configured as a Standard Port by setting this bit (D4 = 1). The default value is 1. The user must set D4 = 1 for devices in 28-pin packages.

Note: For emulator, this bit must be set to 1.

Low-EMI Port 2 (D5). Port 2 can be configured as a low-EMI port by resetting this bit (D5 = 0) or configured as a Standard Port by setting this bit (D5 = 1). The default value is 1.

Low-EMI Port 3 (D6). Port 3 can be configured as a low-EMI port by resetting this bit (D6 = 0) or configured as a Standard Port by setting this bit (D6 = 1). The default value is 1.

Low-EMI OSC (D7). This bit of the PCON Register controls the low-EMI noise oscillator. A 1 in this location configures the oscillator, $\overline{DS}$, $\overline{AS}$ and R/$\overline{W}$ with standard drive, while a 0 configures the oscillator, $\overline{DS}$, $\overline{AS}$ and R/$\overline{W}$ with low noise drive. The low-EMI mode reduces the drive of the oscillator (OSC). The default value is 1.

Note: Maximum external clock frequency of 4 MHz when running in the low-EMI oscillator mode.

Low-EMI Emission. The Z8 can be programmed to operate in a low-EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low-EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns (typical)
- Low-EMI output drivers exhibit resistance of 200 Ohms (typical)
- Low-EMI Oscillator
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz–250 ns cycle time, when LOW EMI OSCILLATOR is selected and system clock (SCLK = XTAL, SMR REGISTER BIT D1 = 1)

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figures 26 and 27). All bits are WRITE ONLY, except bit 7, which is READ ONLY. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and RESET by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR register, specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

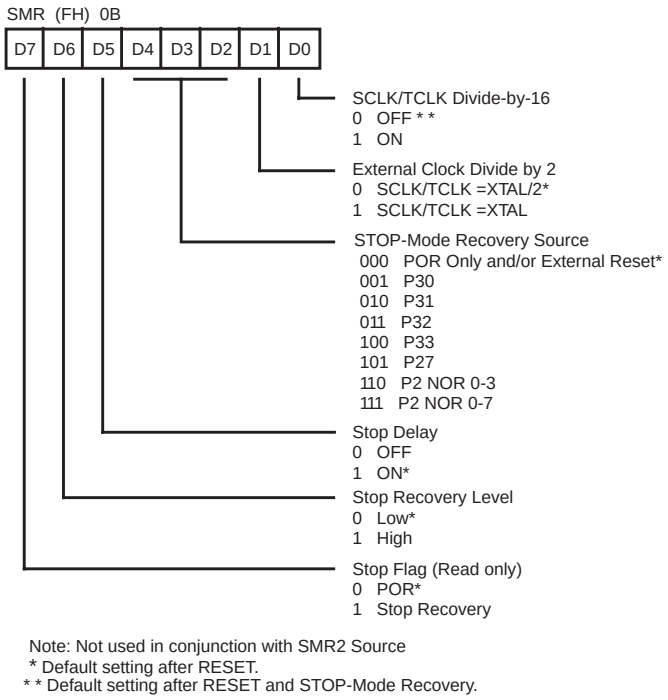


Figure 26. Stop-Mode Recovery Register (WRITE ONLY Except Bit D7, Which Is READ ONLY)

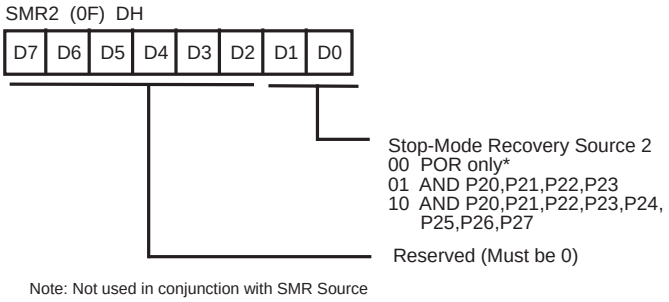


Figure 27. Stop-Mode Recovery Register 2 (0F) DH: WRITE ONLY

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic). This bit is reset to D0 = 0 after a Stop-Mode Recovery.

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided by 2. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1 = 1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is 0. Maximum external clock frequency is 4 MHz when SMR BIT D1 = 1 where SCLK/TCLK = XTAL.

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the STOP recovery (Figure 28 and Table 13). When the Stop-Mode Recovery Sources are selected in this register, then SMR2 register bits D0,D1 must be set to 0.

Note: If the Port 2 pin is configured as an output, this output level is read by the SMR circuitry.

FUNCTIONAL DESCRIPTION (Continued)

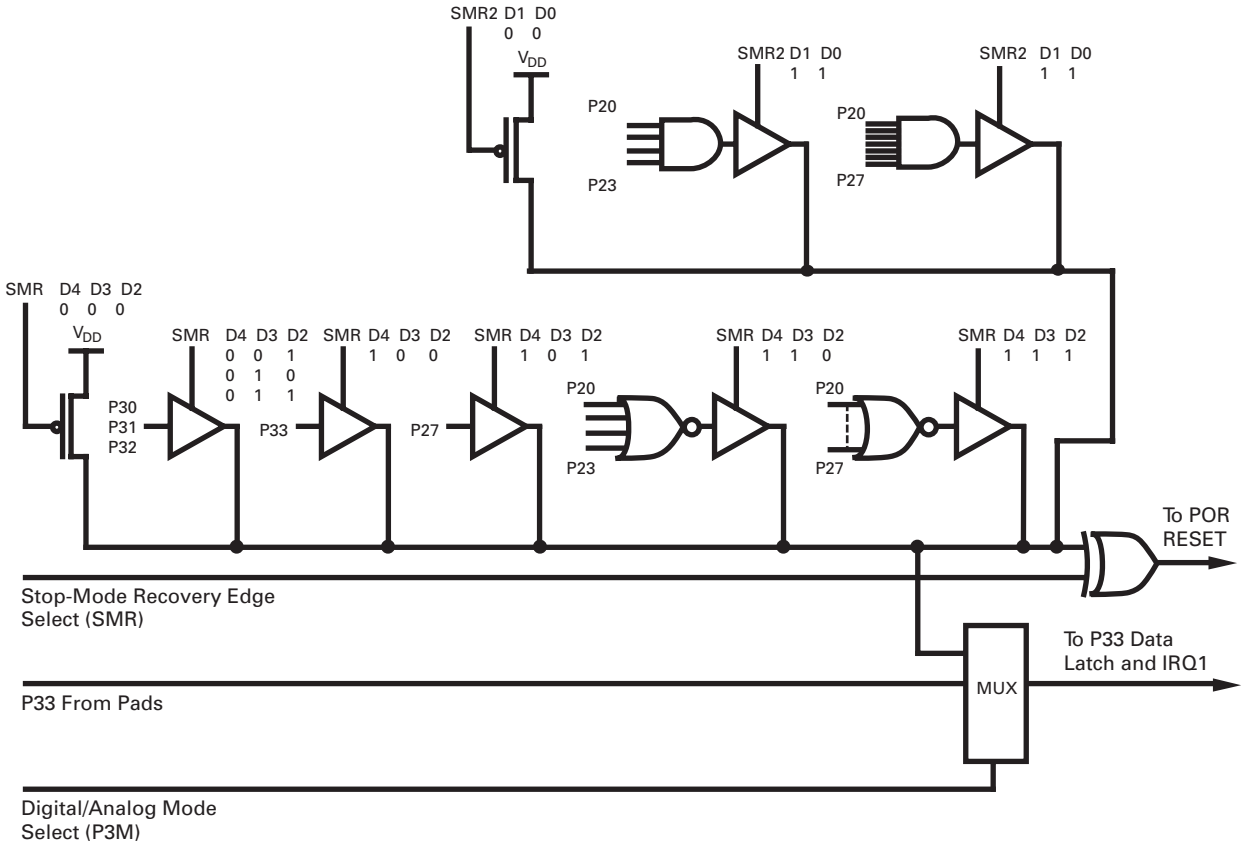


Figure 28. Stop-Mode Recovery Source

Table 13. Stop-Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	P30 transition
0	1	0	P31 transition (not in Analog Mode)
0	1	1	P32 transition (not in Analog Mode)
1	0	0	P33 transition (not in Analog Mode)
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Stop-Mode Recovery Delay Select (D5). This bit, if High, enables the T_{POR} $\overline{\text{RESET}}$ delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the *fast* wake up is selected, the Stop-Mode Recovery source must be kept active for at least 5 TpC.

Stop-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z8 from STOP mode. A 0 indicates low-level recovery. The default is 0 on POR (Figure 28). This bit is used for either SMR or SMR2.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. A 0 in this bit (cold) indicates that the device resets by POR/WDT RESET. A 1 in this bit (warm) indicates that the device awakens by a Stop-Mode Recovery source.

Note: If the Port 2 pin is configured as an output, this output level is read by the SMR2 circuitry.

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register. Bits D2, D3, and D4 must be 0.

Table 14. Stop-Mode Recovery Source

SMR:10 D1	SMR:10 D0	Operation Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an onboard RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 29).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within 64 internal system clocks. After that, the WDTMR is WRITE-protected.

Note: WDT time-out while in STOP mode does not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but the POR delay counter is still enabled even though the SMR stop delay is disabled.

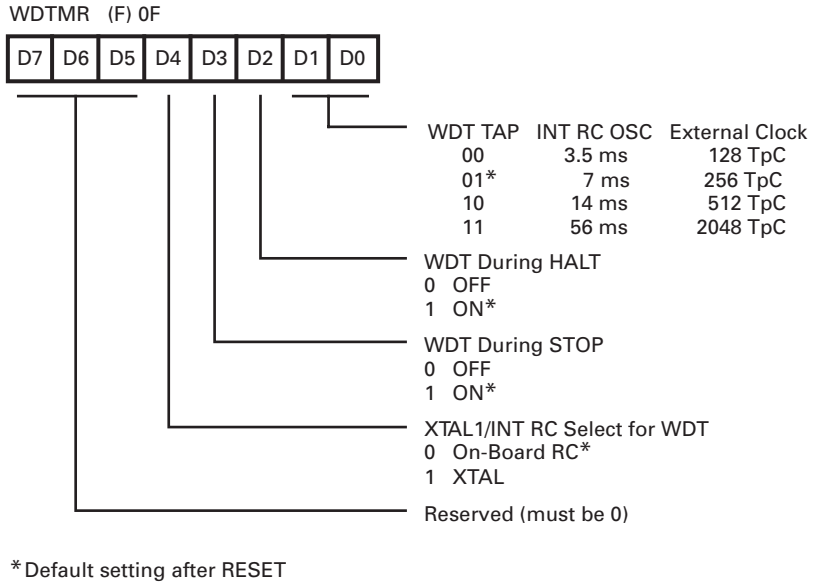


Figure 29. Watch-Dog Timer Mode Register (WRITE ONLY)

WDT Time Select. (D0,D1). Selects the WDT time period and is configured as indicated in Table 15.

Table 15. WDT Time Select

D1	D0	Timeout of Internal RC OSC	Timeout of System Clock
0	0	3.5 ms min	128 SCLK
0	1	7 ms min	256 SCLK
1	0	14 ms min	512 SCLK
1	1	56 ms min	2048 SCLK

Notes:
SCLK = system bus clock cycle.
The default on RESET is 7 ms.
Values provided are for V_{CC} = 5.0V.

FUNCTIONAL DESCRIPTION (Continued)

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Because XTAL clock is stopped during STOP mode, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

Note: If permanent WDT is selected, the WDT runs in all modes and can not be stopped or disabled if the on board RC oscillator is selected as the clock source for WDT.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0 which selects the internal RC oscillator.

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 60 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watch-Dog Reset, or Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH (Figure 30).

Note: The WDT can be permanently enabled (automatically enabled after RESET) through a mask programming option. The option is selected by the customer at the time of ROM code submission. In this mode, WDT is always activated when the device comes out of RESET. Execution of the WDT instruction serves to refresh the WDT time-out period. WDT operation in the HALT and STOP Modes is controlled by WDTMR programming. If this mask option is not selected at the time of ROM code submission, the WDT must be activated by the user through the WDT instruction and is always disabled by any reset to the device.

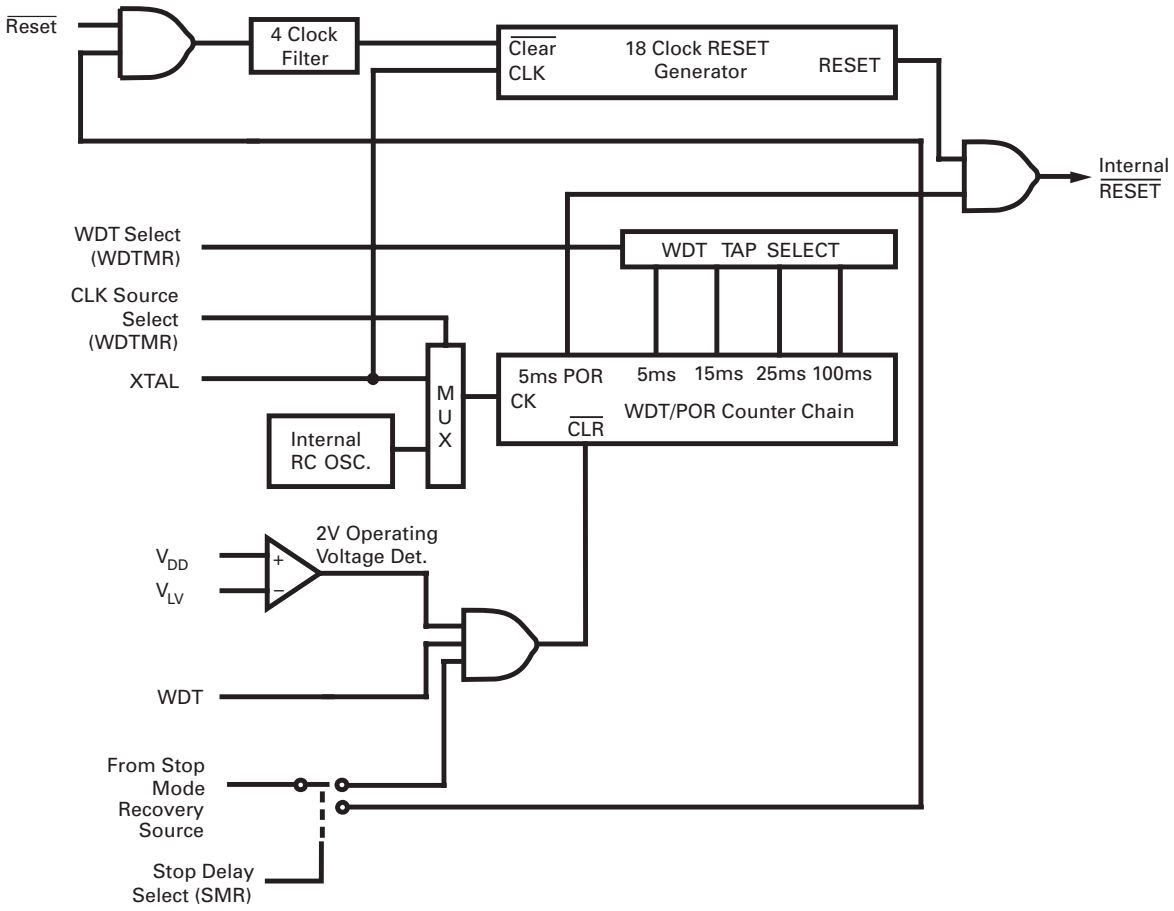


Figure 30. Resets and WDT

Low Voltage Protection. An onboard Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. RESET is globally driven if V_{CC} is below the specified voltage (Low Voltage Protection). The minimum operating voltage is varying with the temperature and operating frequency, while the Low Voltage Protection (V_{LV}) varies with temperature only.

The Low Voltage Protection trip voltage (V_{LV}) is less than 3V and more than 1.4V under the following conditions.

Table 16. Maximum (V_{LV}) Conditions:

Case 1:	T_A = –40ºC, +105ºC, Internal Clock Frequency equal or less than 4 MHz
Case 2:	T_A = –40ºC, +85ºC, Internal Clock Frequency equal or less than 6 MHz

Note: The internal clock frequency relationship to the XTAL clock is dependent on SMR BIT 0 1 setting.

The device functions normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Low Voltage Protection trip point (V_{LV}) is reached, for the temperatures and operating frequencies in Case 1 and Case 2, above. The device is guaranteed to function normally at supply voltages above the Low Voltage Protection trip point. The actual Low Voltage Protection trip point is a function of temperature and process parameters (Figure 36).

ASYNCHRONOUS SERIAL COMMUNICATIONS INTERFACE (ASCI)

Key features of the ASCI include:

- Full-duplex operation
- Programmable data format
- 7 or 8 data bits with optional ninth bit for multiprocessor communication
- P30 and P37 can be used as general-purpose I/O as long as the ASCI channels are disabled
- One or two STOP bits
- Odd, even or no parity
- Programmable interrupt conditions
- Four level data/status FIFOs for the receiver
- Receive parity, framing and overrun error detection
- Break detection and generation

Transmit Data Register. Data written to the ASCI Transmit Data Register (TDR) is transferred to the Transmit Shift Register(TSR) as soon as the TSR is empty. Data can be written while the TSR is shifting out the previous byte of data, providing double buffering for the transmit data. The TDR is READ- and WRITE-accessible. Reading from the TDR does not affect the ASCI data transmit operation currently in progress.

Transmit Shift Register. When the ASCI Transmit Shift Register (TSR) receives data from the ASCI Transmit Data Register, the data is shifted out to the TX (P37) pin. When transmission is completed, the next byte (if available) is automatically loaded from the TDR into the TSR and the next transmission starts. If no data is available for transmission, the TSR idles at a continuous High level. This register is not program-accessible.

Receive Shift Register. When the RE bit is set in the CNTLA register, the RX (P30) pin is monitored for a Low. One-half bit-time after a Low is sensed at RX, the ASCI samples RX again. If RX goes back to High, the ASCI ignores the previous Low and resumes looking for a new Low, but if RX is still Low, it considers RX a START bit and proceeds to clock in the data based upon the selected baud rate. The number of data bits, parity, multiprocessor and STOP bits are selected by the MOD2, MOD1, MOD0 and multiprocessor mode (MP) bits in the CNTLA and CNTLB registers.

After the data is received, the appropriate MP, parity and one STOP bit are checked. Data and any errors are clocked into the receive data and status FIFO during the STOP bit if there is an empty position available. Interrupts and Receive Data Register Full Flag also goes active during this time. If there is no space in the FIFO at the time that the RSR attempts to transfer the received data into it, an overrun error occurs.

Receive Data FIFO. When a complete incoming data byte is assembled in the RSR, it is automatically transferred to the 4-byte FIFO, which serves to reduce the incidence of overrun errors. The top (oldest) character in the FIFO (if any) can be read via the Receive Data Register (RDR).

The next incoming data byte can be shifted into the RSR while the FIFO is full, thus providing an additional level of buffering. However, an overrun occurs if the receive FIFO is still full when the receiver completes assembly of that character and is ready to transfer it to the FIFO. If this situation occurs, the overrun error bit associated with the previous byte in the FIFO is set. The latest data byte is not transferred from the shift register to the FIFO in this case, and is lost. When an overrun occurs, the receiver does not place any further data in the FIFO until the most recent good byte received arrives at the top of the FIFO and sets the Overrun latch, and software then clears the Overrun latch by a WRITE of 0 to the EFR bit. Assembly of bytes continues in the shift register, but this data is ignored until the byte with the overrun error reaches the top of the FIFO and the status is cleared.

When a break occurs (defined as a framing error with the data equal to all zeros), the all-zero byte with its associated error bits are transferred to the FIFO if it is not full and the Break Detect bit in the ASEXT register is set. If the FIFO is full, an overrun is generated, but the break, framing error and data are not transferred to the FIFO. Any time a break is detected, the receiver does not receive any more data until the RX pin returns to a high state.

If the channel is set in multiprocessor mode and the MPE bit of the CNTLA register is set to 1,then break, errors and data are ignored unless the MP bit in the received character is a 1. The two conditions listed above could cause the missing of a break condition if the FIFO is full and the break occurs or if the MP bit in the transmission is not a one with the conditions specified above.

ASCI Status FIFO/Registers. This FIFO contains Parity Error, Framing Error, RX Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCI status register, which also provides several other, non-FIFOed status conditions.

The outputs of the error FIFO go to the set inputs of software-accessible error latches in the status register. Writing

a 0 to the EFR bit in CNTLA is the only way to clear these latches. In other words, when an error bit reaches the top of the FIFO, it sets an error latch. If the FIFO contains more data and the software reads the next byte out of the FIFO, the error latch remains set until the software writes a 0 to the EFR bit. The error bits are cumulative, so if additional errors are in the FIFO they set any unset error latches as they reach the top.

Baud Rate Generator. The baud rate generator features two modes. The first provides a dual set of fixed clock divide ratios as defined in CNTLB. In the second mode, the BRG is configured as a sixteen-bit down counter that divides the processor clock by the value in a software accessible, sixteen-bit, time-constant register. As a result, virtually any frequency can be created by appropriately selecting the main processor clock frequency. The BRG can also be disabled in favor of the SCLK.

The Receiver and Transmitter subsequently divide the output of the Baud rate Generator (or the signal from the CLK pin) by 1, 16 or 64 under the control of the DR bit in the CNTLB register and the X1 bit in the ASCI Extension Control Register (ASEXT).

RESET. During RESET, the ASCI is forced to the following conditions:

- FIFO Empty
- All Error Bits Cleared (including those in the FIFO)
- Receive Enable Cleared (CNTLA BIT 6 = 0)
- Transmit Enable Cleared (CNTLA BIT 5 = 0)

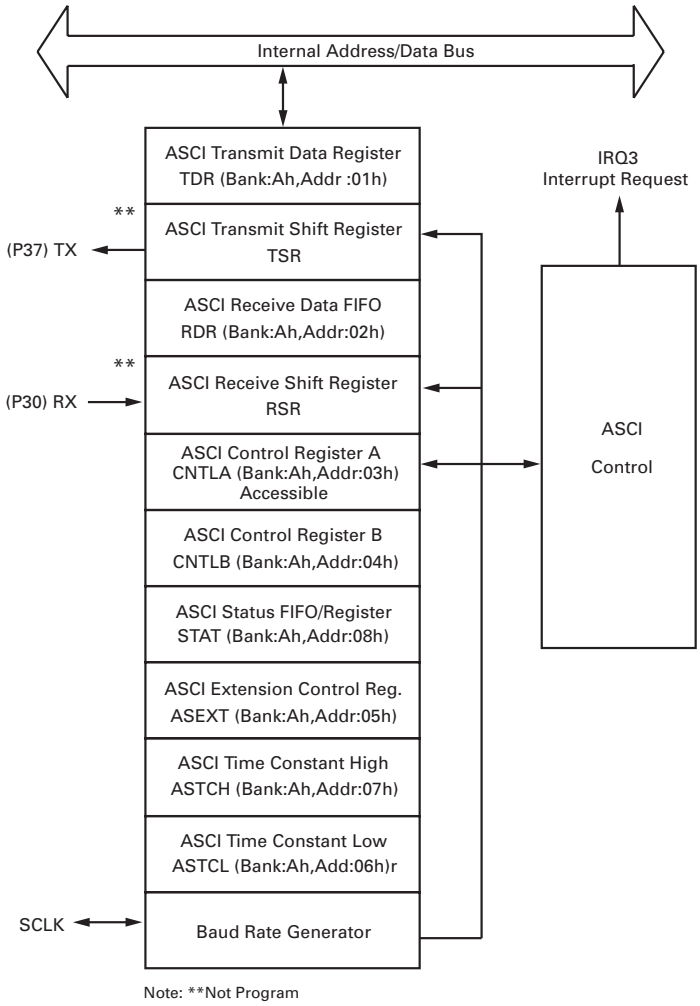


Figure 31. ASCI Interface Diagram

INTERRUPTS

The ASCI channel generates one interrupt (IRQ3) from two sources of interrupts: a receiver and a transmitter. In addition, there are several conditions that may cause these interrupts to trigger. Figure 32 illustrates the different conditions for each interrupt source enabled under program control.

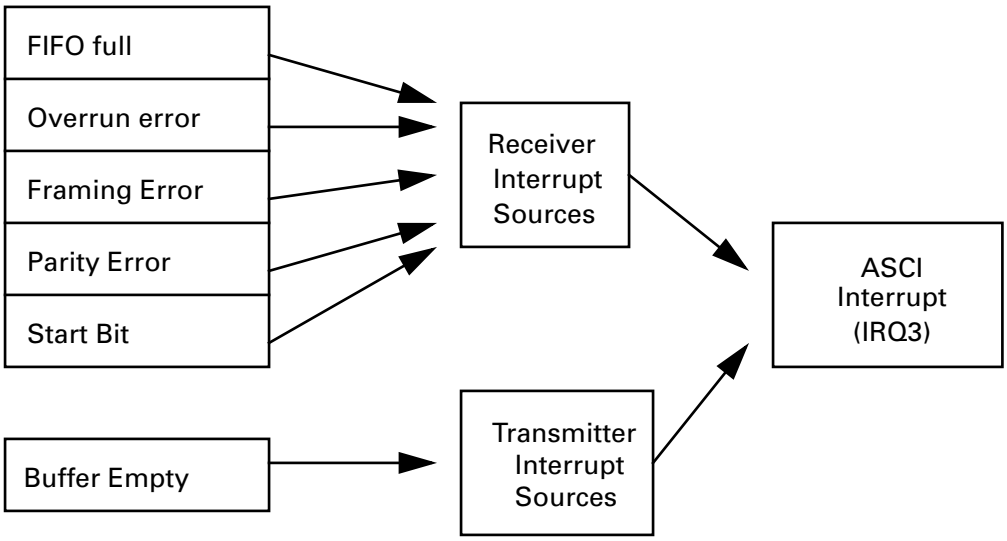


Figure 32. ASCI Interrupt Conditions and Sources

EXPANDED REGISTER GROUP (A)

			B7	B6	B5	B4	B3	B2	B1	B0
	%(A)0F	RESERVED								
	%(A)0E	RESERVED								
	%(A)0D	RESERVED								
	%(A)0C	RESERVED								
	%(A)0B	RESERVED								
	%(A)0A	RESERVED								
	%(A)09	GEN PURPOSE	u	u	u	u	u	u	u	u
*	%(A)08	STAT	0	0	0	0	0	0	1	0
*	%(A)07	ASTCH	1	1	1	1	1	1	1	1
*	%(A)06	ASTCL	1	1	1	1	1	1	1	1
*	%(A)05	ASEXT	0	0	0	0	0	0	0	0
*	%(A)04	CNTLB	0	0	0	0	0	1	1	1
*	%(A)03	CNTLA	0	0	0	1	0	0	0	0
*	%(A)02	RDR	u	u	u	u	u	u	u	u
*	%(A)01	TDR	u	u	u	u	u	u	u	u
	%(A)00	RESERVED								

* Not reset with a STOP-Mode Recovery.

Figure 33. Expanded Register Group (A) Registers

ASCI TRANSMIT DATA REGISTER (TDR)

(%(A)01H: READ/WRITE)

Table 17. TDR Register Bit Functions

Bit	7	6	5	4	3	2	1	0
R	Transmit Data							
W								
Reset	U	U	U	U	U	U	U	U

Data written to the ASCI Transmit Data Register (TDR) is transferred to the Transmit Shift Register (TSR) as soon as the TSR is empty. The TSR is not not software-accessible. The ASCI transmitter is double-buffered so data can be written to the TDR while the TSR is shifting out the previous byte. Data can be written into and read out of the TDR. When the TDR is read, the data transmit operation is not affected.

ASCI RECEIVE DATA REGISTER (RDR)

(%(A)02H: READ/WRITE)

Table 18. RDR Register Bit Functions

Bit	7	6	5	4	3	2	1	0
R	Receive Data							
W								
Reset	U	U	U	U	U	U	U	U

When a complete incoming data byte is assembled in the Receive Shift Register (RSR), it is automatically transferred to the highest available location in the Receive Data FIFO. The Receive Data Register (RDR) is the highest location in the Receive Data FIFO. The RDRF bit in the STAT register is set when one or more bytes is available from the FIFO. The FIFO status for the character in the RDR is available in the STAT register via bits 6, 5 and 4. STAT should be read before reading the RDR. The data in both FIFO locations is *popped* when the character is read from the RDR.

ASCI CONTROL REGISTER A (CNTLA)

(%(A)03H: READ/WRITE)

Table 19. CNTLA Register Bit Functions

Bit	7	6	5	4	3	2	1	0
R	Multiprocessor Enable (MPE)	Receiver Enable (RE)	Transmitter Enable (TE)	Reserved	Multiprocessor Bit Received (MPBR)	MOD2	MOD1	MOD0
W					Error Flag Receive (EFR)	Mode Select		
Reset	0	0	0	1	0	0	0	0

Bit 7 is the Multiprocessor Enable

The ASCI features a multiprocessor communication mode that utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP bit in the corresponding register is set to 1. If multiprocessor mode is not selected (MP bit in CNTLB = 0), multiprocessor enable (MPE) has no effect. If multiprocessor mode is selected (MP bit in CNTLB = 1), MPE enables or disables the *wake-up* feature as follows. If MPE is set to 1, only received bytes in which the multiprocessor bit (MPB) = 1 are treated as valid data characters and loaded into the receiver FIFO with corresponding error flags in the status FIFO. Bytes with MPB = 0 are ignored by the ASCI. If MPE is reset to 0, all bytes are received by the ASCI, regardless of the state of the MPB data bit.

Bit 6 is the Receiver Enable

When Receiver Enable(RE) is set to 1,the ASCI receiver is enabled. When RE is reset to 0, the receiver is disabled and any receive operation in progress is aborted. However, the previous contents of the receiver data and status FIFO are not affected.

Bit 5 is the Transmitter Enable

When Transmitter Enable(TE) is set to 1,the ASCI transmitter is enabled. When TE is reset to 0, the transmitter is disabled and any transmit operation in progress is aborted. However, the previous contents of the transmitter data register and the TDRE flag are not affected.

Bit 4 is Reserved

Bit 3 is the Multiprocessor Bit Receive (Read only)

When multiprocessor mode is enabled (MP in CNTLB = 1), this bit, when read, contains the value of the MPB bit for the data byte currently available at the Receive Data Register (the *top* of the receiver FIFO).

Bit 3 is the Error Flag Reset (WRITE ONLY)

When written to 0, the error flags (OVRN, FE; PE in STAT and BRK in ASEXT) are cleared to 0. This command self-resets, and as a result, writing EFR to a 1 is not required.

Bits 2–0 are the ASCI Data Format Mode 2,1,0

These bits program the ASCI data format.

Table 20. Format Mode Control Bits

Bit	Name	Function	Bit = 0	Bit = 1
2	MOD2	Number of Data Bits	7	8
1	MOD1	Parity Enabled	No Parity	With Parity
0	MOD0	Number of Stop Bits	1	2

If MOD1 = 1, parity is checked on received data and a parity bit is appended to the data bits in the transmitted data. Parity Even/Odd (PEO) in CNTLB selects even or odd parity.

The ASCI serial data format is illustrated in Figure 34.

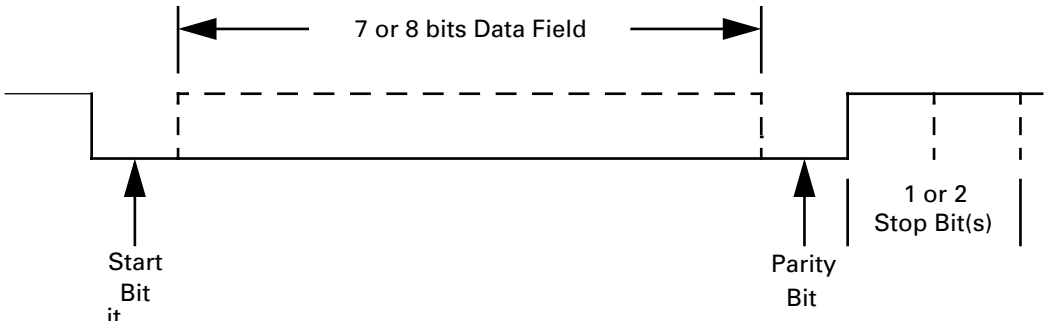


Figure 34. ASCI Serial Data Format

ASCI CONTROL REGISTER B (CNTLB)

(%(A)04H: READ/WRITE)

Table 21. CNTLB Register Bit Functions

Bit	7	6	5	4	3	2	1	0
R	Multiprocessor Bit Transmitter (MPBT)	Multiprocessor Mode (MP)		Parity Even/Odd (PEO)	Divide Ratio (DR)	SS2	SS1	SS0
W			Prescale (PR)			Clock Source and Speed		
Reset	0	0	0	0	0	1	1	1

BIT 7 is the Multiprocessor Bit Transmit

When multiprocessor format is selected (MP BIT = 1), Multiprocessor Bit Transmit (MPBT) is used to specify the MPB data bit for transmission. If MPBT = 1, then a 1 is transmitted in the MPB bit position. If MPBT = 0, a 0 is transmitted.

BIT 6 is the Multiprocessor Mode

When Multiprocessor Mode (MP) is set to 1, the serial data format is configured for multiprocessor mode, adding a bit position whose value is specified in MPBT immediately after the specified number of data bits and preceding the specified number of STOP bits.

Note: The multiprocessor format does not provide parity. The serial data format while in MP mode is illustrated in Figure 35.

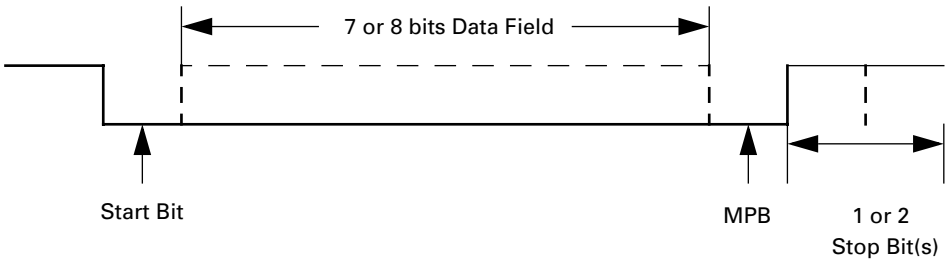


Figure 35. MP Mode Serial Data Format

If MP = 0, the data format is based on MOD2–0 in CNTLA and may include parity.

Bit 5 is the BRG Prescaler

The Prescale bit specifies the baud rate generator prescale factor when using the SS2–0 bits to define the ASCI baud rate (BRG MODE = 0). Writing a 0 to this bit sets the BRG Prescaler to divide by 10. Setting this bit to a 1 sets the BRG Prescaler to divide by 30. See the Baud Rate Generation Summary for more information on setting the ASCI baud rate.

Bit 4 is the Parity Even/Odd

Parity Even/Odd (PEO) controls the parity bit transmitted on the serial output and the parity check on the serial input. If PEO is cleared to 0, even parity is transmitted and checked If PEO is set to 1, odd parity is transmitted and checked.

Bit 3 is the Divide Ratio

The Divide Ratio bit specifies the divider used to obtain the baud rate from the data sampling clock when using the SS2–0 bits to define the ASCI baud rate (BRG MODE = 0). If DR is 0, then DIVIDE-BY-16 is used. If DR is set to a 1, then DIVIDE-BY-64 is used. See the Baud Rate Generation Summary for more information on setting the ASCI baud rate.

DR	Sampling Clock
0	Divide by 16
1	Divide by 64

Bit 2,1 are the Clock Source and Speed Select

When the BRG mode bit in the ASEXT register is set to 0, these 3 bits, along with DR and PR in this register define the ASCI baud rate. Bits 2, 1 and 0 specify a power-of-two divider of the SCLK as defined in Table 22. These bits should never be set to all 1s or erratic results may occur. See the Baud Rate Generation Summary for more information on setting the ASCI baud rate.

Table 22. Clock Source and Speed Bits

SS2	SS1	SS0	Divider (DIV)
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	Reserved

ASCI EXTENSION CONTROL REGISTER (ASEXT)

(%(A)05H: READ/WRITE)

Table 23. ASEXT Register Bit Functions

Bit	7	6	5	4	3	2	1	0
R	RX State (RX)	Reserved	Reserved	Reserved (must be 0)	BRG Mode (BRGM)	RX Interrupt on Start Bit (RIS)	Break Detect (BD)	Send Break (SB)
W								
Reset	P30	0	0	0	0	0	0	0

BIT 7 is the RX State (READ ONLY)

Provides the real time state of RX, the channel's receive data input pin—P30.

BIT 6 is Reserved

When read, this bit reflects the default value 0. When WRITE, this bit is ignored.

Bit 5 is Reserved

When read, this bit reflects the default value 0. When WRITE, this bit is ignored.

Bit 4 is the X1 Bit Clock

Reserved—must be set to 0 or erratic results may occur.

Bit 3 is the BRG Mode

When this bit is set to a 1, the ASCI's baud rate is set by the 16-bit programmable divider programmed in ASCI Time Constant High (ASTH) and ASCI Time Constant Low (ASTL). If this bit is set to a 0, the baud rate is defined by the PR bit, the DR bit, and the SS2–0 bits in the CNTLB register. In either case, the source for the baud rate generator is the SCLK. See the Baud Rate Generation Summary for more information on setting the ASCI baud rate.

Bit 2 is the Rx Interrupt on Start

If software sets this bit to 1,a receive interrupt is requested (in a combinatorial fashion) when a START bit is detected on RX. Such a receive interrupt is always followed by the setting of RDRF in the middle of the STOP bit. This interrupt request must be cleared by writing this bit back to a 0. Writing a 1 to this bit has no effect. One function of this feature is to wake the part from Sleep mode when a character arrives, so that the ASCI receives clocking with which to process the character. Another function is to ensure that the associated interrupt service routine is activated in time to sense the setting of RDRF in the status register, and to start a timer for baud rate measurement at that time.

Bit 1 is the Break Detect (READ ONLY)

This status bit is set to a 1 when a Break is detected, defined as a framing error with the data bits all equal to 0. The all-zero byte with its associated error bits are transferred to the FIFO if it is not full. If the FIFO is full, an overrun is generated, but the break, framing error and data are not transferred to the FIFO. Any time a break is detected, the receiver do not receive any more data until the RX pin returns to a High state. When set, this bit remains set until it is cleared by writing a 0 to the EFR bit in the CNTLA register.

Bit 0 is the Send Break

Setting this bit to a 1 forces the channel's transmitter data output pin, TX, to a Low for as long as it remains set. Before starting the break, any character(s) in the TSR and in the TDR are completely transmitted. If a character is loaded into the TDR while a break is being generated, that character is held until the break is terminated and transmitted.

ASCI TIME CONSTANT REGISTER (ASTL)

(%(A)06H: READ/WRITE)

Table 24. ASTL Register Bit Functions

Bit	7	6	5	4	3	2	1	0
R	ASCI Time Constant Low							
W								
Reset	1	1	1	1	1	1	1	1

ASCI TIME CONSTANT REGISTER (ASTH)

(%(A)07H: READ/WRITE)

Table 25. ASTH Register Bit Functions

Bit	7	6	5	4	3	2	1	0
R	ASCI Time Constant High							
W								
Reset	1	1	1	1	1	1	1	1

The ASTL and ASTH registers are only used when the BRG mode bit in the ASEXT register is set to a 1. These two 8-bit registers form a 16-bit counter with a flip-flop logic circuit (DIVIDE-BY-2) on the output so that the final BRG output is symmetrical. The values written to these registers determine the time constant from which the baud rate is generated.

ASCI STATUS REGISTER (STAT)

(%(A)08H: READ/WRITE)

Table 26. ASCI Status Register (STAT)

Bit	7	6	5	4	3	2	1	0
R	Receive Data Register Full (RDRF)	Overrun Error (OE)	Parity Error (PE)	Framing Error (FE)	Receiver Interrupt Enable (RIE)	Reserved	Transmit Data Register Empty TDRE)	Transmitter Interrupt Enable (TIE)
W								
Reset	0	0	0	0	0	0	0	0

BIT 7 is the Receive Data Register Full

RDRF is set to 1 when the receiver transfers a character from the RSR into an empty Rx FIFO.

Note: If a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO.

When there is more than one character in the FIFO, and software reads a character, RDRF either remains set or is cleared and immediately set again. RDRF is cleared to 0 when the FIFO becomes empty after reading the RDR and during Power-On Reset.

Bit 6 is the Overrun Error

An overrun occurs if the receive FIFO is still full when the receiver completes assembly of a character and is ready to transfer it to the FIFO. If this situation occurs, the overrun error bit associated with the previous byte in the FIFO is set. In this case, the latest data byte is not transferred from the shift register to the FIFO and is lost.

When an overrun occurs, the receiver does not place any further data in the FIFO until the most recent good byte received (the byte with the associated overrun error bit set) moves to the top of the FIFO and sets the Overrun latch, and software then clears the Overrun latch. Assembly of bytes continues in the shift register, but this data is ignored until the byte with the overrun error reaches the top of the FIFO and the status is cleared. When set, the bit remains set until it is cleared by writing a 0 to the EFR bit in the CNTLA register. The bit is also cleared during Power-On Reset.

Bit 5 is the Parity Error

A parity error is detected when parity generation and checking is enabled by the MOD1 bit in the CNTLA register and a character has been assembled in which the parity does not match that specified by the PEO bit in CNTLB.

Note: PE is FIFOed and the error bit is not actually set until the associated data becomes available for reading in the RDR.

When set, the bit remains set until it is cleared by writing a 0 to the EFT bit in the CNTLA register. The bit is cleared at Power-On Reset.

Bit 4 is the Framing Error

A framing error is detected when the STOP bit of a character is sampled as a 0 (space). Like PE, FE is FIFOed and the error bit is not actually set until the associated data becomes available for reading in the RDR. When set, the bit remains set until it is cleared by writing a 0 to the EFR bit in the CNTLA register. The bit is cleared at Power-On Reset.

Bit 3 is the Receiver Interrupt Enable

RIE should be set to a 1 to enable ASCI receive interrupt requests. An interrupt (IRQ3) is generated when RDRF (bit 7 of the STAT register) is a 1. A receive interrupt is also generated if this bit is set to a 1, bit 2 of the ASEXT register (RX interrupt on the START bit) is set to a 1, and a START bit is detected by the receiver.

Bit 2 is Reserved

When read, this bit reflects the default value 0. When WRITE, this bit is ignored.

Bit 1 is the Transmit Data Register Empty

TDRE = 1 indicates that the Transmit Data Register (TDR) is empty and that the next data byte to be transmitted can be written into the TDR. TDRE is cleared to 0 after the byte is written to TDR, until the ASCI transfers the byte from the TDR to the Transmit Shift Register (TSR), and then TDRE is again set to 1. TDRE is set to 1 at Power-On Reset.

Bit 0 is the Transmit Interrupt Enable

TIE should be set to a 1 to enable ASCI transmit interrupt requests. An interrupt (IRQ3) is generated when TDRE (bit 1 of the STAT register) is a 1. TIE is cleared to 0 at Power-On Reset.

An anomaly exists that requires setting of the RIE bit to allow the generation of transmit interrupts. If RIE is not set, transmit interrupts are not generated, even if TIE is set. See Precautions.

Baud Rate Generation Summary

The application can select between one of two baud rate generators for the ASCI. If the BRG Mode bit in the ASEXT register is set to a 0, the SS2,1,0 bits, the DR, bit and the PR bit in CNTLB are used to select the baud rate. If the BRG Mode bit is set to a 1, the ASTL and ASTH registers are used to select the baud rate.

The following formulas are used to calculate the baud rate from the two baud rate generators:

If BRG mode = 0:

$$\text{Baud Rate} = \frac{\text{SCLK}}{(10 + 20 \times \text{PS}) \times \text{DIV} \times \text{Divide Ratio}}$$

Where:

1. SCLK is the system clock.
2. PS = 1 or 0 and is bit 5 of CNTLB.
3. DIV = 1, 2, 4, 8, 16, 32 or 64 as reflected by SS2–0 in CNTLB.
4. DIVIDE RATIO = 16 or 64, as defined by DR in CNTLB.

If BRG mode = 1:

$$\text{Baud Rate} = \frac{\text{SCLK}}{(2 \times (\text{TC} + 2) \times \text{Divide Ratio}}$$

or

$$\text{TC} = \frac{\text{SCLK}}{2 \times \text{Baud Rate} \times \text{Divide Ratio}} - 2$$

Where:

1. SCLK is the system clock.
2. TC is the 16-bit value programmed into ASTL and ASTH.
3. DIVIDE RATIO = 16 or 64, as defined by DR in CNTLB.
4. Baud Rate is the desired baud rate.

ASCI STATUS REGISTER (STAT) (Continued)

Table 27. Baud Rate List (BRG Mode = 0)

Prescaler		Sampling Rate		Baud Rate					Example Baud Rate (bps)		
PS	Divide Ratio	DR	Rate	SS2	SS1	SS0	Divide Ratio	General Divide Ratio	SCLK = 6.144 MHz	SCLK = 4.608 MHz	SCLK = 3.072 MHz
0	SCLK ÷ 10	0	16	0	0	0	÷1	SCLK ÷ 160	38400		19200
				0	0	1	÷2	SCLK ÷ 320	19200		9600
				0	1	0	÷4	SCLK ÷ 640	9600		4800
				0	1	1	÷8	SCLK ÷ 1280	4800		2400
				1	0	0	÷16	SCLK ÷ 2560	2400		1200
				1	0	1	÷32	SCLK ÷ 5120	1200		600
				1	1	0	÷64	SCLK ÷ 10240	600		300
		1	64	0	0	0	÷1	SCLK ÷ 640	9600		4800
				0	0	1	÷2	SCLK ÷ 1280	4800		2400
				0	1	0	÷4	SCLK ÷ 2560	2400		1200
				0	1	1	÷8	SCLK ÷ 5120	1200		600
				1	0	0	÷16	SCLK ÷ 10240	600		300
				1	0	1	÷32	SCLK ÷ 20480	300		150
				1	1	0	÷64	SCLK ÷ 40960	150		75
1	SCLK ÷ 30	0	16	0	0	0	÷1	SCLK ÷ 480		4800	
				0	0	1	÷2	SCLK ÷ 960		2400	
				0	1	0	÷4	SCLK ÷ 1920		1200	
				0	1	1	÷8	SCLK ÷ 3840		600	
				1	0	0	÷16	SCLK ÷ 7680		300	
				1	0	1	÷32	SCLK ÷ 15360		150	
				1	1	0	÷64	SCLK ÷ 30720		75	
		1	64	0	0	0	÷1	SCLK ÷ 1920		2400	
				0	0	1	÷2	SCLK ÷ 3840		1200	
				0	1	0	÷4	SCLK ÷ 7680		600	
				0	1	1	÷8	SCLK ÷ 15360		300	
				1	0	0	÷16	SCLK ÷ 30720		150	
				1	0	1	÷32	SCLK ÷ 61440		75	
				1	1	0	÷64	SCLK ÷ 122880		37.5	

LOW VOLTAGE PROTECTION

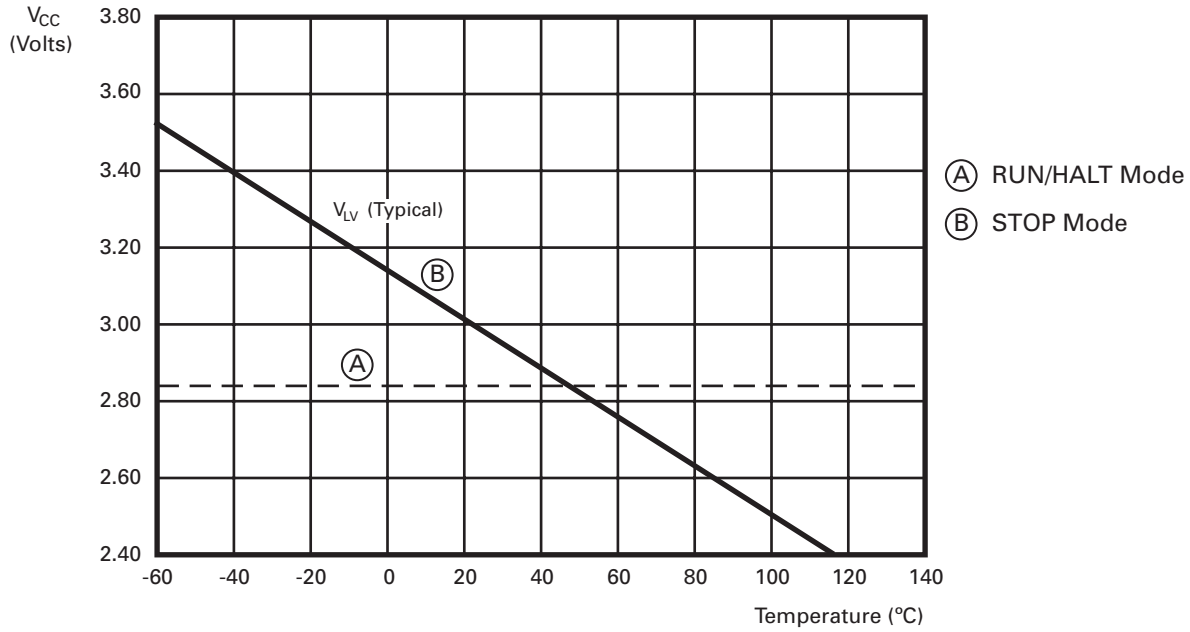


Figure 36. Typical Low Voltage Protection vs. Temperature

MASK OPTIONS

Below is an example of the ROM mask bit option selection for this product.

Options	Option Selections	
ROM Protect	Disable ROM Protect	Enable ROM Protect
RAM Protect	Disable RAM Protect	Enable RAM Protect
System Clock Source	RC Oscillator Enable	Crystal/Other Clock Source
Oscillator Operational Mode	Normal High-Frequency Operation Enabled	32-kHz Crystal Operation Enabled (Limits High-Frequency Operation)
WDT Mode	WDT Enabled by Software Only	WDT Enabled Automatically After RESET
Auto Latch Mode	Disable Auto Latches	Enable Auto Latches
Port 0 Pull-Ups	Disable Pull-Ups	Enable Pull-Ups
Port 1 Pull-Ups	Disable Pull-Ups	Enable Pull-Ups
Port 2 Pull-Ups	Disable Pull-Ups	Enable Pull-Ups

ROM Protect. Selecting the DISABLE ROM PROTECT option READs the software program that is in the program memory using ZiLOG's internal factory test mode. However, none of the standard methods for reading or verifying the code in the microcontroller uses an EPROM programmer. With this option disabled, ZiLOG is able to fully test the ROM memory and provides its standard warranty for the part. Selecting the ENABLE ROM PROTECT option negates the possibility of reading the code out of the part using a tester, programmer, or any other standard method. ZiLOG will be unable to test the ROM memory at any time prior to customer delivery.

The ROM PROTECT option bit only affects the ability to read the code and does not affect the operation of the part in an application. If the ROM PROTECT option is disabled, ZiLOG tests the part for ROM fallout and parts which fail are not shipped to the customer. When the ROM PROTECT option is enabled, ZiLOG cannot perform these tests on the ROM. When ROM PROTECT is enabled, except for the improper transfer of the code by ZiLOG, all ROM memory software errors shall be the responsibility of the Buyer and ZiLOG shall have no obligation to repair or replace product containing software errors. Selecting the ENABLE ROM PROTECT option waives all warranties of ZiLOG, expressed or implied, on microcontrollers containing ROM failures including, but not limited to, the implied warranty of merchantability and fitness for a particular purpose.

RAM Protect. Selecting the DISABLE RAM PROTECT option does not affect the RAM memory. RAM memory operates as defined in this Product Specification for all address locations. Selecting the ENABLE RAM PROTECT option, allows protection (under software control) of a portion of the RAM's address space from being read or written.

System Clock Source. Selecting the RC OSCILLATOR ENABLE option, configures the oscillator circuit on the microcontroller to work with an external RC circuit. Selecting the CRYSTAL/OTHER CLOCK SOURCE option configures the oscillator circuit to work with an external crystal, ceramic resonator, or LC oscillator.

Oscillator Operational Mode. Selecting the NORMAL HIGH FREQUENCY OPERATION ENABLED option enables the part to operate using a standard crystal or resonator, but it does not operate using a 32-kHz crystal. Selecting the 32-KHZ OPERATION ENABLED option enables the microcontroller to work with a 32-kHz crystal and an external feedback resistor—these must be supplied between the XTAL1 and XTAL2 pins. (If RC OSCILLATOR ENABLED is selected in the SYSTEM CLOCK SOURCE option, this option defaults to the NORMAL HIGH FREQUENCY OPERATION ENABLED bit.)

WDT Mode. Selecting the WDT ENABLED BY SOFTWARE ONLY option operates the Watch Dog Timer (WDT) when turned on under software control. Selecting the WDT ENABLED AUTOMATICALLY AFTER RESET option starts the WDT automatically at RESET.There is no way to disable or stop this mode, making it necessary in the code to periodically clear the WDT to prevent it from resetting the microcontroller. If the WDT ENABLED AUTOMATICALLY AFTER RESET option and the WDT DRIVEN BY SYSTEM CLOCK option (if offered) are selected, the WDT *nev-*

er operates in STOP mode, and cannot be enabled, by any means, to operate in STOP mode.

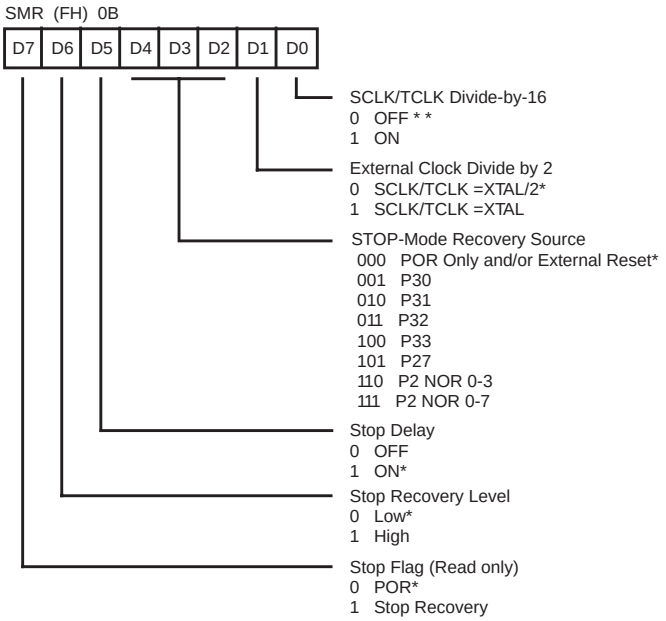
Auto Latch Mode. Selecting the DISABLE AUTOLATCHES option disables the autolatches on the Port pins. These pins will float rather than be pulled to a valid CMOS level when they are inputs and not connected to an external signal. Selecting the ENABLE AUTOLATCHES option enables the autolatches on the Port pins and pulls the pins to a valid CMOS level when they are not connected to an external signal.

Port 0 Pull-Ups. Selecting DISABLE PULL-UPS disables the input pull-up circuitry on all Port 0 pins. Selecting ENABLE PULL-UPS enables the input pull-up circuitry on all Port 0 pins. This option bit does not affect any of the other port pins on the part.

Port 1 Pull-Ups. Selecting DISABLE PULL-UPS disables the input pull-up circuitry on all Port 1 pins. Selecting ENABLE PULL-UPS enables the input pull-up circuitry on all Port 1 pins. This option bit does not affect any of the other port pins on the part.

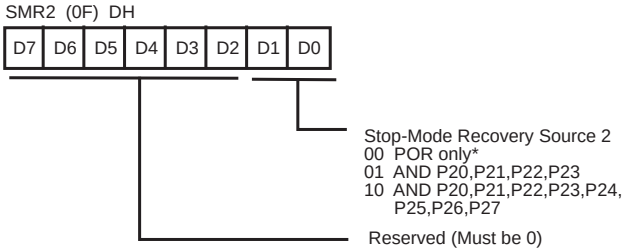
Port 2 Pull-Ups. Selecting DISABLE PULL-UPS disables the input pull-up circuitry on all Port 2 pins. Selecting ENABLE PULL-UPS enables the input pull-up circuitry on all Port 2 pins. This option bit does not affect any of the other port pins on the part.

EXPANDED REGISTER FILE CONTROL REGISTERS



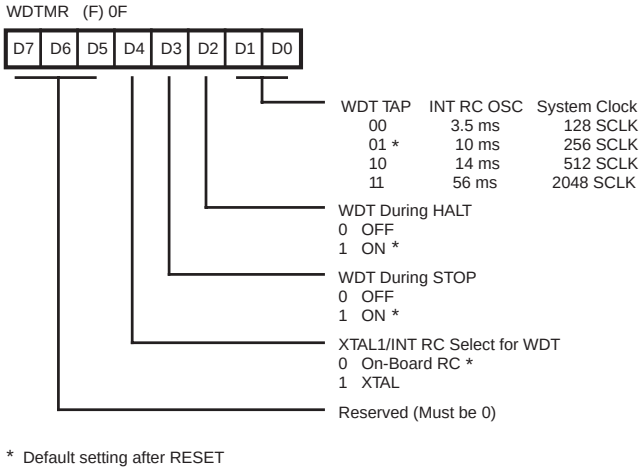
Note: Not used in conjunction with SMR2 Source
* Default setting after RESET.
* * Default setting after RESET and STOP-Mode Recovery.

Figure 37. Stop-Mode Recovery Register (WRITE ONLY, except Bit D7, which is READ ONLY)



Note: Not used in conjunction with SMR Source

Figure 38. Stop-Mode Recovery Register2



* Default setting after RESET

Figure 39. Watch-Dog Timer Mode Register (WRITE ONLY)

Z8 CONTROL REGISTERS

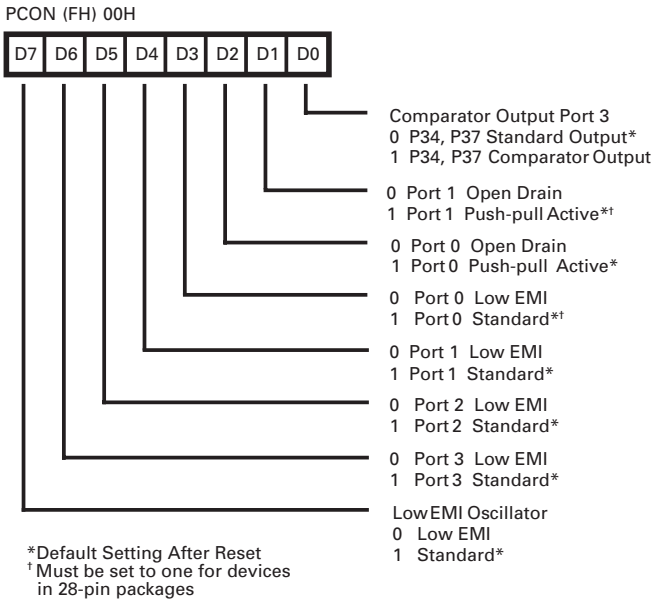


Figure 40. Port Configuration Register (PCON) (WRITE ONLY)

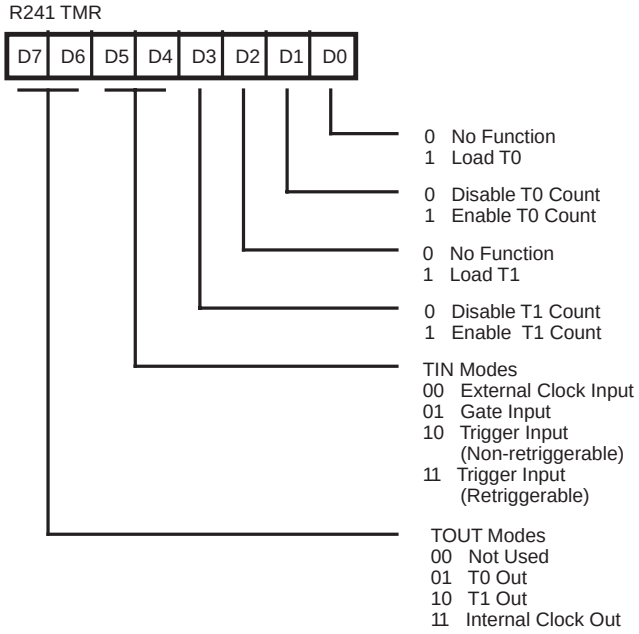


Figure 41. Timer Mode Register ($F1_H$: READ/WRITE)

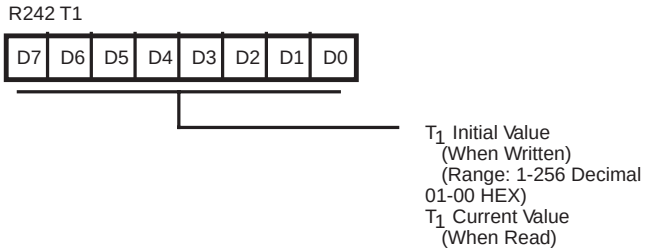


Figure 42. Counter/Timer 1 Register ($F2_H$: READ/WRITE)

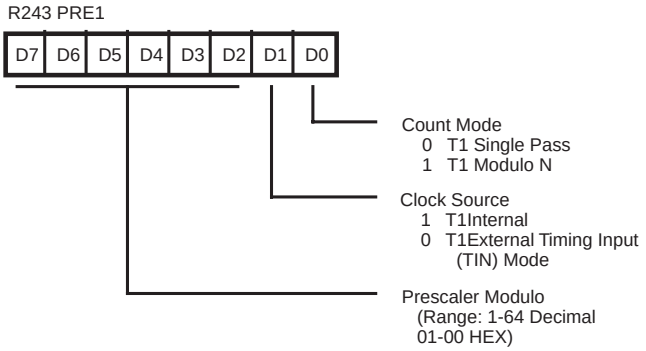


Figure 43. Prescaler 1 Register ($F3_H$: WRITE ONLY)

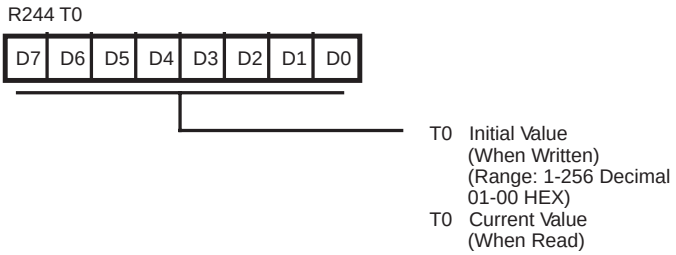


Figure 44. Counter/Timer 0 Register ($F4_H$: READ/WRITE)

Z8 CONTROL REGISTERS (Continued)

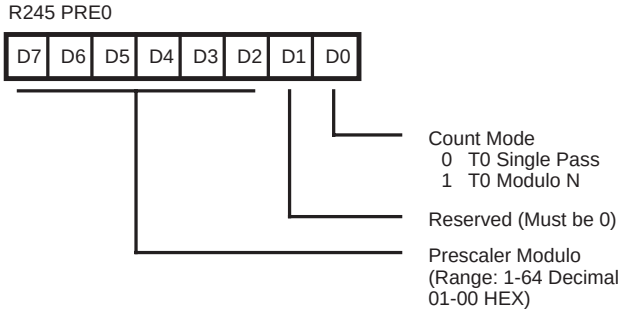


Figure 45. Prescaler 0 Register ($F5_H$: WRITE ONLY)

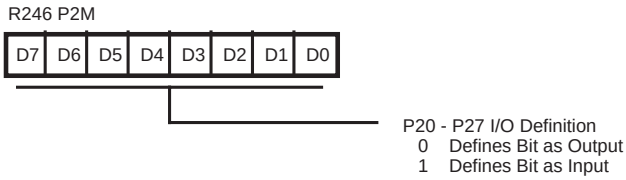


Figure 46. Port 2 Mode Register ($F6_H$: WRITE ONLY)

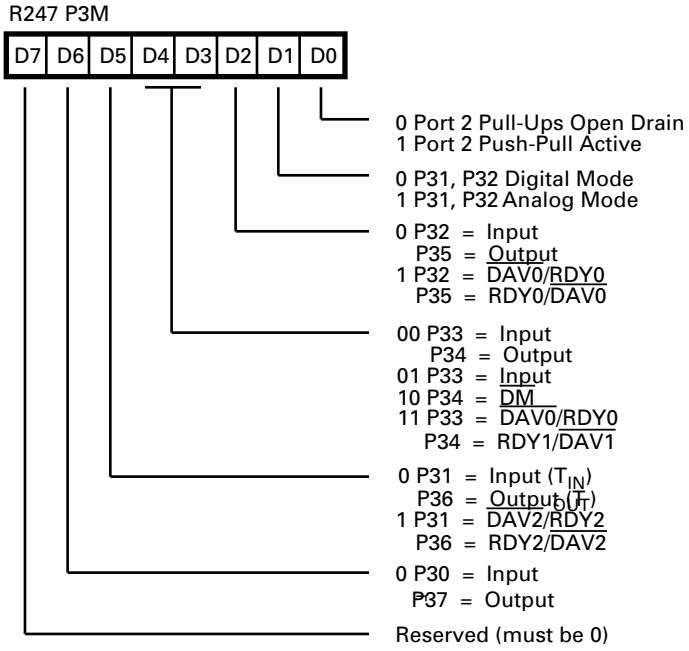


Figure 47. Port 3 Mode Register ($F7_H$: WRITE ONLY)

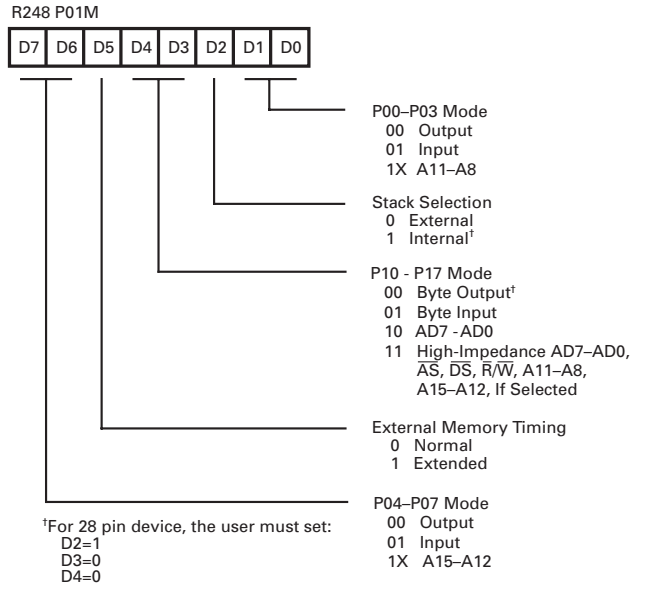


Figure 48. Port 0 and 1 Mode Register ($F8_H$: WRITE ONLY)

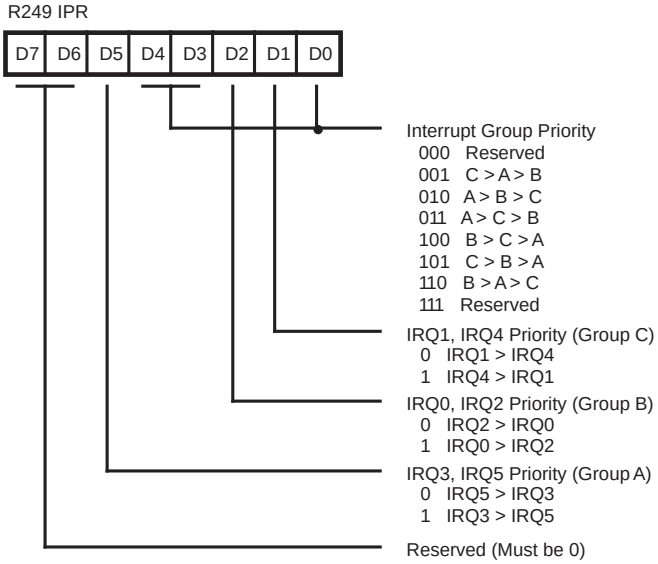


Figure 49. Interrupt Priority Register ($F9_H$: WRITE ONLY)

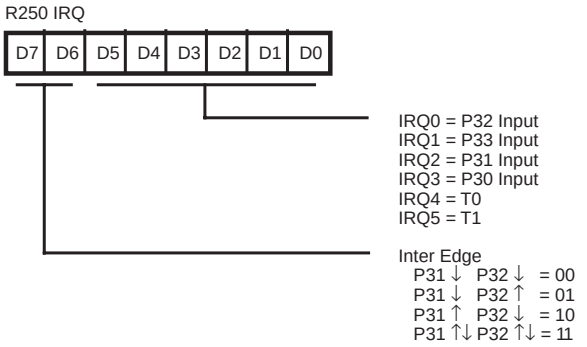


Figure 50. Interrupt Request Register (FA_H: READ/WRITE)

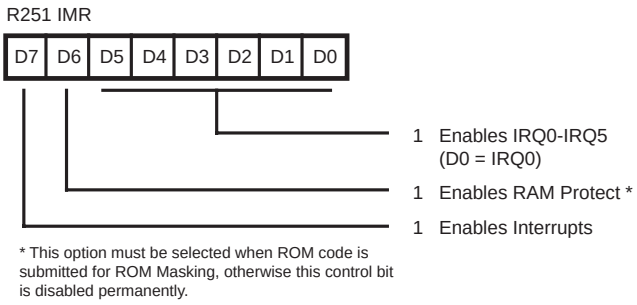


Figure 51. Interrupt Mask Register (FB_H: READ/WRITE)

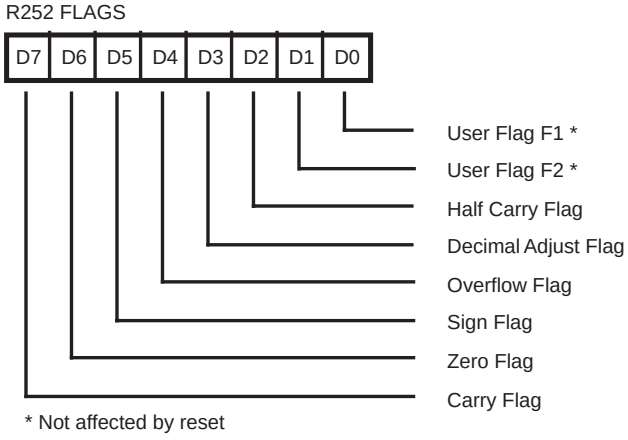


Figure 52. Flag Register (FC_H: READ/WRITE)

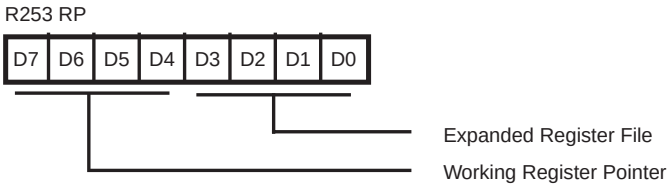


Figure 53. Register Pointer (FD_H: READ/WRITE)

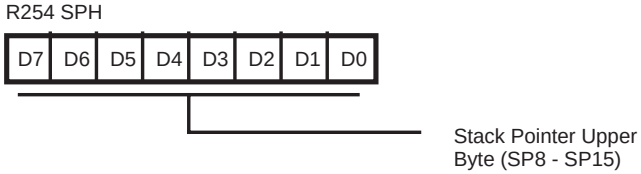


Figure 54. Stack Pointer High (FE_H: READ/WRITE)

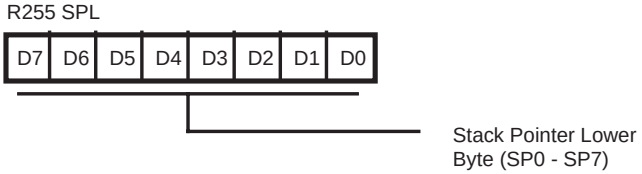
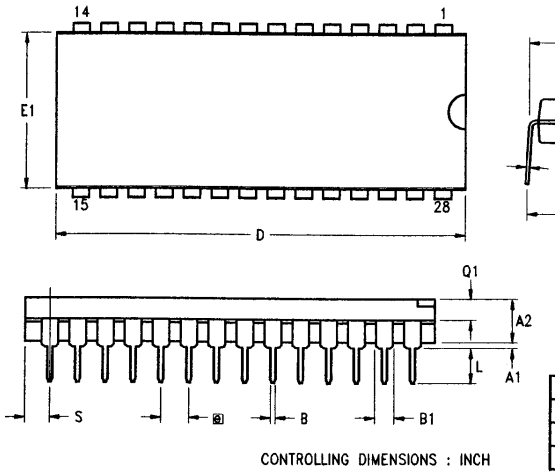


Figure 55. Stack Pointer Low (FF_H: READ/WRITE)

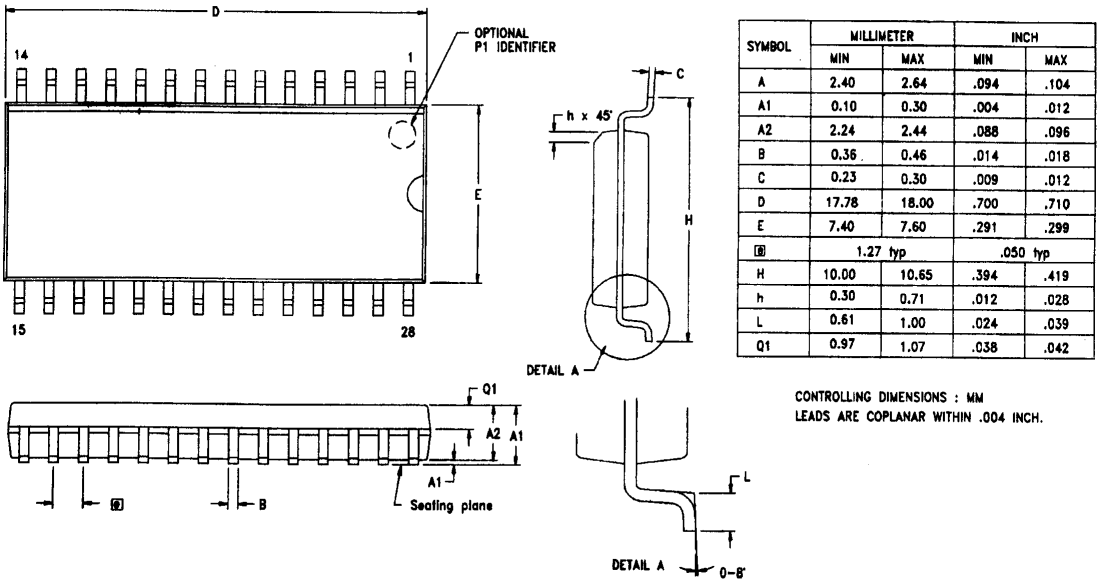
PACKAGE INFORMATION



SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	1.02	.020	.040
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

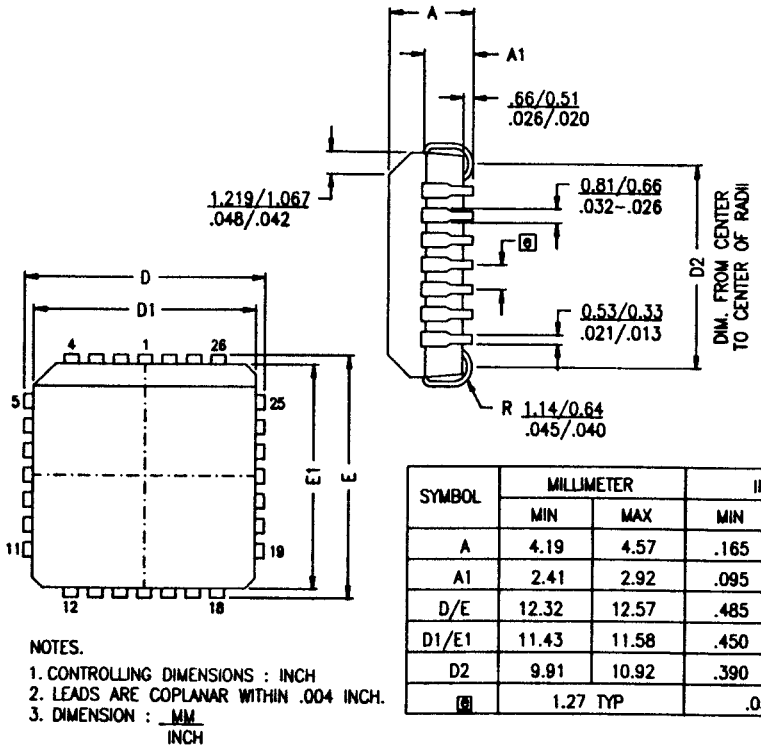
Figure 56. 28-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 typ		.050 typ	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.07	.038	.042

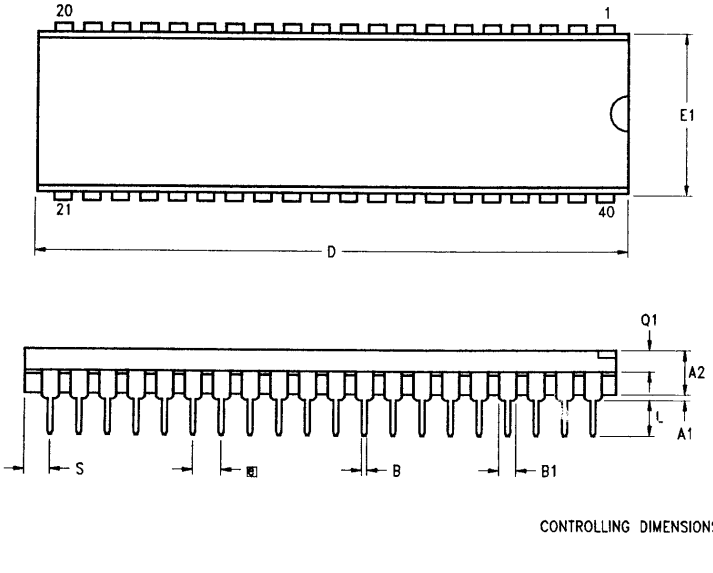
CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 57. 28-Pin SOIC Package Diagram



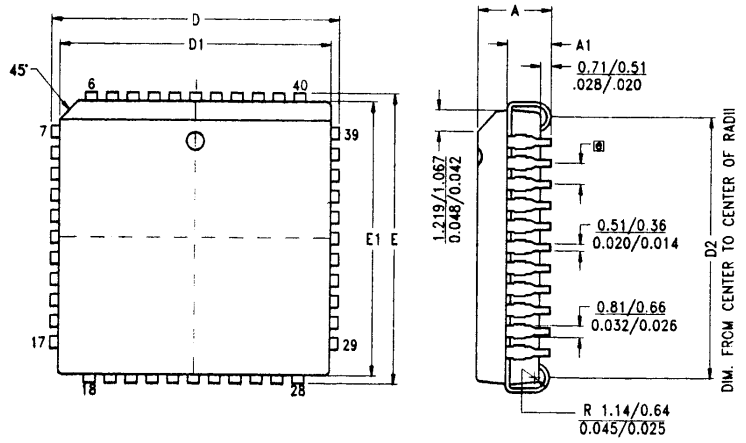
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.19	4.57	.165	.180
A1	2.41	2.92	.095	.115
D/E	12.32	12.57	.485	.495
D1/E1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
e	1.27 TYP		.050 TYP	

Figure 58. 28-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

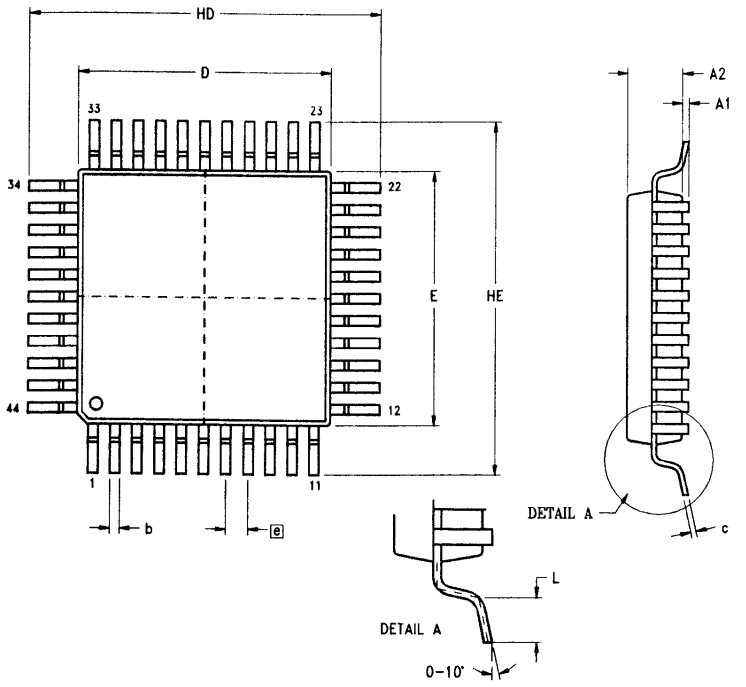
Figure 59. 40-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 TYP		0.050 TYP	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

Figure 60. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 61. 44-Pin QFP Package Diagram

ORDERING INFORMATION

Z86C34

Standard Temperature			Extended Temperature		
28-Pin DIP	28-Pin SOIC	28-Pin PLCC	28-Pin DIP	28-Pin SOIC	28-Pin PLCC
Z86C3416PSC	Z86C3416SSC	Z86C3416VSC	Z86C3416PEC	Z86C3416SEC	Z86C3416VEC

Z86C35

Standard Temperature			Extended Temperature		
28-Pin DIP	28-Pin SOIC	28-Pin PLCC	28-Pin DIP	28-Pin SOIC	28-Pin PLCC
Z86C3516PSC	Z86C3516SSC	Z86C3516VSC	Z86C3516PEC	Z86C3516SEC	Z86C3516VEC

Z86C36

Standard Temperature			Extended Temperature		
28-Pin DIP	28-Pin SOIC	28-Pin PLCC	28-Pin DIP	28-Pin SOIC	28-Pin PLCC
Z86C3616PSC	Z86C3616SSC	Z86C3616VSC	Z86C3616PEC	Z86C3616SEC	Z86C3616VEC

Z86C44

Standard Temperature			Extended Temperature		
40-Pin DIP	44-Pin PLCC	44-Pin QFP	40-Pin DIP	44-Pin PLCC	44-Pin QFP
Z86C4416PSC	Z86C4416VSC	Z86C4416FSC	Z86C4416PEC	Z86C4416VEC	Z86C4416FEC

Z86C45

Standard Temperature			Extended Temperature		
40-Pin DIP	44-Pin PLCC	44-Pin QFP	40-Pin DIP	44-Pin PLCC	44-Pin QFP
Z86C4516PSC	Z86C4516VSC	Z86C4516FSC	Z86C4516PEC	Z86C4516VEC	Z86C4516FEC

Z86C46

Standard Temperature			Extended Temperature		
40-Pin DIP	44-Pin PLCC	44-Pin QFP	40-Pin DIP	44-Pin PLCC	44-Pin QFP
Z86C4616PSC	Z86C4616VSC	Z86C4616FSC	Z86C4616PEC	Z86C4616VEC	Z86C4616FEC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

PRECAUTIONS (Continued)

PRECAUTIONS

1. Enabling the transmit interrupt (bit 0 in the ASCI STAT register) does not make the device ready for transmitter-related interrupts. The receiver interrupt (bit 3 in the ASCI STAT register) must also be enabled.

   Workaround: For transmit interrupts to be generated, the RIE bit must also be set. When IRQ3 is generated, the software should check the STAT register for details on the interrupt source.

2. When using the device in full-duplex mode under interrupts (both transmit and receive interrupts enabled), a small window exists where a transmit or receive interrupt may be lost. This situation occurs when an interrupt is generated by one side (either the transmitter or receiver) and, before the interrupt is serviced, another interrupt is generated by the other side. The second interrupt may be lost.

   Workaround: The only workaround is not to use transmitter interrupts when using the ASCI in full-duplex mode. Use the transmitter in polled mode and the receiver in interrupt mode for full duplex operation. In half-duplex operation, this anomaly does not create a problem.

CODES

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

Preferred Package	P = Plastic DIP
	V = Plastic Chip Carrier
Longer Lead Time	F = Plastic Quad Flat Pack
	S = Small Outline Integrated Chip
Preferred Temperature	S = 0°C to +70°C
Longer Lead Time	E = –40°C to +105°C
Speed	16 = 16 MHz
Environmental	C = Plastic Standard

Example:

The Z86C36 is a 16-MHz PLCC, 0ºC to 70ºC, with Plastic Standard Flow.

Z	ZiLOG Prefix
86C36	Product Number
16	Speed
P	Package
S	Temperature
C	Environmental Flow

Pre-Characterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

ZiLOG, Inc.
910 East Hamilton Avenue, Suite 110
Campbell, CA 95008
Telephone (408) 558-8500
FAX (408) 558-8300
Internet: http://www.zilog.com