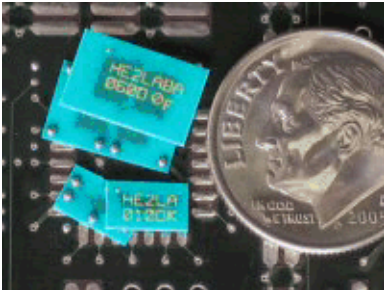


New Specification Coming Soon

Description

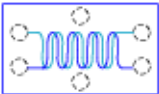


High-efficiency delay lines for clock and data deskew in differential circuit designs requiring precise timing control in a small, low profile BGA package. The differential delay lines are constructed as broadside-coupled transmission lines on ceramic. These designs feature characteristics similar to unshielded twisted-pair cable.

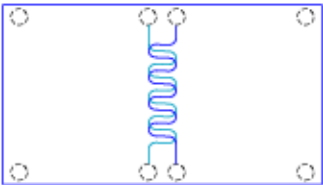
This product is currently available with solder finishes of Sn63/Pb37, as well as a RoHS compliant, Pb free solder finish of Sn95.5/Ag3.8/Cu0.7. For the RoHS compliant part, the customer must specify this upon ordering by following the instructions in the part numbering section of this specification.

Electrical

Size A



Size B

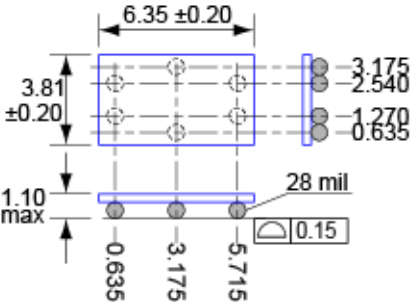


- Not Actual Size -

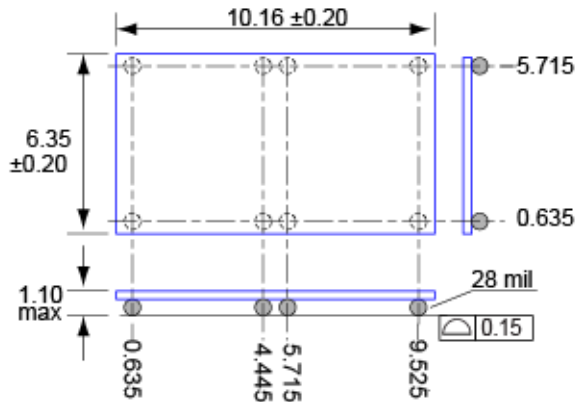
Size Designator:	A	B
Delay Range:	0.1 to 0.5 ns	0.1 to 1.6 ns
Standard Delay Increment:	0.1 ns	0.1 ns
Delay Tolerance:	± (15 ps + 2% of nominal)	
Differential Impedance:	100 Ω ± 10%	
DC Resistance:	0.1 - 0.5 ns < 1.15 Ω over 0.5 ns < 2.30 Ω/ns	
Rated Current:	100 mA	
Temp. Coef. of Time Delay:	< 150 ppm/C	
Insulation Resistance:	> 100MΩ (100 Vdc)	
Isolation Resistance:	> 100 MΩ (100 Vdc)	
Operating Temperature:	-40 to +85°C	
Storage Temperature:	-55 to +125C°	

Mechanical

Size A



Size B



Notes for Both:

Either DL1 or DL2 can be used for the inverted and non-inverted signals.

Ball positions labeled 'No Connection' are only present for mechanical stability (attach all to open pads on board).

Notes:

Delay Line 1 I/O (DL1) = b1 & b3

Delay Line 2 I/O (DL2) = c1 & c3

The following positions do not have a ball: a1, a3, b2, c2, d1, d3

No Connection = all other

Both signals shall enter positions '1' and exit positions '3' or both signals shall enter positions '3' and exit positions '1'.

Notes:

Delay Line 1 I/O (DL1) = a2 & b2

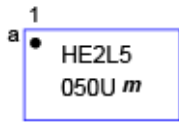
Delay Line 2 I/O (DL2) = a3 & b3

No Connection = all other

Both signals shall enter positions 'a' and exit positions 'b' or both signals shall enter positions 'b' and exit positions 'a'.

Marking

Size A



Size B

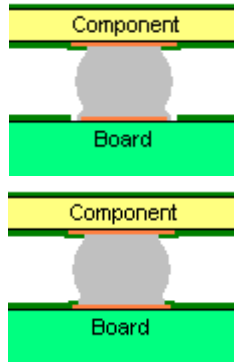


the part number code will be marked on the top of the part in 2 rows followed by a TFT "don't stop" logo ("B" size only)

a 1 digit monthly date code

A '1' pin identifier (dot) will be located as shown above

Land Pattern



Copper Defined Land Pattern:

Dimensions (mm)

Copper Land diameter	0.66 - 0.71
Soldermask diameter	0.81 - 0.86
Soldermask clearance	0.07 min

Soldermask Defined Land Pattern:

Dimensions (mm)

Soldermask diameter	0.66 - 0.71
Soldermask diameter	0.05 min

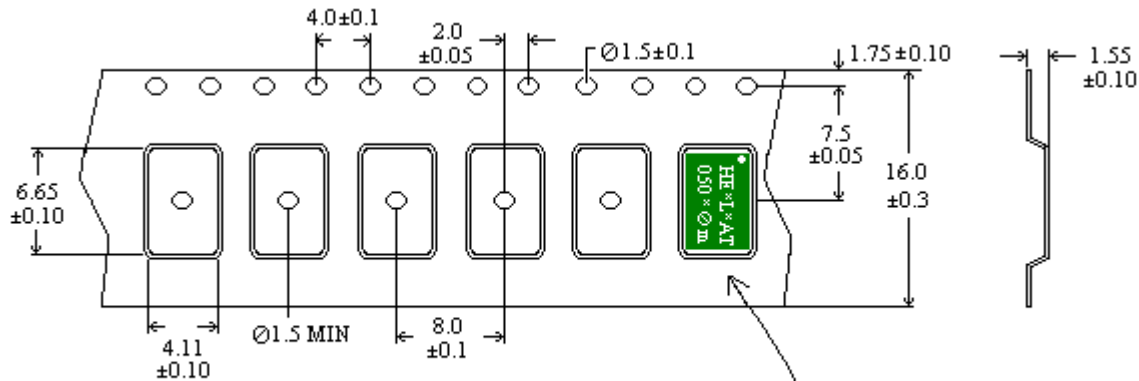
Note:

Adjust the copper land diameter accordingly to ensure the minimum soldermask coverage.

Recommended dimensions as per IPC-7095 "Design and Assembly Process Implementation for BGAs".

Packaging

Size Designator A:



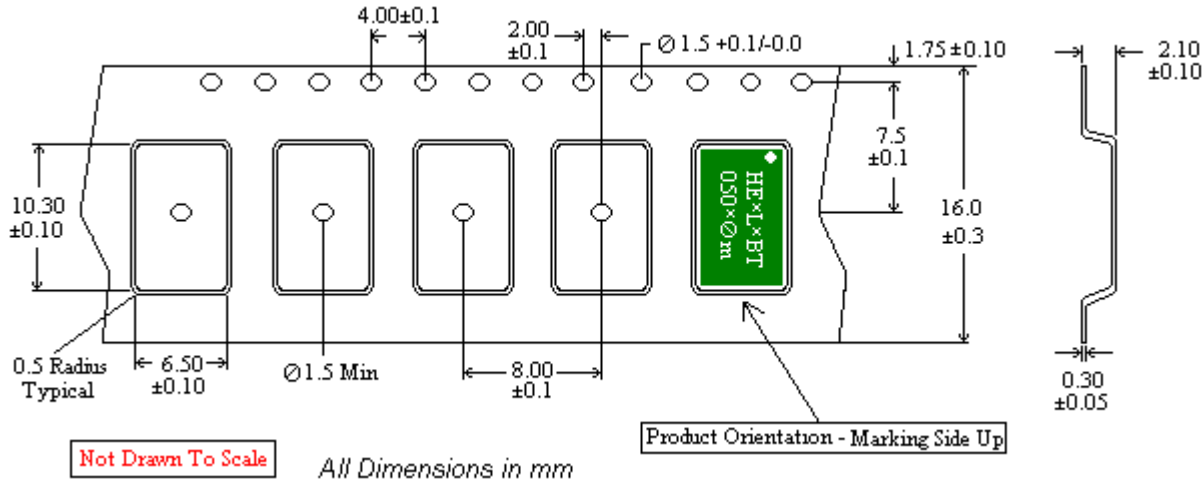
Not Drawn To Scale

All Dimensions in mm

Additional Comments:

- All taping done in accordance with EIA 481 standards
- Pieces taped with the marking up and showing through the cover tape
- Labels will contain the TFT part number and quantity of pieces taped
- Carrier Tape Part#: CT-9916H-123
- Carrier Tape Drawing#: 01-019491

Size Designator B:



Additional Comments:

- All taping done in accordance with EIA 481 standards
- Pieces taped with the marking up and showing through the cover tape
- Labels will contain the TFT part number and quantity of pieces taped
- Carrier Tape Part#: TBD
- Carrier Tape Drawing#: TBD

Part Number

HE 2L A * *** D -T5 -C

	RoHS compliant and lead free
	Packaging (T = Tape, 5 = 500 pcs/reel)
	Serial Code (D = Coupled pair)
	Delay ns x 100 (050 = 0.5 ns)
	Size designator (A or B size)
	Impedance (A = 100 ohm)
	Number of signal lines
	Product family



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