

2N7002E

TrenchMOS™ Logic Level FET

Rev. 01 — 11 February 2002

Product data

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™¹ technology.

Product availability:

2N7002E in SOT23.

2. Features

- TrenchMOS™ technology
- Very fast switching
- Logic level compatible
- Subminiature surface mount package.

3. Applications

- Relay driver
- High speed line driver
- Logic level translator.

4. Pinning information

Table 1: Pinning - SOT23, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	source (s)		
3	drain (d)		
		SOT23	N-channel MOSFET

1. TrenchMOS is a trademark of Koninklijke Philips Electronics N.V.



PHILIPS

5. Quick reference data

Table 2: Quick reference data

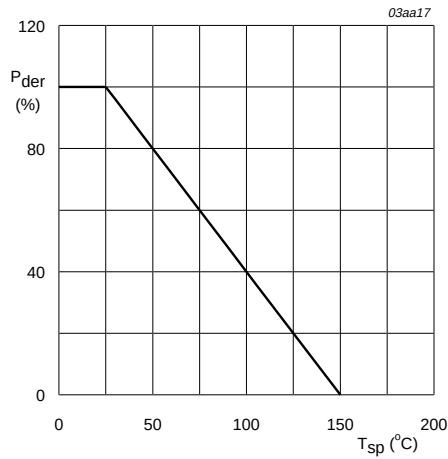
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	-	60	V
I_D	drain current (DC)	$T_{sp} = 25$ °C; $V_{GS} = 10$ V	-	385	mA
P_{tot}	total power dissipation	$T_{sp} = 25$ °C	-	0.83	W
T_j	junction temperature		-	150	°C
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 500$ mA; $T_j = 25$ °C	2.3	3	Ω
		$V_{GS} = 4.5$ V; $I_D = 75$ mA; $T_j = 25$ °C	3.1	4	Ω

6. Limiting values

Table 3: Limiting values

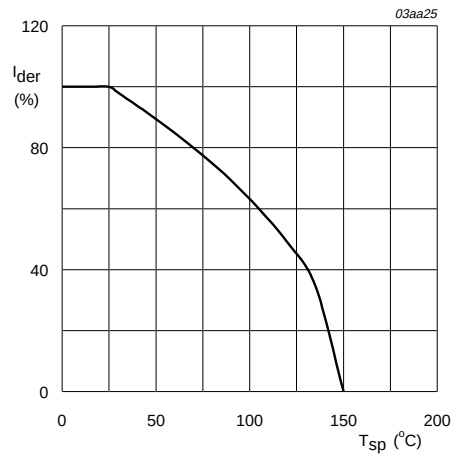
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	-	60	V
V_{DGR}	drain-gate voltage (DC)	$T_j = 25$ to 150 °C; $R_{GS} = 20$ k Ω	-	60	V
V_{GS}	gate-source voltage (DC)		-	± 30	V
V_{GSM}	peak gate-source voltage	$t_p \leq 50$ μ s; pulsed; duty cycle = 25%	-	± 40	V
I_D	drain current (DC)	$T_{sp} = 25$ °C; $V_{GS} = 10$ V; Figure 2 and 3	-	385	mA
		$T_{sp} = 100$ °C; $V_{GS} = 10$ V; Figure 2	-	245	mA
I_{DM}	peak drain current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ μ s; Figure 3	-	1.5	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; Figure 1	-	0.83	W
T_{stg}	storage temperature		-65	+150	°C
T_j	operating junction temperature		-65	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25$ °C	-	385	mA
I_{SM}	peak source (diode forward) current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ μ s	-	1.5	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

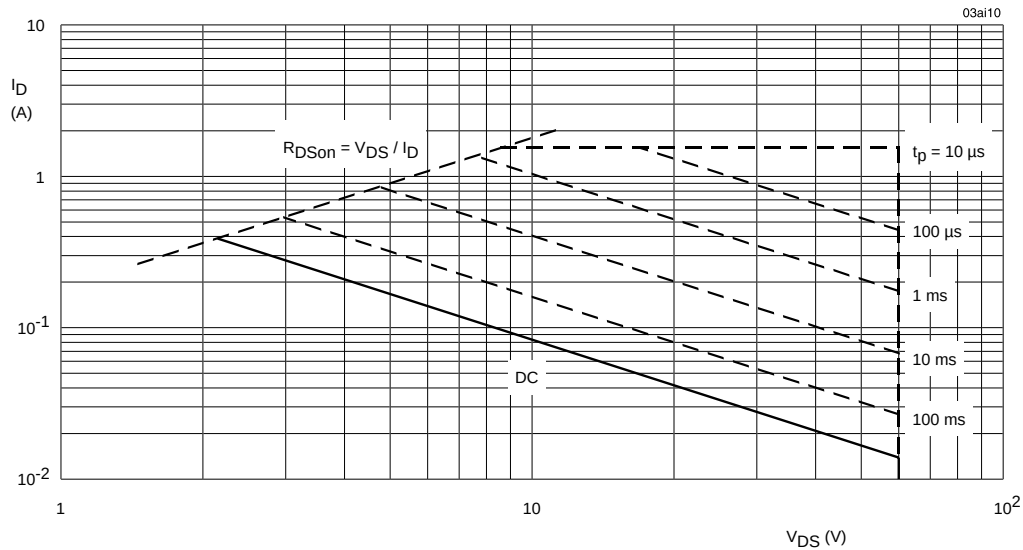
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$V_{GS} \geq 4.5 \text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 10 \text{ V}$.

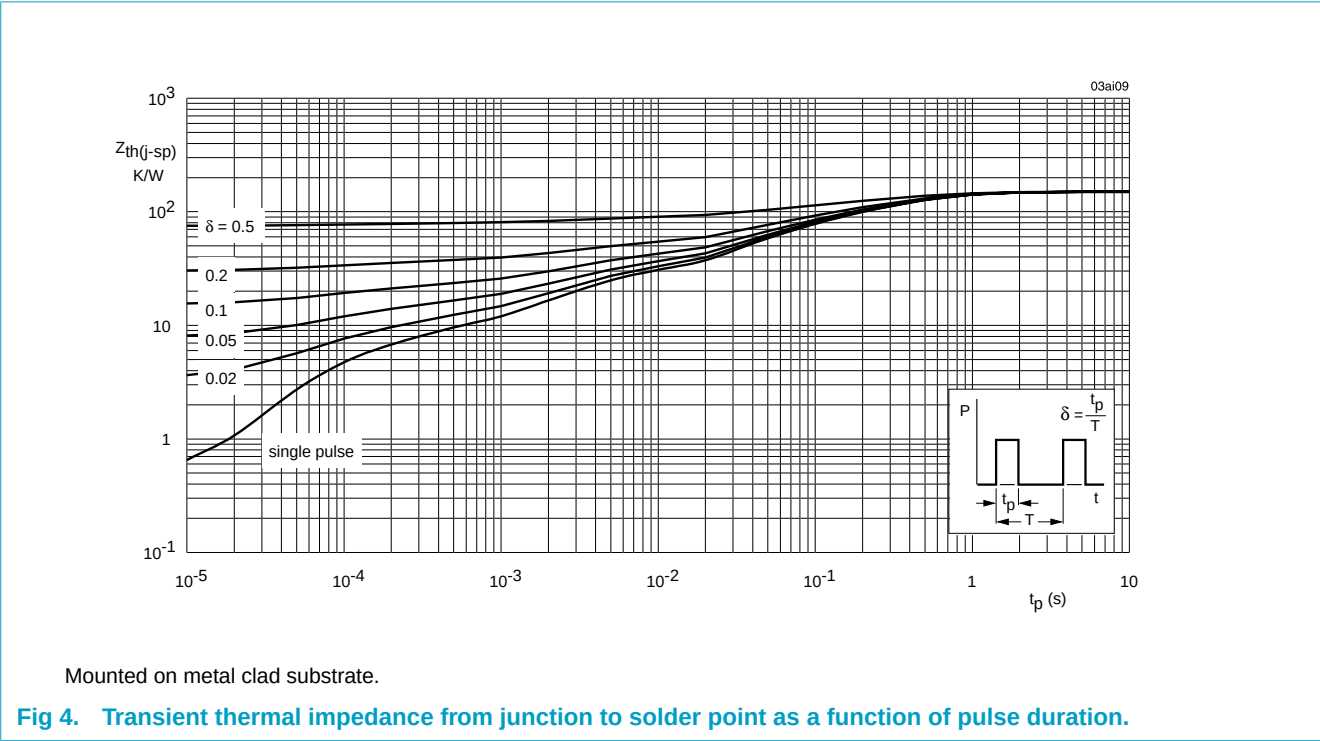
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad board; Figure 4	-	-	150	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; minimum footprint	-	-	350	K/W

7.1 Transient thermal impedance

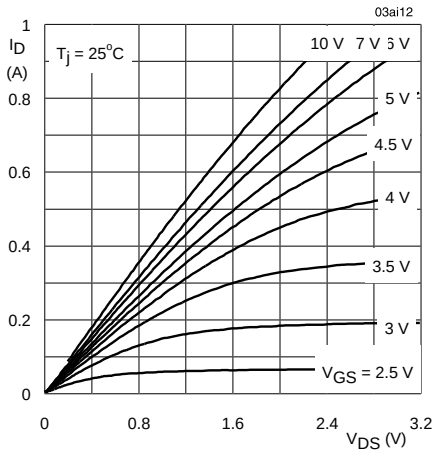


8. Characteristics

Table 5: Characteristics

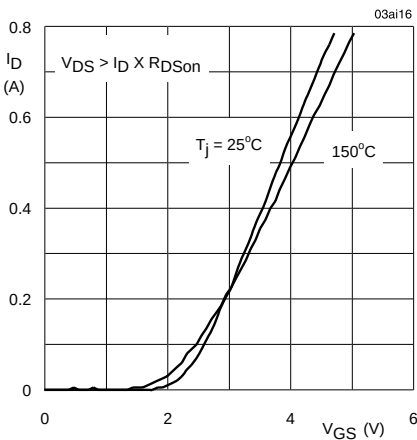
$T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ °C}$	60	75	-	V
		$T_j = -55\text{ °C}$	55	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9 $T_j = 25\text{ °C}$	1	2	-	V
		$T_j = 150\text{ °C}$	0.6	-	-	V
		$T_j = -55\text{ °C}$	-	-	3.5	V
I_{DSS}	drain-source leakage current	$V_{DS} = 48\text{ V}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ °C}$	-	0.01	1.0	μA
		$T_j = 150\text{ °C}$	-	-	10	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 15\text{ V}$; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 500\text{ mA}$; Figure 7 and 8 $T_j = 25\text{ °C}$	-	2.3	3	Ω
		$T_j = 150\text{ °C}$	-	4.2	5.55	Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 75\text{ mA}$; Figure 7 and 8 $T_j = 25\text{ °C}$	-	3.1	4	Ω
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 200\text{ mA}$	100	300	-	mS
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 10\text{ V}$; $f = 1\text{ MHz}$; Figure 11	-	25	40	pF
C_{oss}	output capacitance		-	18	30	pF
C_{rss}	reverse transfer capacitance		-	7.5	10	pF
t_{on}	turn-on time	$V_{DD} = 50\text{ V}$; $R_D = 250\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_G = 50\text{ }\Omega$; $R_{GS} = 50\text{ }\Omega$	-	3	10	ns
t_{off}	turn-off time		-	12	15	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 300\text{ mA}$; $V_{GS} = 0\text{ V}$; Figure 12	-	0.85	1.5	V
t_{rr}	reverse recovery time	$I_S = 300\text{ mA}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	30	-	ns
Q_r	recovered charge	$V_{DS} = 25\text{ V}$	-	30	-	nC



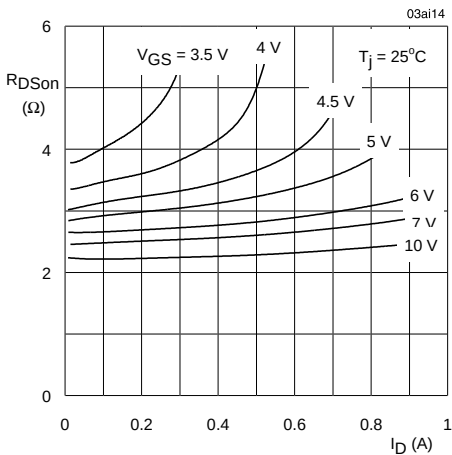
$T_j = 25^\circ\text{C}$.

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



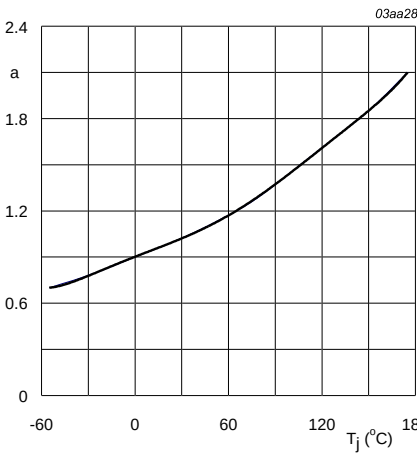
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$.

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



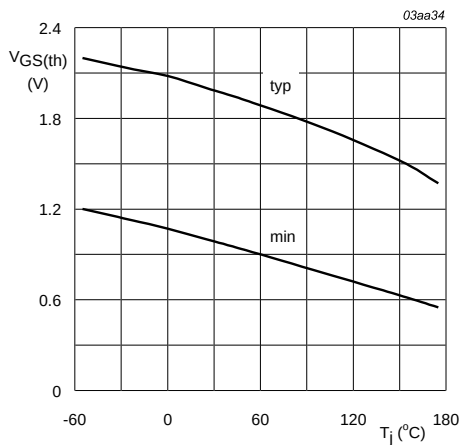
$T_j = 25^\circ\text{C}$.

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



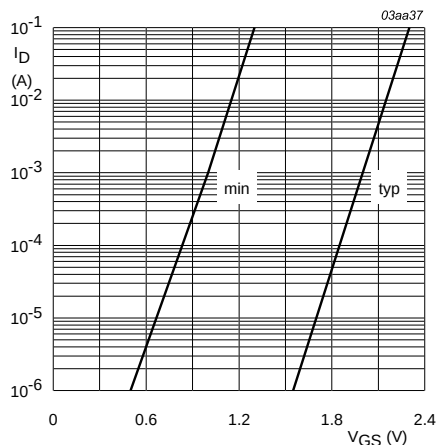
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



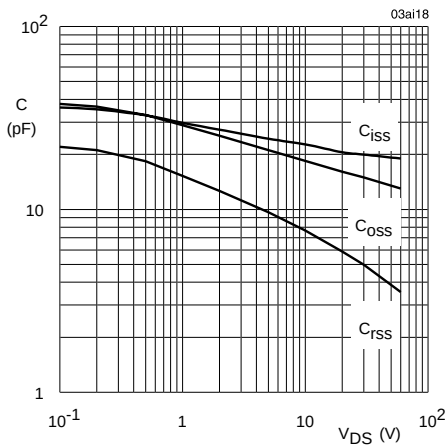
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$.

Fig 9. Gate-source threshold voltage as a function of junction temperature.



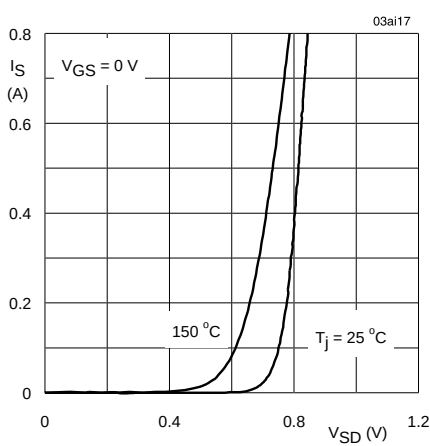
$T_j = 25 \text{ }^\circ\text{C}$; $V_{DS} = 5 \text{ V}$.

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$.

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25 \text{ }^\circ\text{C}$ and $150 \text{ }^\circ\text{C}$; $V_{GS} = 0 \text{ V}$.

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

9. Package outline

Plastic surface mounted package; 3 leads

SOT23

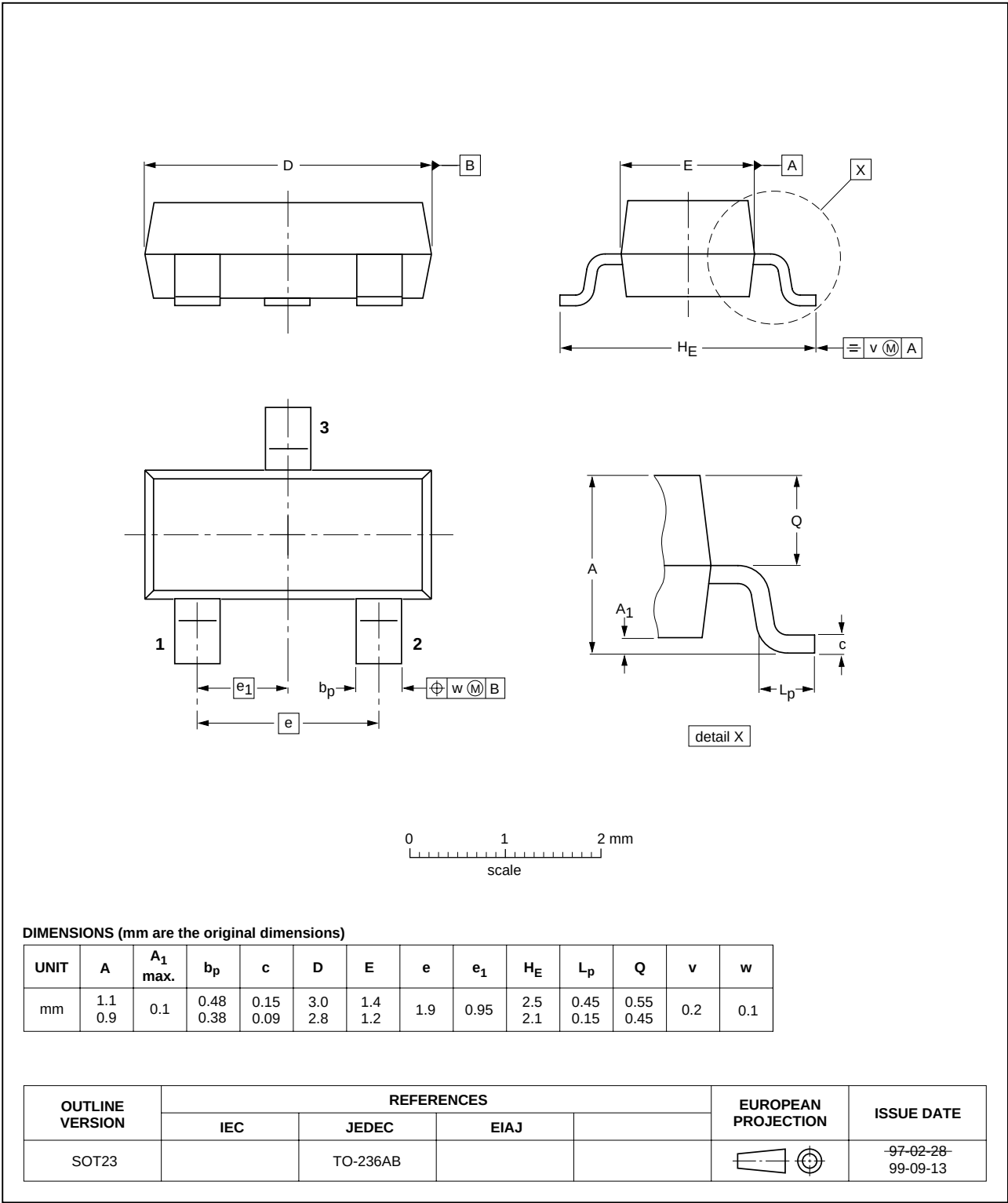


Fig 13. SOT23.

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20020211	-	Product spec; initial version

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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