

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM3J120TU

○ Power Management Switch Applications

○ High-Current Switching Applications

- 1.5 V drive
- Low on-resistance

$$\begin{aligned}
 R_{on} &= 140 \text{ m}\Omega \text{ (max)} (@V_{GS} = -1.5 \text{ V}) \\
 R_{on} &= 78 \text{ m}\Omega \text{ (max)} (@V_{GS} = -1.8 \text{ V}) \\
 R_{on} &= 49 \text{ m}\Omega \text{ (max)} (@V_{GS} = -2.5 \text{ V}) \\
 R_{on} &= 38 \text{ m}\Omega \text{ (max)} (@V_{GS} = -4.0 \text{ V})
 \end{aligned}$$

Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | Symbol | Rating | Unit |
|-------------------------|-------------------------|-----------------|------|
| Drain-Source voltage | V _{DS} | -20 | V |
| Gate-Source voltage | V _{GSS} | ± 8 | V |
| Drain current | DC | I _D | A |
| | Pulse | I _{DP} | |
| Drain power dissipation | P _D (Note 1) | 800 | mW |
| | P _D (Note 2) | 500 | |
| Channel temperature | T _{ch} | 150 | °C |
| Storage temperature | T _{stg} | -55~150 | °C |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the

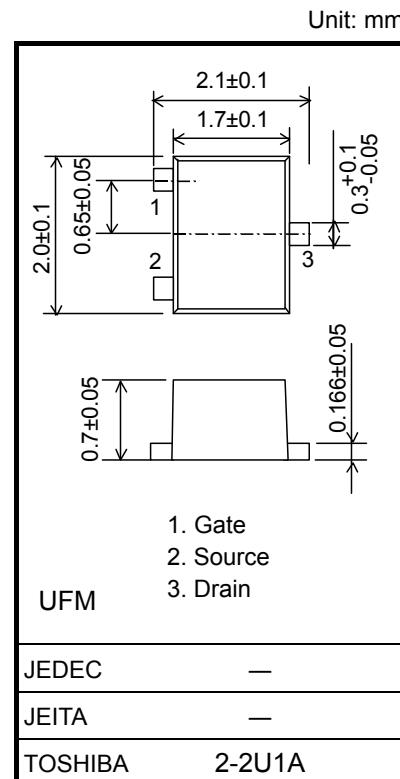
Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1 : Mounted on ceramic board

(25.4 mm × 25.4 mm × 0.8 t, Cu Pad: 645 mm²)

Note 2 : Mounted on FR4 board

(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm²)



Weight: 6.6mg (typ.)

Electrical Characteristics (Ta = 25°C)

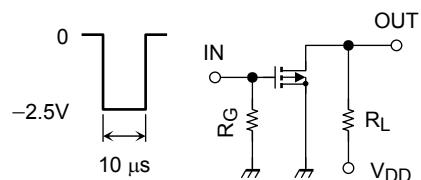
| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|--------------------------------|-----------------------|--|--|------|------|------|
| Drain-Source breakdown voltage | V _{(BR) DSS} | I _D = -1 mA, V _{GS} = 0 | -20 | — | — | V |
| | V _{(BR) DSX} | I _D = -1 mA, V _{GS} = +8 V | -12 | — | — | |
| Drain cut-off current | I _{DSS} | V _{DS} = -20 V, V _{GS} = 0 | — | — | -10 | μA |
| Gate leakage current | I _{GSS} | V _{GS} = ±8 V, V _{DS} = 0 | — | — | ±1 | μA |
| Gate threshold voltage | V _{th} | V _{DS} = -3 V, I _D = -1 mA | -0.3 | — | -1.0 | V |
| Forward transfer admittance | Y _{fs} | V _{DS} = -3 V, I _D = -2.0 A (Note 3) | 6.1 | 12.1 | — | S |
| Drain-Source ON-resistance | R _{DS (ON)} | I _D = -3.0 A, V _{GS} = -4.0 V (Note 3) | — | 28 | 38 | mΩ |
| | | I _D = -2.0 A, V _{GS} = -2.5 V (Note 3) | — | 34 | 49 | |
| | | I _D = -1.0 A, V _{GS} = -1.8 V (Note 3) | — | 47 | 78 | |
| | | I _D = -0.3 A, V _{GS} = -1.5 V (Note 3) | — | 60 | 140 | |
| Input capacitance | C _{iss} | V _{DS} = -10 V, V _{GS} = 0 f = 1 MHz | — | 1484 | — | pF |
| Output capacitance | C _{oss} | | — | 185 | — | pF |
| Reverse transfer capacitance | C _{rss} | | — | 169 | — | pF |
| Switching time | Turn-on time | t _{on} | V _{DD} = -10 V, I _D = -2.0 A V _{GS} = 0 ~ -2.5 V, R _G = 4.7 Ω | 67 | — | ns |
| | Turn-off time | t _{off} | | 92 | — | |

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit | |
|------------------------------|-----------|---|----------|------|-----|------|---|
| Total gate charge | Q_g | $V_{DS} = -16 \text{ V}$, $I_{DS} = -4.0 \text{ A}$, $V_{GS} = -4.0 \text{ V}$, | — | 22.3 | — | nC | |
| Gate-Source charge | Q_{gs} | | — | 14.9 | — | | |
| Gate-Drain charge | Q_{gd} | | — | 7.3 | — | | |
| Drain-Source forward voltage | V_{DSF} | $I_D = 4.0 \text{ A}$, $V_{GS} = 0$ | (Note 3) | — | 0.8 | 1.2 | V |

Note 3: Pulse test

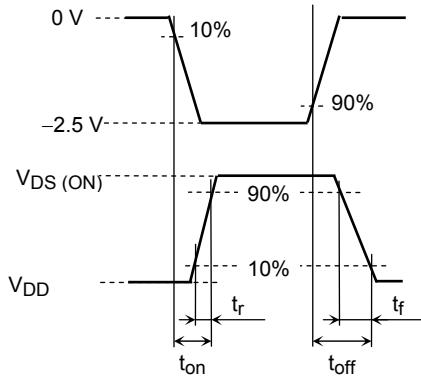
Switching Time Test Circuit

(a) Test Circuit

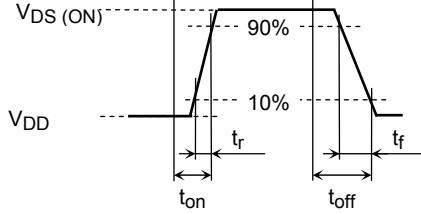


$V_{DD} = -10 \text{ V}$
 $R_G = 4.7 \Omega$
D.U. $\leq 1\%$
 V_{IN} : $t_r, t_f < 5 \text{ ns}$
Common Source
 $T_a = 25 \text{ }^{\circ}\text{C}$

(b) V_{IN}

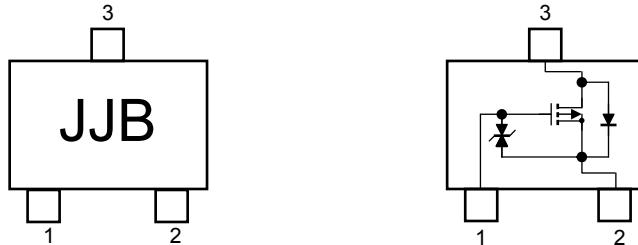


(c) V_{OUT}



Marking

Equivalent Circuit (top view)



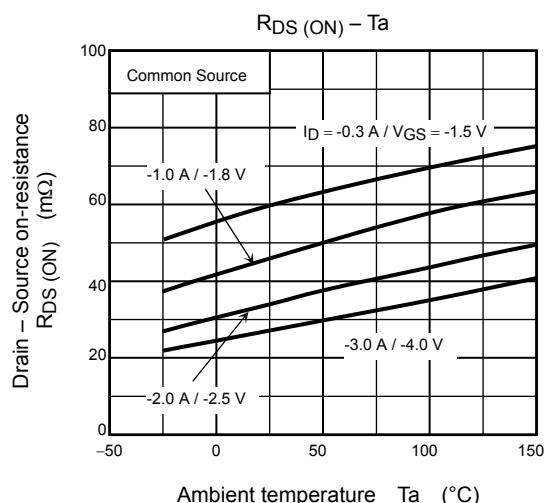
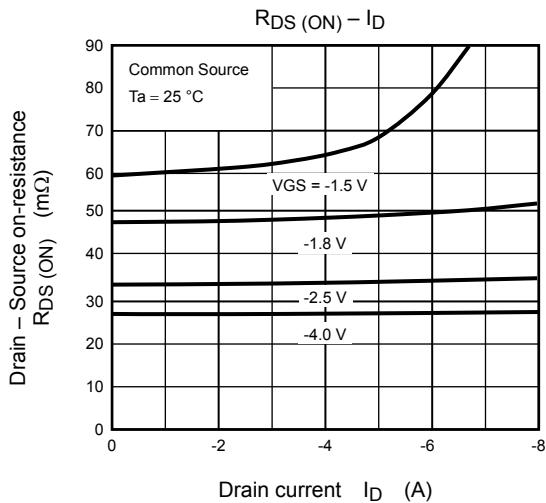
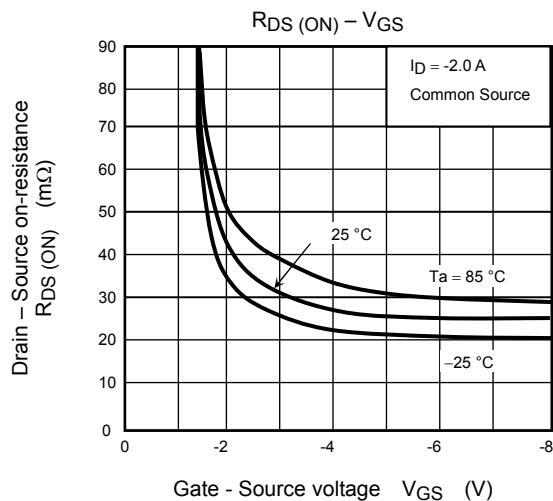
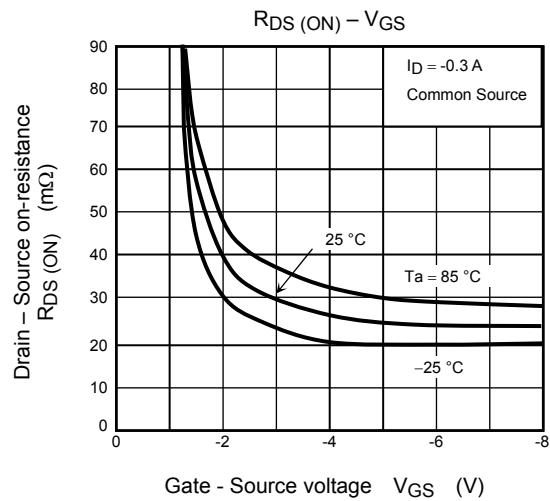
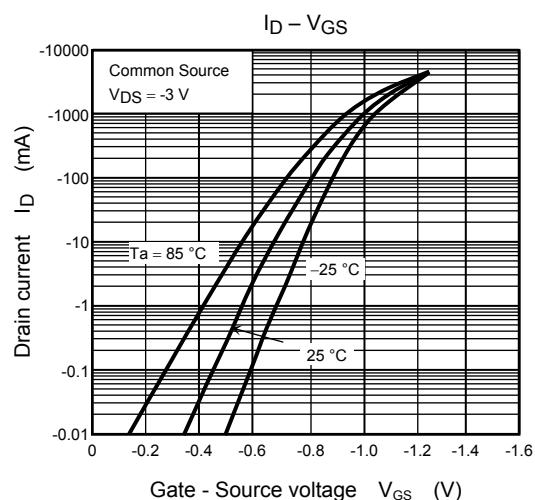
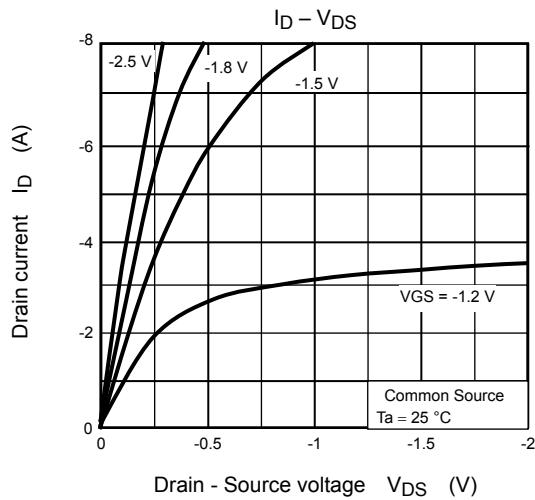
Precaution

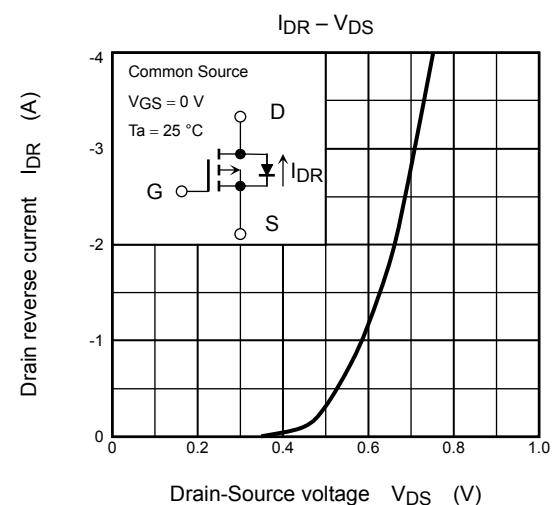
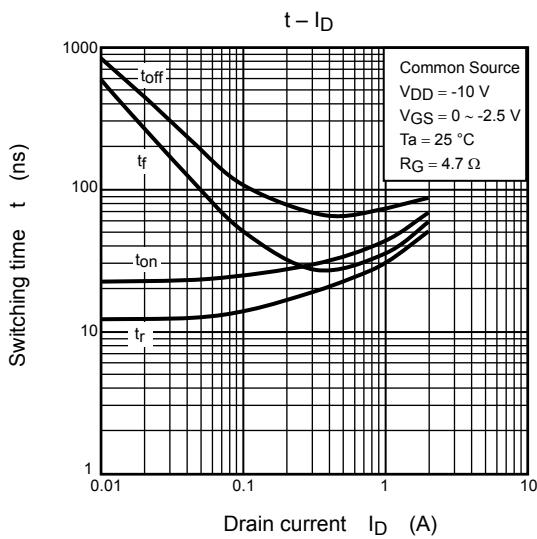
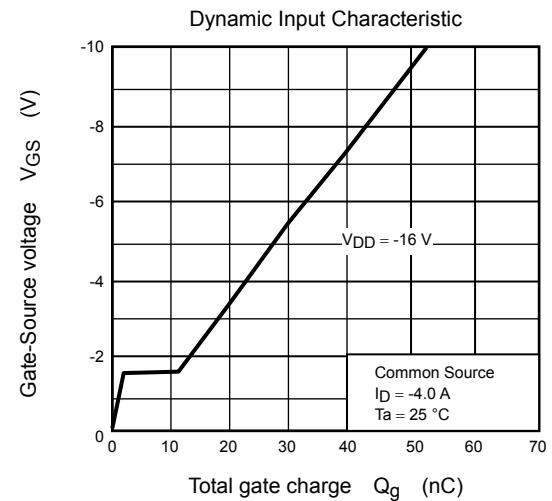
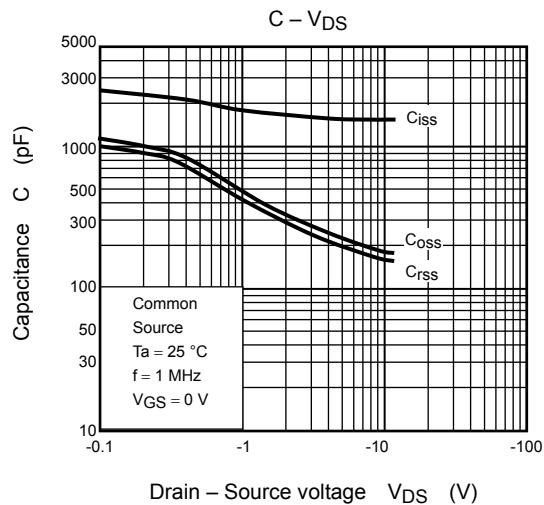
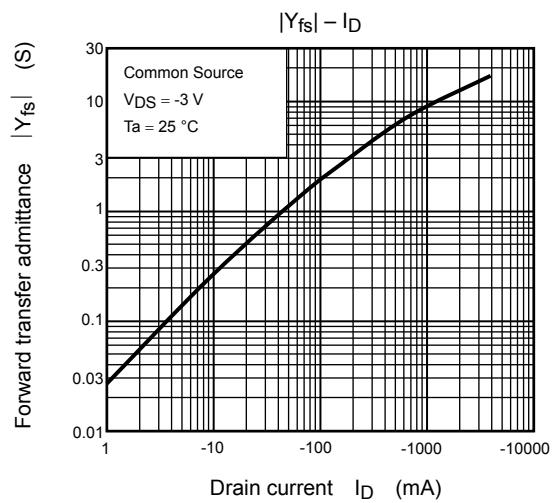
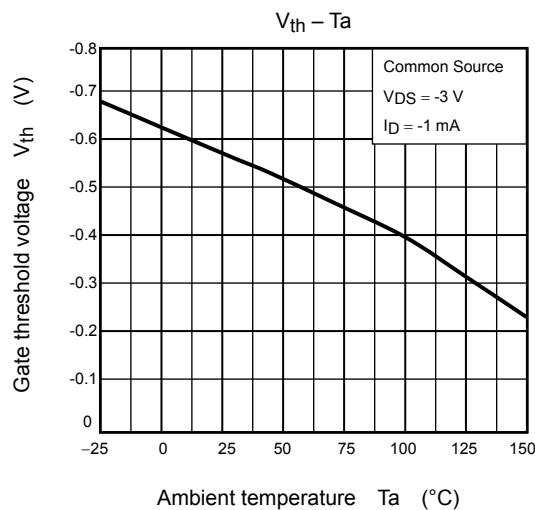
V_{th} can be expressed as the voltage between the gate and source when the low operating current value is $I_D = -1\text{mA}$ for this product. For normal switching operation, V_{GS} (on) requires a higher voltage than V_{th} and V_{GS} (off) requires a lower voltage than V_{th} . (The relationship can be established as follows: V_{GS} (off) $< V_{th} < V_{GS}$ (on).)

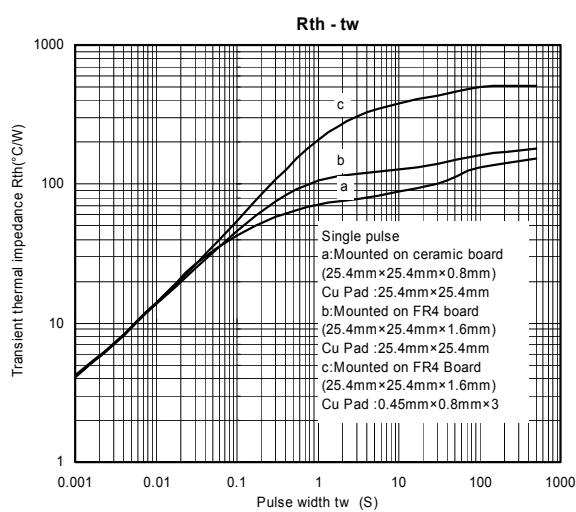
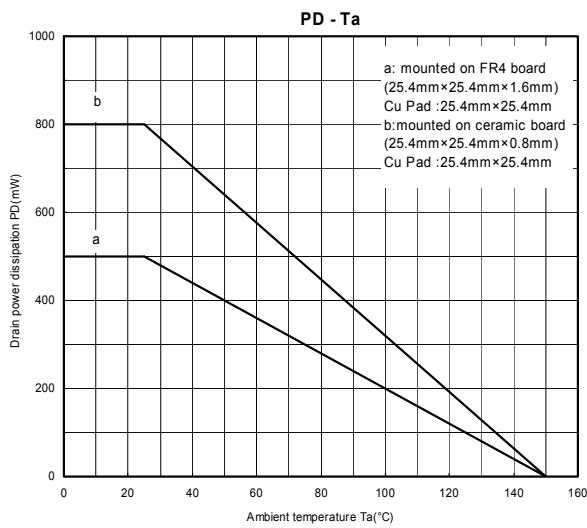
Be sure to take this into consideration when using the device.

Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.







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20070701-EN GENERAL

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