CMOS 8-BIT MICROCONTROLLER

TMP88CK49N, TMP88CM49N
TMP88CK49F, TMP88CM49F

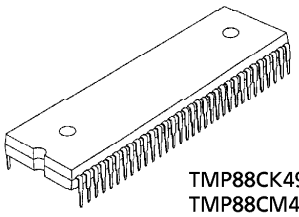
TMP88CK49N, TMP88CM49N, TMP88CK49F, and TMP88CM49F, are high-speed and high-function 8-bit single-chip microcomputers whose built-in features include large-capacity RAM, multi-function timer/counter, and 10-bit A/D converter, serial interface (UART/I2C bus). They are equipped with DC sensorless/sensor motor control, and AC motor inverter control.

PART No.	ROM	RAM	PACKAGE	OTP MCU
TMP88CK49N	24K bytes	1K bytes	SDIP64-P-750-1.78	TMP88PS49N
TMP88CK49F			QFP64-P-1420-1.00A	TMP88PS49F
TMP88CM49N	32K bytes		SDIP64-P-750-1.78	TMP88PS49N
TMP88CM49F			QFP64-P-1420-1.00A	TMP88PS49F

FEATURES

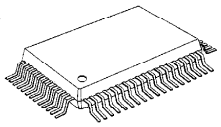
- ◆8-bit single-chip microcomputer TLCS-870/X series microcomputer
- ◆Interrupt sources: 34 (6 external, 28 Internal)
- ◆I/O ports: 56 pins
  - Large-current output: 8 pins (typ. 20 mA), LED direct drive
- ◆16-bit timer/counter: 2 channels
  - Timer, event counter, programmable pulse generator (PPG) output, pulse width measurement, external trigger timer, window mode
- ◆8-bit Timer/Counter: 2 channels
  - Timer, event counter, capture (pulse width/duty measurement), pulse width modulation (PWM) output, programmable divider output (PDO) mode
- ◆Time base timer (interrupt frequency : 1 to 16384 Hz)
- ◆Watchdog timer
- ◆Divider output function (frequency : 1 to 8 kHz)
- ◆Programmable motor driver (PMD) : 2 channels
  - Rotor position : minimum resolution of 250 ns for detecting rotor position
  - Motor control timer, timer capture function
  - Overload protection function
    DC overload protection function
    AC overload protection function (0-vector controllable : Can halt counter in 3-phase PWM output circuit)
  - Protection circuit for malfunction (urgent halt)
  - Automatic direction change, automatic position detection start
- ◆High-speed PWM output: 2 channels
  - Cycle: 32 kHz, 64 kHz, 128 kHz
  - Resolution: 8-bit, 7-bit, 6-bit mode selectable
- ◆Serial interface
  - 8-bir SIO/I2C bus
  - Universal asynchronous receiver transmitter (UART)
- ◆10-bit successive approximation type A/D converter
  - Analog input: 16 channels
  - Conversion time: 46 μs (at 16 MHz operation)
- ◆Low power dissipation operation (2 modes)
  - STOP mode: Stops oscillation (battery or capacitor backup). Port output hold or high impedance selectable
  - IDLE mode: Stops CPU but continues operation of peripheral hardware. Released by interrupt (restarts CPU)
- ◆Operating voltage: 4.5 to 5.5 V at 16 MHz operation
- ◆Emulation pod

SDIP64-P-750-1.78



TMP88CK49N
TMP88CM49N
TMP88PS49N

QFP64-P-1420-1.00A



TMP88CK49F
TMP88CM49F
TMP88PS49F

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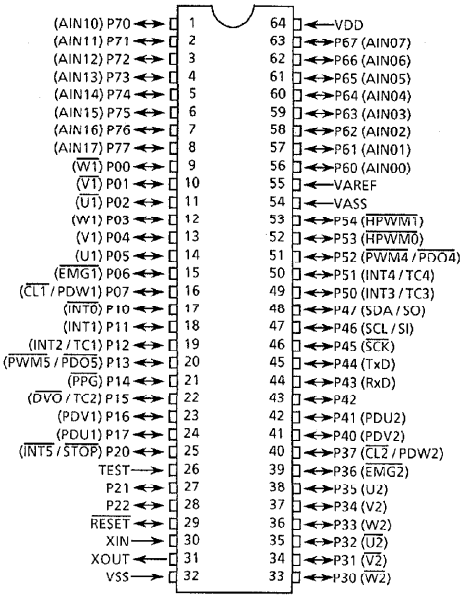
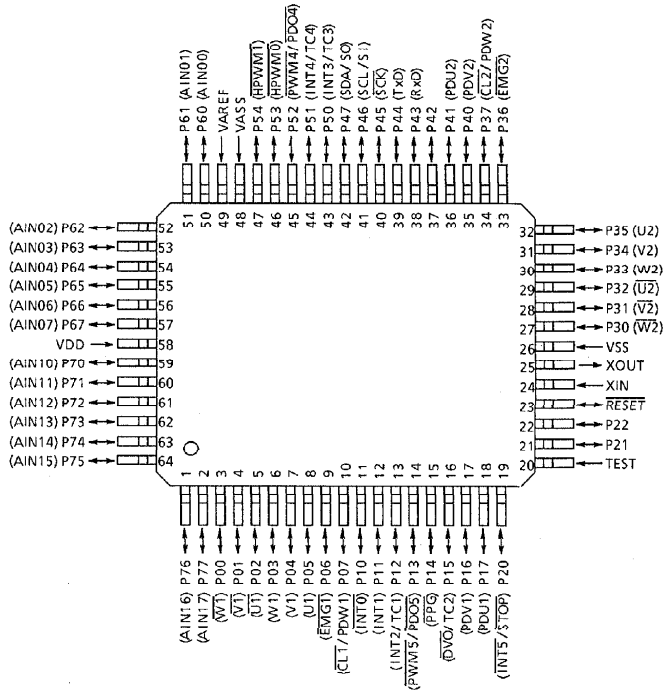
PIN ASSIGNMENTS

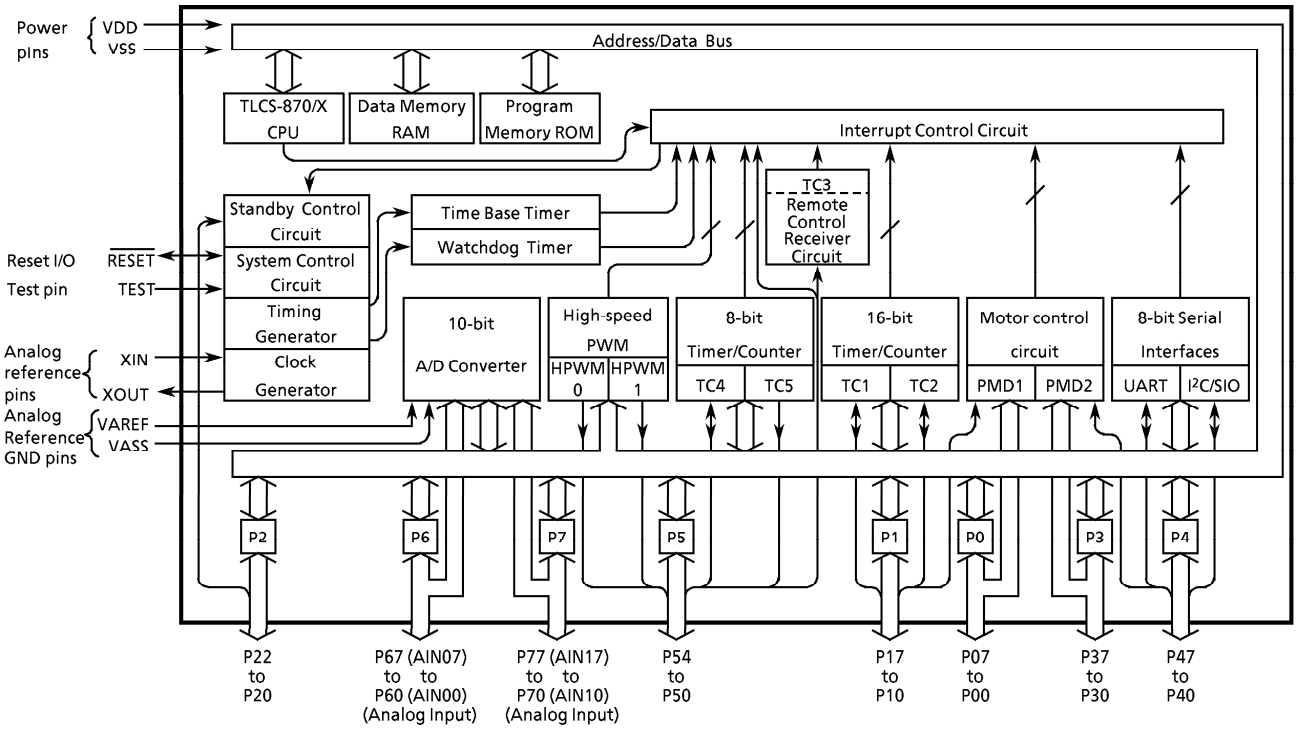
SDIP64-P-750-1.78



QFP64-P-1420-1.00A



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	I/O	FUNCTION	
P07 ($\overline{CL1}$/PDW1)	I/O (Input)	8-bit programmable I/O port (tri state) Input or output specifiable in units of bits. When using pins for motor control circuit, set accordingly using P0CR, then MDCR to 1.	Overload protection input 1/motor control circuit 1-phase position detection input
P06 ($\overline{EMG1}$)			Motor control circuit malfunction detection input 1
P05 (U1)	I/O (Output)		Motor control circuit U1-/V1-/W1-phase output
P04 (V1)			
P03 (W1)			
P02 ($\overline{U1}$)	I/O (Output)		Motor control circuit $\overline{U1}$-/ $\overline{V1}$-/$\overline{W1}$-phase output
P01 ($\overline{V1}$)			
P00 ($\overline{W1}$)			
P17 (PDU1)	I/O (Input)	8-bit programmable I/O port (tri state) Input or output specifiable units of bits. When using pins for motor control circuit, timer/counter input, or external interrupt input, set them to input mode. When using pins for PPG output, divider output, or PWM output/PDO output, set them to output mode.	Motor control circuit U1-phase position detection input
P16 (PDV1)			Motor control circuit V1-phase position detection input
P15 ($\overline{DVO}$/TC2)	II/O (Output/Input)		Divider output or timer/counter 2 input
P14 ($\overline{PPG}$)	I/O (Output)		Programmable pulse generator output
P13 ($\overline{PWM5}$/$\overline{PDO5}$)			$\overline{PWM5}$ output/$\overline{PDO5}$ output
P12 (INT2/TC1)	I/O (Input)		External interrupt input 2 or Timer/Counter 1 input
P11 ($\overline{INT1}$)			External interrupt input 1
P10 ($\overline{INT0}$)			External interrupt input 0
P22	I/O	3-bit I/O port When using pins for input port, external interrupt input, or STOP mode release input, set output latches to 1.	—
P21			—
P20 ($\overline{INT5}$/$\overline{STOP}$)	I/O (Input)		External interrupt input 5 or STOP mode release signal input
P37 ($\overline{CL2}$/PDW2)	I/O (Input)	8-bit I/O port (large-current output) When using pins for motor control circuit input, set output latches to 1, then MDCR2 to 1.	Overload protection input 2/motor control circuit W2-phase position detection input Motor control circuit malfunction detection input 2
P36 ($\overline{EMG2}$)			Motor control circuit malfunction detection input 2
P35 (U2)	I/O (Output)		Motor control circuit U2-/V2-/W2-phase output
P34 (V2)			
P33 (W2)			
P32 ($\overline{U2}$)	I/O (Output)		Motor control circuit $\overline{U2}$-/$\overline{V2}$-/$\overline{W2}$-phase output
P31 ($\overline{V2}$)			
P30 ($\overline{W2}$)			
P47 (SDA/SO1)	II/O (I/O/Output)	8-bit I/O port When using pins for motor control circuit input, UART/I²C/SIO, set output latches to 1.	I²C/SIO I/O
P46 (SCL1/SI1)	II/O (I/O/Input)		
P45 ($\overline{SCK}$)	I/O (I/O)		
P44 (TxD)	I/O (Input)		UART data input
P43 (RxD)	I/O (Output)		UART data output
P42	I/O		—
P41 (PDU2)	I/O (Input)		Motor control circuit U2-phase position detection input
P40 (PDV2)			Motor control circuit V2-phase position detection input

PIN NAME	Input/Output	FUNCTION	
P54 ($\overline{\text{HPWM1}}$)	I/O (Output)	5-bit input/output port with latch. When using pins for input port, HPWM output, PWM output/PDO output, external interrupt input, or timer/counter input, set output latches to 1.	High-speed PWM output
P53 ($\overline{\text{HPWM0}}$)			$\overline{\text{PWM4}}$ output/$\overline{\text{ODP4}}$ output
P52 ($\overline{\text{PWM4}}$/$\overline{\text{PDO4}}$)			8-BIT PWM output 4 or, 8-bit programmable divider output 4
P51 (INT4/TC4)	I/O (Input)		External interrupt 4 input or timer/counter 4 input
P50 (INT3/TC3)			External interrupt 3 input or timer/counter 3 input
P67 (AIN7) to P60 (AIN0)	I/O (Input)	8-bit programmable I/O port (tri state) Input or output specifiable in units of bits. When using pins for analog input, set to input mode using P6CR and ADCCR.	A/D converter analog input
P77 (AIN17) to P70 (AIN10)	I/O (Input)	8-bit programmable I/O port (tri state) Input or output specifiable in units of bits. When using pins for analog input, set to input mode using P7CR and ADCCR.	A/D converter analog input
XIN, XOUT	Input, Output	High-frequency oscillator connecting pins. For external clock input, input to XIN and leave XOUT open.	
$\overline{\text{RESET}}$	I/O	Reset signal input, watchdog timer output, address trap reset output, system clock reset output	
TEST	Input	Shipment test pin. Fix to low level.	
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)	
VAREF, VASS		Analog reference voltage for A/D conversion. Reference GND.	

OPERATION

1. CPU Core Functions

The CPU core consists of the CPU, system clock control circuit, and interrupt control circuit. This chapter describes the CPU core, program memory, data memory and the reset circuit.

1.1 Memory Address Map

The TMP88CK49/M49 memory consists of four blocks : ROM, RAM, special function registers (SFR) and Data buffer registers (DBR). They are all mapped to a 1M-byte address space. Figure 1-1 shows the TMP88CK49/M49 memory address map. There are 16 general-purpose registers mapped to the RAM address space.

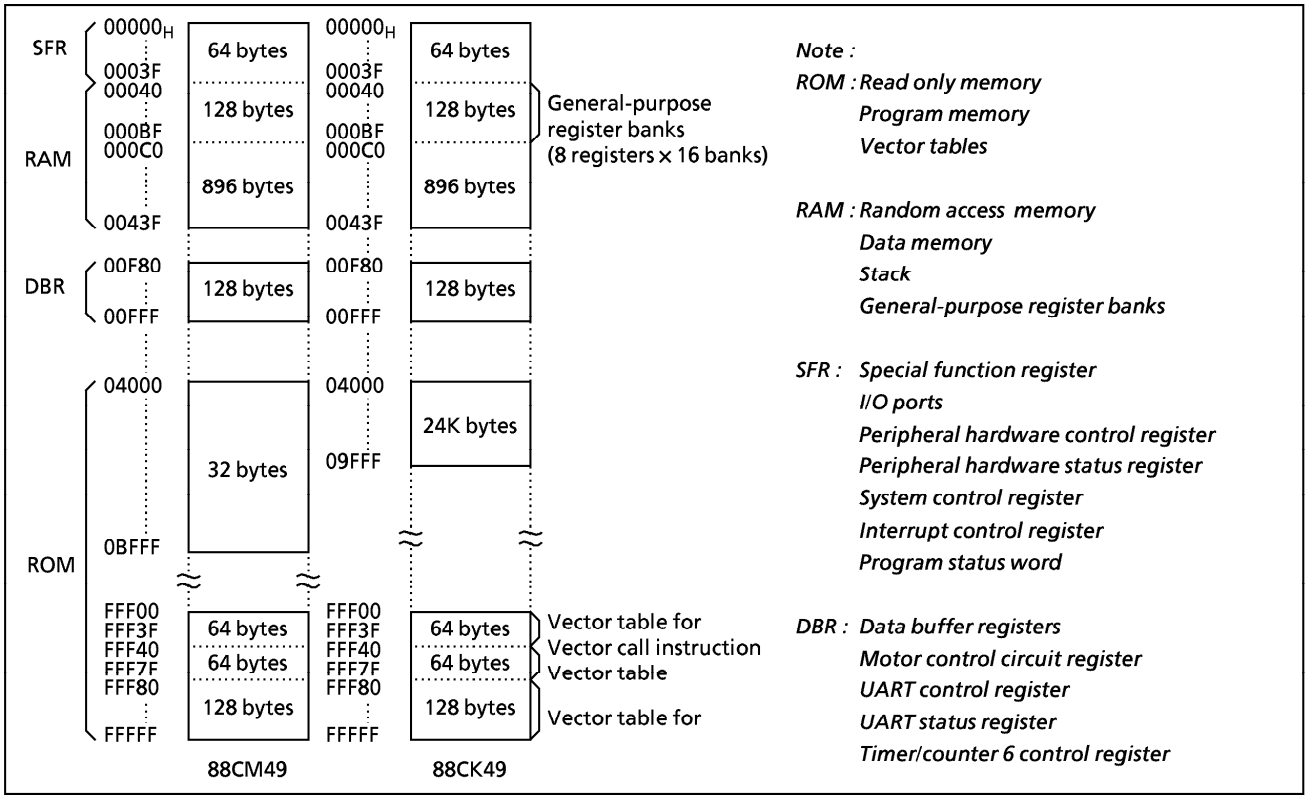


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

TMP88CK49 contains a 24K-byte program memory (mask ROM) at addresses from 04000 to $09EFF_H$.
TMP88CM49 contains a 32K-byte program memory (mask ROM) at addresses from 04000 to $0BEFF_H$.
In addition, both contain a 256-byte program memory (mask ROM) at addresses from FFF00 to $FFFFF_H$.

1.6 Reset circuit

TMP88CK49/M49 supports four types of reset generation: external reset input, address trap reset output, watchdog timer reset output, and system clock reset output.
Table 1-3 shows initialization of the internal hardware by reset.
At power on, the internal reset output circuits (watchdog timer reset, address trap reset, and system clock reset) are not initialized. Thus, at power on, the $\overline{\text{RESET}}$ pin may output low level for up to 24/fc [s] (1.5 μs, @ 16 MHz).

Table 1-4. Initialization of Internal Hardware by Reset

Internal hardware		Initial value	Internal hardware	Initial value
Program counter	(PC)	($FFFFC_H$ to $FFFFE_H$)	Timing generator prescaler and divider	0
Stack pointer	(SP)	Not initialized.		
General-purpose register	(WABCDEHL)	Not initialized.		
Register bank selector	(RBS)	0	Watchdog timer	Enable
Jump status flag	(JF)	1		
Zero flag	(ZF)	Not initialized.	I/O port output latch	See I/O port description.
Carry flag	(CF)	Not initialized.		
Half carry flag	(HF)	Not initialized.		
Sign flag	(SF)	Not initialized.		
Overflow flag	(VF)	Not initialized.		
Interrupt master enable flag	(IMF)	0		
Interrupt enable flag	(EF)	0	Control register	See control register description.
Interrupt latch	(IL)	0		
			RAM	Not initialized.

1.6.1 External Reset Input

The $\overline{\text{RESET}}$ pin has a pull-up resistor for hysteresis input. When the supply voltage is within the operating voltage and oscillation is stabilized, holding the $\overline{\text{RESET}}$ pin at low level for a minimum of 3 machine cycles (12/fc [s]) generates reset and initializes the internal states.
When the $\overline{\text{RESET}}$ pin input reaches high level, reset is released. Execution of the program starts from the vector address stored at addresses FFFFC to $FFFFE_H$.

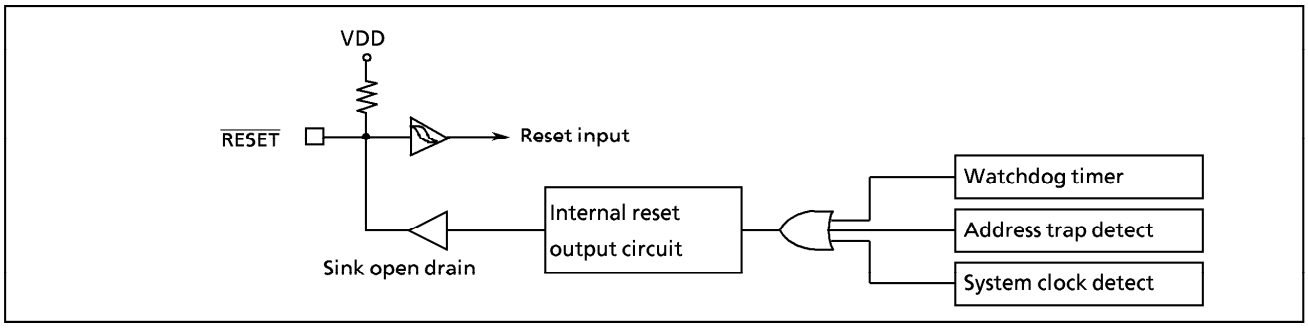
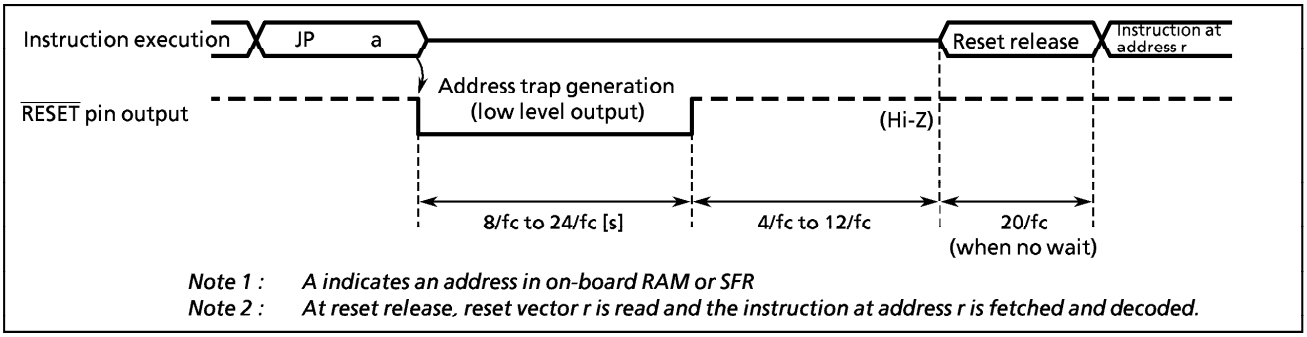


Figure 1-19. Reset Circuit

1.6.2 Address Trap Reset

When CPU runaway is caused by noise, for example, and an attempt is made to fetch an instruction from on-board RAM or the SFR, an internal reset is generated and a reset signal (low level) is output from the $\overline{\text{RESET}}$ pin. The reset signal is output for 8/fc to 24/fc [s] (0.5-1.5 μs @ 16 MHz)



Note 1 : A indicates an address in on-board RAM or SFR
Note 2 : At reset release, reset vector r is read and the instruction at address r is fetched and decoded.

Figure 1-20. Address Trap Reset

1.6.3 System Clock Rest

Zero-clearing bits 7 and 6 in SYSCR2 stops the system clock and causes MCU deadlock. To avoid deadlock, detecting that bits 7 and 6 in SYSCR2 are both set to 0 automatically generates a reset signal and continues oscillation. Reset signal is output from the $\overline{\text{RESET}}$ pin. Reset signal is output for 8/fc to 24/fc [s] (0.5 to 1.5 μs @ 16 MHz)

2. Peripheral Hardware Functions

2.1 Special Function Registers (SFR) and Data Buffer Registers (DBR)

The TLCS-870 series uses memory mapped I/O: peripheral hardware control and data transfer are performed using the special function registers (SFR) and data buffer registers (DBR).

SFRs are mapped to addresses 00000 to $0003F_H$; DBR, to addresses 00F80 to $00FBF_H$ and 00FFB to $00FFF_H$.

Figure 2-1 (a) shows the TMP88CK49/M49 SFRs; 2-1 (b), DBRs.

Address	Read	Write
00000_H	Port P0	
01	Port P1	
02	Port P2	
03	Port P3	
04	Port P4	
05	Port P5	
06	Port P6	
07	Port P7	
08	reserved	
09		
0A	–	P0CR (Port P0 I/O control)
0B	–	P1CR (Port P1 I/O control)
0C	–	P6CR (Port P6 I/O control)
0D	–	P7CR (Port P7 I/O control)
0E	ADCCR (A/D converter control)	
0F	ADCDR1 (Upper 8 bits of A/D conversion value)	
10	–	$TREG1A_L$ (Timer register 1A)
11	–	$TREG1A_H$
12	$TREG1B_L$ (Timer register 1B)	
13	$TREG1B_H$	
14	–	TC1CR (Timer/counter 1 control)
15	–	TC2CR (Timer/counter 2 control)
16	–	$TREG2_L$ (Timer register 2)
17	–	$TREG2_H$
18	TREG3A (Timer register 3A)	
19	TREG3B (Timer register 3B)	–
1A	–	TC3CR (Timer/counter 2 control)
1B	–	TREG4 (Timer register 4)
1C	–	TC4CR (Timer/counter 4 control)
1D		TREG5 (Timer register 5)
1E		TC5CR (Timer/counter 5 control)
1F	RCCR (Remote control)	

Address	Read	Write
00020_H	–	SBICR1 (SBI control 1)
21	SBIDBR (SBI data buffer)	
22	–	I2CAR (I^2C bus address)
23	SBISR (SBI status)	SBICR2 (SBI control 2)
24	ADCDR2L (Lower 8 bits of A/D conversion value)	
25	ADCDR2H (Lower 2 bits of A/D conversion value)	
26	HPWMCR (HPWM control)	
27	–	HPWMDR1 (HPWM1 data)
28	–	HPWMDR2 (HPWM2 data)
29	–	
2A	–	
2B	EIRC (Extended interrupt enable register/extended interrupt latch)	
2C	EIRE (Extended interrupt enable register lower)	
2D	EIRD (Extended interrupt enable register upper)	
2E	ILE (Extended interrupt latch lower)	
2F	ILD (Extended interrupt latch upper)	
30	reserved	
31	reserved	
32	reserved	
33	reserved	
34	–	WDTCR1 (WDT control 1)
35	–	WDTCR2 (WDT control 2)
36	TBTCR (TBT/TG/divider output control)	
37	EINTCR (External interrupt input control)	
38	SYSCR1 (System control 1)	
39	SYSCR2 (System control 2)	
3A	EIRL	(Interrupt enable register)
3B	EIRH	
3C	ILL	(Interrupt latch)
3D	ILH	
3E	PSWL	(Program status word)
3F	PSWH	

Figure 2-1 (a). Special Function Registers

PMD

Address		Read	Write
Channel 1	Channel 2		
$00F80_H$	$00FA0_H$	PDCRA (Position detect control register)	
00F81	00FA1	PDCRB	
00F82	00FA2	SDREG (Sampling delay control register)	
00F83	00FA3	CMPCR (Compare control register)	
00F84	00FA4	MTCRA (Mode timer control register)	
00F85	00FA5	MTCRB	
00F86	00FA6	MCAPA (Mode capture register)	—
00F87	00FA7	MCAPB	—
00F88	00FA8	CMP1A (Compare register 1)	
00F89	00FA9	CMP1B	
00F8A	00FAA	CMP2A (Compare register 2)	
00F8B	00FAB	CMP2B	
00F8C	00FAC	CMP3A (Compare register 3)	
00F8D	00FAD	CMP3B	
00F8E	00FAE	CMP4A (Compare register 4)	
00F8F	00FAF	CMP4B	
00F90	00FB0	EMGCRA (EMG control register)	
00F91	00FB1	EMGCRB	
00F92	00FB2	DTR (Dead time register)	
00F93	00FB3	MDCR (PMD control register)	
00F94	00FB4	MDOUTA (PWD output register)	
00F95	00FB5	MDOUTB	
00F96	00FB6	MDCNTA (PMD counter)	EMGREL (EMG release register)
00F97	00FB7	MDCNTB	—
00F98	00FB8	CMPUA (PMD compare register)	
00F99	00FB9	CMPUB	
00F9A	00FBA	CMPVA (PMD compare register)	
00F9B	00FBB	CMPVB	
00F9C	00FBC	CMPWA (PMD compare register)	
00F9D	00FBD	CMPWB	
00F9E	00FBE	MDPRDA (PMD period register)	
00F9F	00FBF	MDPRDB	

UART, TC6

Address	Read	Write
$00FFB_H$	RDBUF (UART receive buffer)	TDBUF (UART transmit buffer)
C	UARTSR (UART status register)	UARTCR1 (UART control 1)
D	—	UARTCR2 (UART control 2)
E	—	TREG6 (Timer register 6)
F	—	TC6CR (Timer/counter 6 control)

Figure 2-1 (b). Data Buffer Registers

2.2 I/O Ports

TMP88CK49/M49 features eight built-in I/O ports (56 pins).

① Port P0 : 8-bit I/O port (also used for motor control circuit I/O)
② Port P1 : 8-bit I/O port (also used for external interrupt, timer/counter I/O, divider output, and motor control circuit input)
③ Port P2 : 3-bit I/O port (also used for external interrupt and STOP mode release signal input)
④ Port P3 : 8-bit I/O port (also used for motor control circuit I/O)
⑤ Port P4 : 8-bit I/O port (also used for serial interface I/O and motor control circuit input)
⑥ Port P5 : 5-bit I/O port (also used for external interrupt input and timer/counter I/O)
⑦ Port P6 : 8-bit I/O port (also used for analog input)
⑧ Port P7 : 8-bit I/O port (also used for analog input)

All output ports have built-in latches in which data are held. Input ports do not have latches; thus, data should be held externally until read externally, or held after more than one read. Figure 2-2 shows data input and output timings.
External data are read from I/O ports at the S1 state of the read cycle at instruction execution. This timing cannot be checked externally; thus, transient input data such as chattering should be handled by program. Data are output to I/O ports at the S2 state of the write cycle at instruction execution.

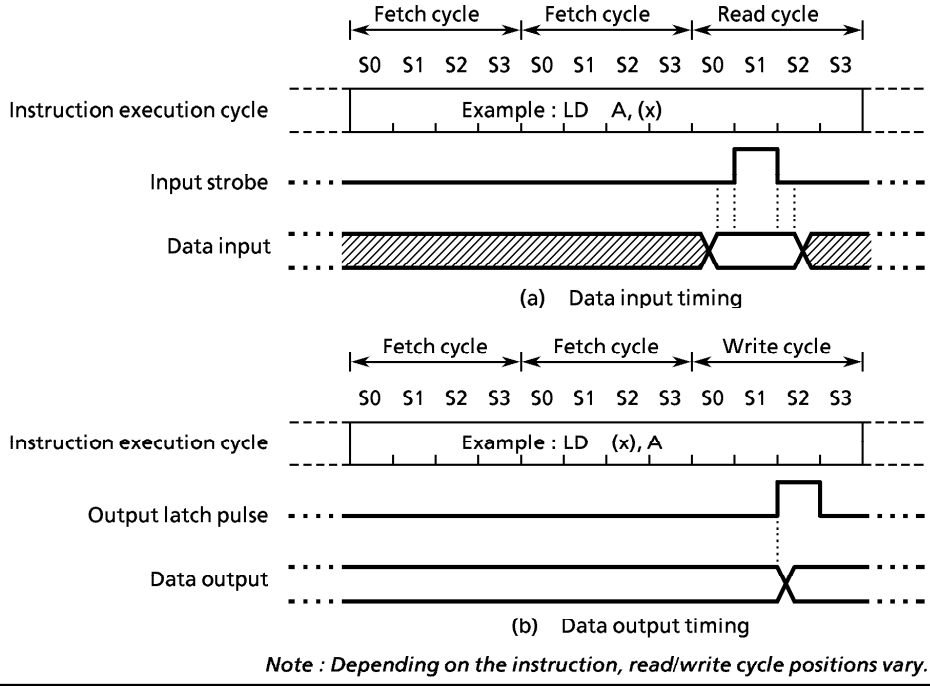


Figure 2-2. Examples of Data Input and Output Timings

When data are read from an I/O port other than a programmable I/O port, whether pin input values or output latch data are read depends on the instruction as follows.

(1) **Instructions which read output latch data:**

① XCH r, (src)
② SET/CLR/CPL (src). b
③ SET/CLR/CPL (pp). g
④ LD (src). b, CF
⑤ LD (pp). b,CF
⑥ XCH CF, (src).b
⑦ ADD/ADDC/SUB/SUBB/AND/OR/XOR (src), n
⑧ ADD/ADDC/SUB/SUBB/AND/OR/XOR (src)-side for ADD/ADDC/SUB/SUBB/AND/OR/XOR (src), (HL) instructions.
⑨ MXOR (src), m

(2) **Instructions which read pin input values:**

Instructions other than (1) above, and (HL)-side for ADD/ADDC/SUB/SUBB/AND/OR/XOR (src), (HL) instructions.

2.2.1 Port P0 (P07-P00)

Port P0 is an 8-bit general-pupose I/O port whose input or output is specifiable in units of bits. Specify input or output using the Port P0 I/O control register (P0CR). At reset, P0CR is initialized to 0, port P0 is set to input mode, and the port P0 output latches are initialized to 0.

Note : With ports set to input mode, pin input values are read. When a port is used for both input and output modes, data in the output latches set to input mode may be overwritten by execution of a bit manipulation instruction.

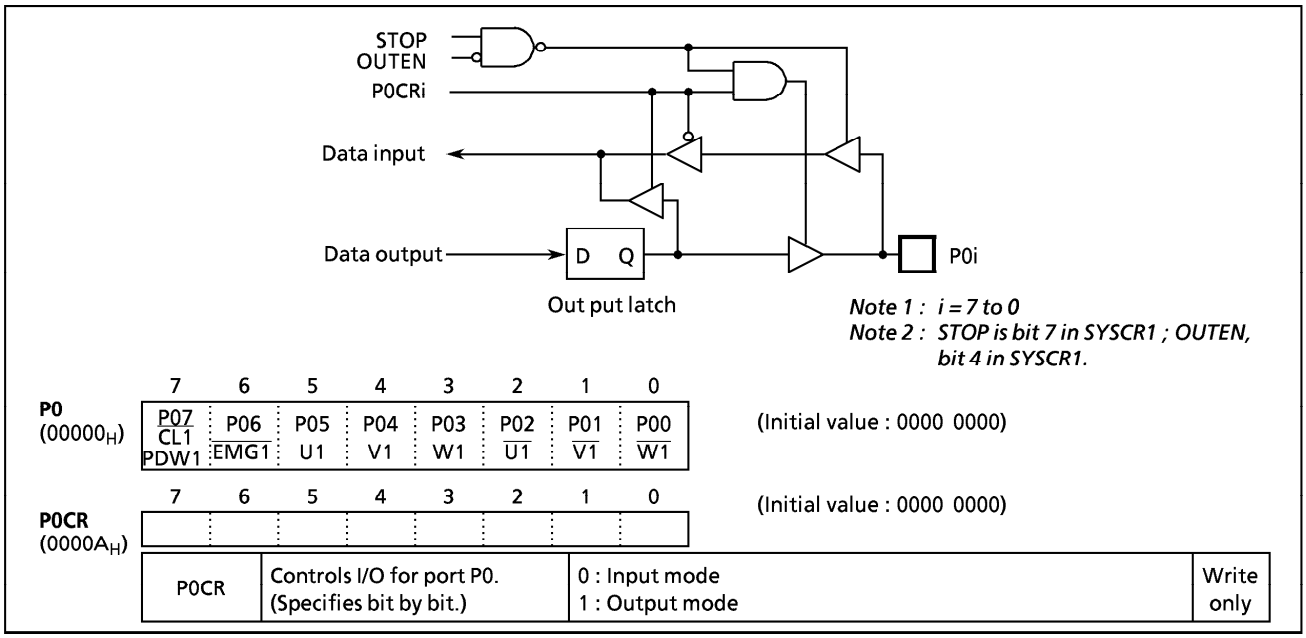


Figure 2-3. Port P0 and Port P0 I/O Control Register

Example : Set upper 4 bits of port P0 to input mode and lower 4 bits to output mode. The initial output value is 1010B.

```
LD      (P0), 00001010B     ;  Sets initial value for port P0 output latches.
LD      (P0CR), 00001111B   ;  Sets I/O mode for port P0.
```

2.2.2 Port P1 (P17-P10)

Port P1 is an 8-bit port whose input or output is specifiable in units of bits. Specify input or output using the Port P1 I/O control register (P1CR). At reset, P1CR is initialized to 0, port P1 is set to input mode, and the port P1 output latches are initialized to 0.

To use port P1 pins as function pins, set the input pins to input mode. For output mode, set the output latches for the output pins to 1. We recommend you use the P11 and P12 pins for external interrupt input, timer/counter input or as an input port. (If used as an output port, the interrupt latches are set by a rising or falling edge.) The P10 pin can be used for either I/O port or external interrupt input according to the external interrupt control register (INT0EN). At reset, the P10 pin is set to an input port.

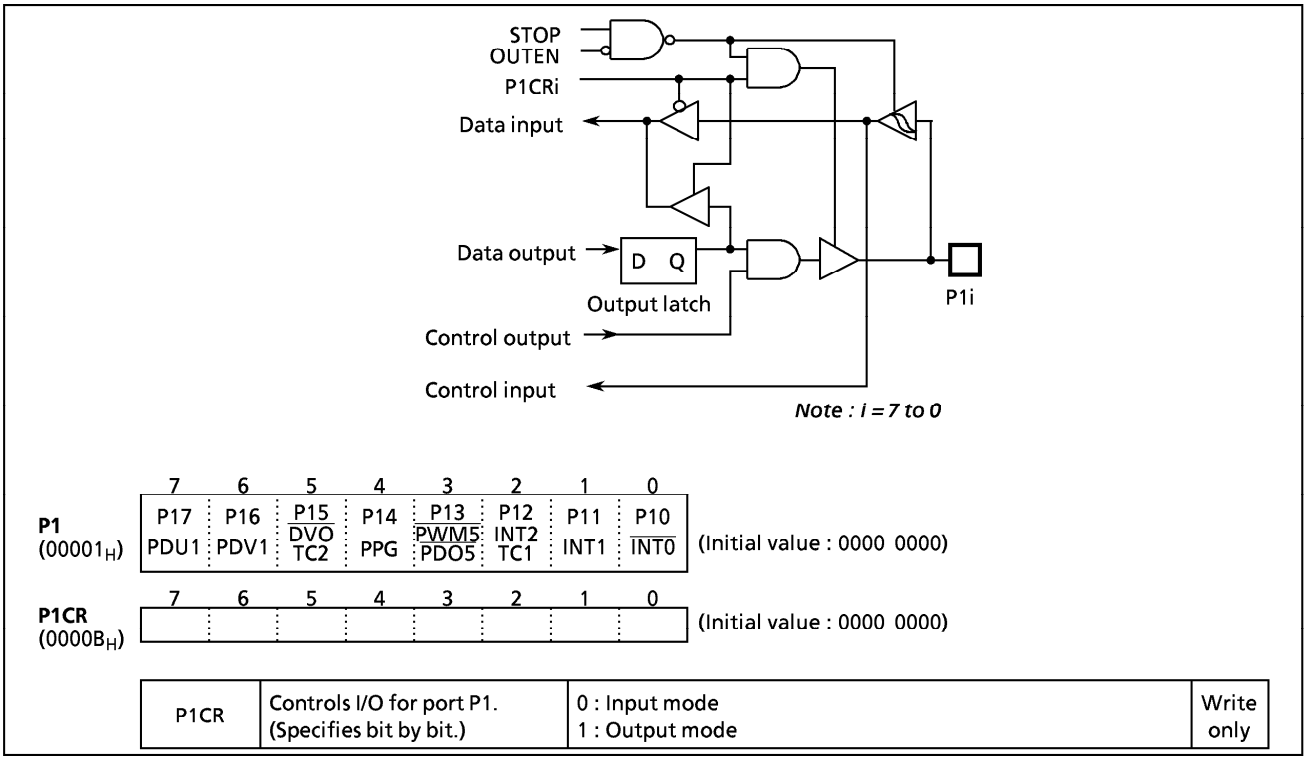


Figure 2-4. Port P1 and Port P1 I/O Control Register

Example : Set P17 and P16 to an output port, P13 and P11 to an input port, the other pins as function pins. P17 outputs 1 and P16 outputs 0.

```
LD      (EINTCR), 01000000B     ;  INT0EN←1
LD      (P1), 10111111B         ;  P17←1, P14←1, P16←0
LD      (P1CR), 11010000B
```

Note : With ports set to input mode, pin input values are read. When a port is used for both input and output modes, data in the output latches set to input mode may be overwritten by execution of a bit manipulation instruction.

2.2.3 Port P2 (P22-P20)

Port P2 is a 3-bit I/O port. It is also used for external interrupt input, and STOP mode release signal. To use port P2 as function pins or an input port, set the output latches to 1. At reset, the output latches are initialized to 1.

We recommend that the P20 pin be used for external interrupt input, STOP mode release signal input, or input port. (If used as an output port pin, the interrupt latch is set at a falling edge.)

When the read instruction is executed for port P2, undefined values are read from bits 7 to 3.

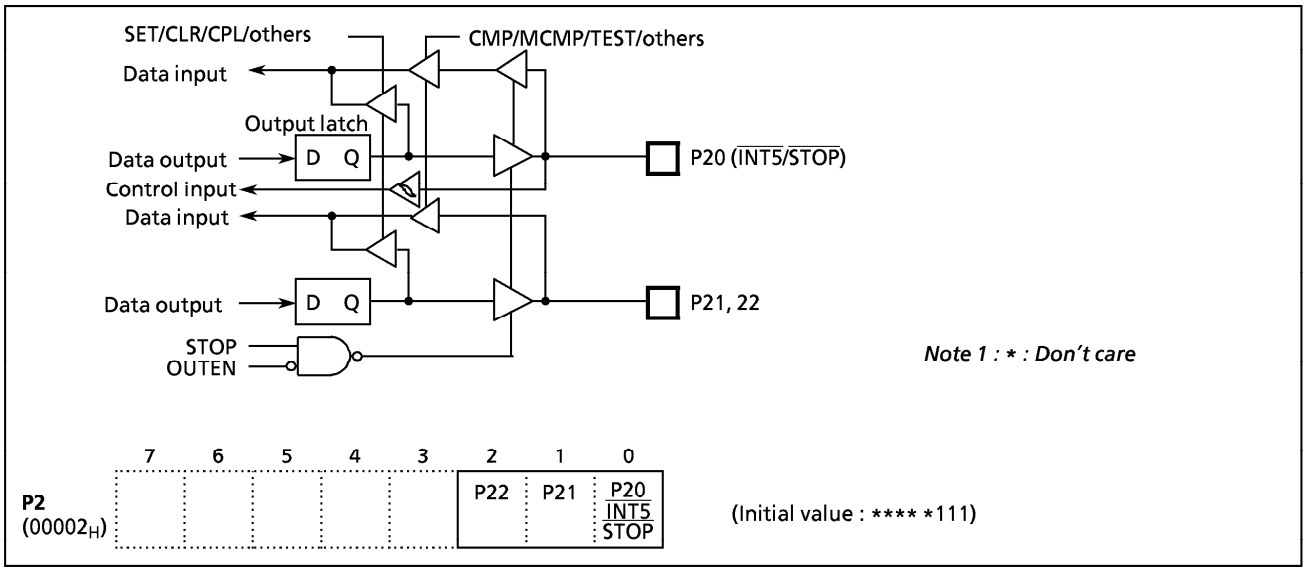


Figure 2-5. Port P2

2.2.4 Port P3 (P37-P30)

Port P3 is an 8-bit I/O port whose input or output is specifiable in units of bits. The port can handle a large output current to enable direct drive of LEDs. At reset, the port P3 output latches are initialized to 1.

Example 1 : Output immediate value 5AH from port P3.

```
LD      (P3), 5AH       ;  P3←5AH
```

Example 2 : Invert output or upper 4 bits (P37 to P34) in port P3.

```
XOR     (P3), 11110000B ;  P37 to P34←P37 to P34
```

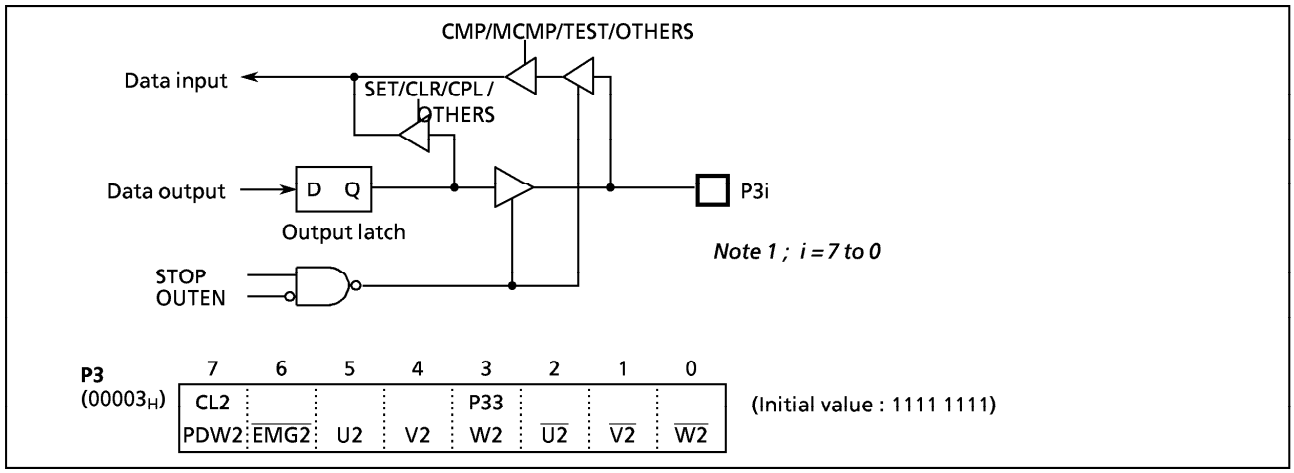


Figure 2-6. Port P3

2.2.5 Port P4 (P47 and P40)

To use port P4 as an input port or as function pins, set the output latches to 1. At reset, the port P4 output latches are initialized to 1.

2.2.6 Port P5 (P54-P50)

Port P5 is a 5-bit I/O port. To use port P5 as input pins or function pins, set the output latches to 1. At reset, the port P5 output latches are initialized to 1.

When the read instruction is executed for port P5, 1s are read from bits 7 to 5.

Example : Clear the P53 pin (low-level output)

```
CLR     (P5). 3         ;  P53←0
```

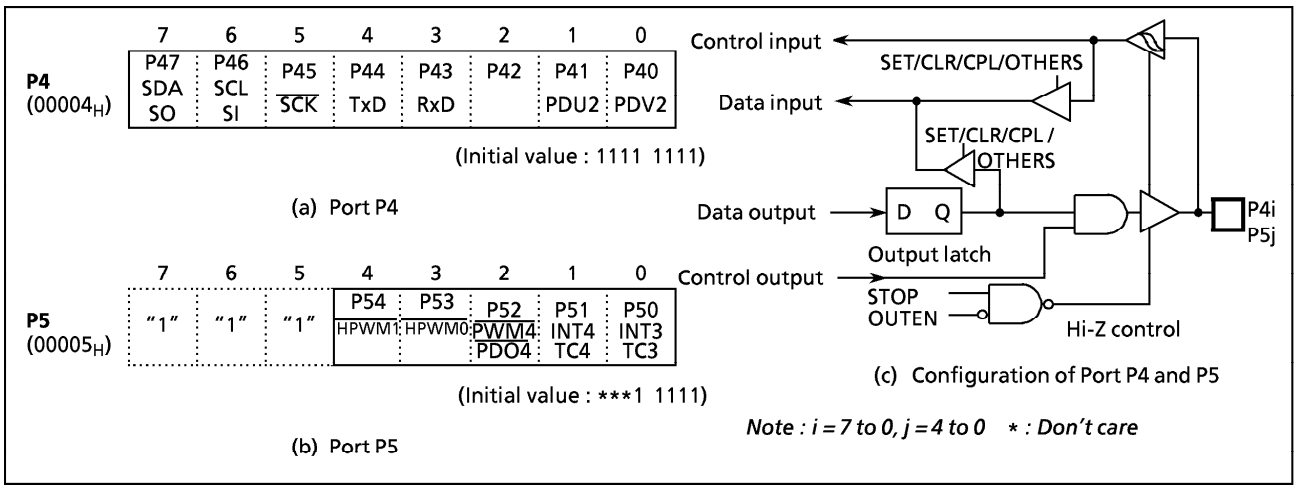
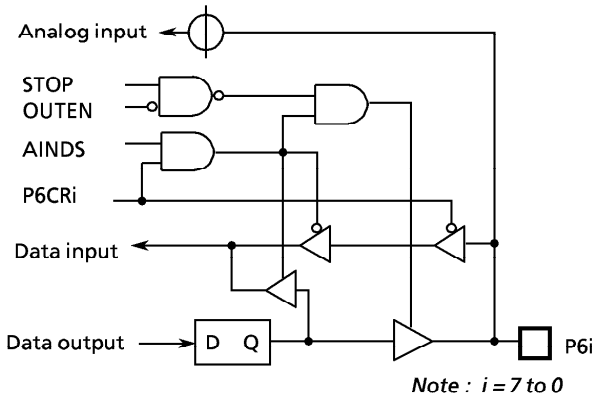


Figure 2-7. Port P4 and P5

2.2.7 Port P6 (P67 to P60)

Port P6 is an 8-bit I/O port whose input or output is specifiable in units of bits. Port P6 is also used for analog input. Specify input or output using the port P6 I/O control register (P6CR) and AINDS (bit 4 in ADCCR).

At reset, P6CR is set to 1; AINDS is cleared to 0 ; thus, port P6 is set to analog input. At reset, the port P6 output latches are initialized to 0. P6CR is a write-only register. When using the A/D converter, the port P6 pins not used for analog input can only be used as input port pins.



P6 (00006_H)

7	6	5	4	3	2	1	0
P67 AIN07	P66 AIN06	P65 AIN05	P64 AIN04	P63 AIN03	P62 AIN02	P61 AIN01	P60 AIN00

(Initial value : 0000 0000)

P6CR ($0000C_H$)

7	6	5	4	3	2	1	0

(Initial value : 1111 1111)

P6CR	Controls I/O for port P6. (Specifies bit by bit.)	AINDS = 1 (A/D not used) 0 : Input mode 1 : Output mode	AINDS = 0 (A/D used) 0 : Input port 1 : Analog input	Write only

Figure 2-8. Port P6 and Port P6 I/O Control Register

2.2.8 Port P7 (P77 to P70)

Port P7 is an 8-bit I/O port whose input or output is specifiable in units of bits. Port P7 is also used for analog input. Specify input or output by port P7 I/O control register (P7CR) and AINDS (bit 4 in ADCCR). At reset, P7CR is cleared to 1, AINDS to 0. At reset, the port P7 output latches are initialized to 0. P7CR is a write-only register. When using the A/D converter, the port pins not used for analog input can only be used as input port pins.

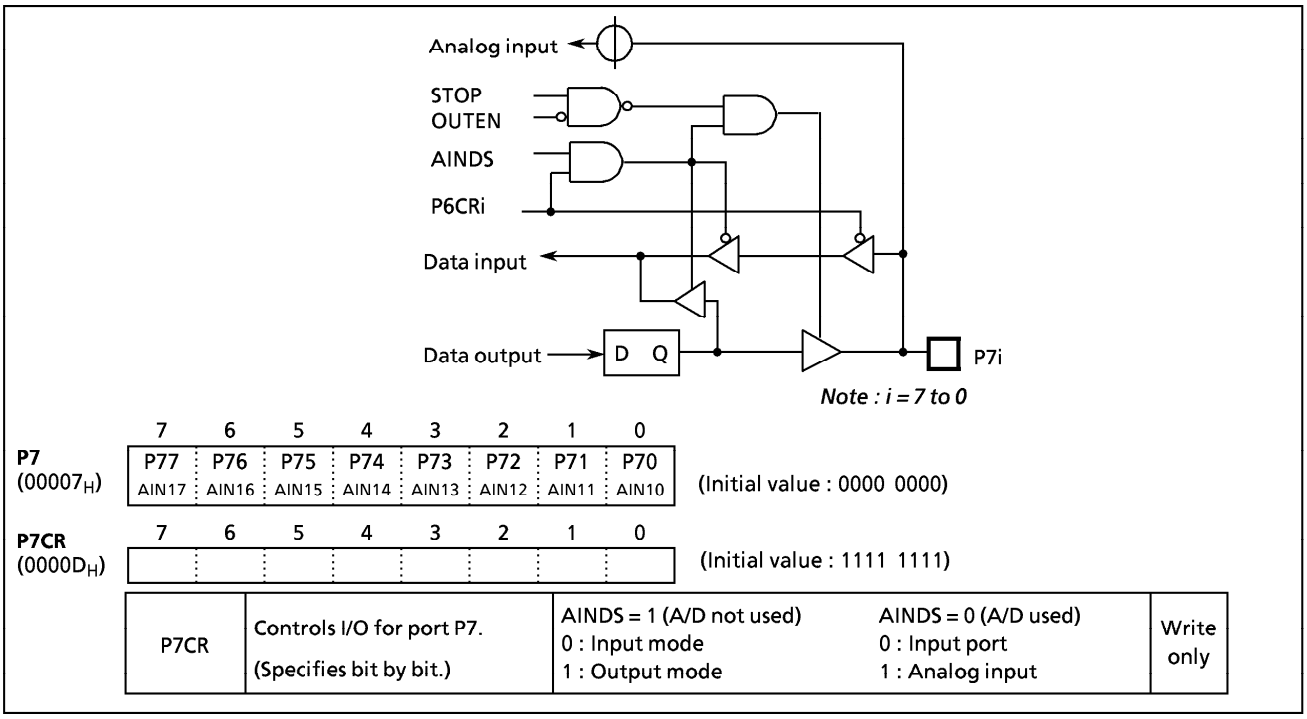


Figure 2-9. Port P7 and Port P7 I/O Control Register

Note : With ports set to input mode, pin input values are read. When a port is used for both input and output modes, data in the output latches set to input mode may be overwritten by execution of a bit manipulation instruction.

Example : Set the lower 4 bits of port P7 to an output port and the remaining bits to an input port.

```
LD      (P7CR), 0FH      ;  P7CR←00001111
```

2.3 Time Base Timer (TBT)

The time base timer is the reference time generation timer for key scan and dynamic display processing; it generates the time base timer interrupt (INTBT) at a fixed cycle.

After the time base timer is enabled, time base timer interrupts are generated at the first rising edge of the source clock (select timing generator divider output using TBTCK). Sine the divider is not cleared by program, only the first interrupt may be generated before the set interrupt cycle. (Figure 2-10 (b))

Select the interrupt frequency with the time base timer disabled. (When switching to timer disabled from timer enabled, do not change the set interrupt frequency.) Note that selecting the frequency and enabling the time base timer can be performed simultaneously.

Example : Set time base timer interrupt frequency to fc/216 [Hz] and enable interrupts.

```
LD      (TBTCR), 00001010B
SET     (EIRL). 6
```

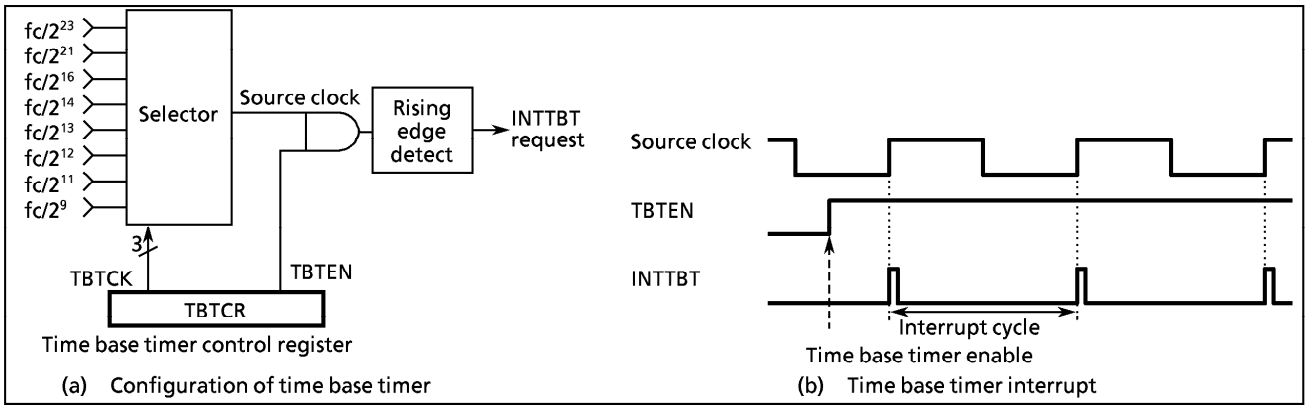


Figure 2-10. Time Base Timer

Time base timer control register

TBTCR (00036_H)

7	6	5	4	3	2	1	0
(DVOEN)	(DVOCK)		(DV7CK)	TBTEN	TBTCK		

(Initial value : 0**0 0***)

TBTEN	Enables/disables time base timer	0 : Disable 1 : Enable	R/W
TBTCK	Selects time base timer interrupt frequency. unit : Hz	000 : $fc/2^{23}$ 001 : $fc/2^{21}$ 010 : $fc/2^{16}$ 011 : $fc/2^{14}$ 100 : $fc/2^{13}$ 101 : $fc/2^{12}$ 110 : $fc/2^{11}$ 111 : $fc/2^{9}$	

*Note : fc : High frequency clock [Hz] * : Don't care*

Figure 2-11. Time Base Timer Control Register

Table 2-1. Time Base Timer Interrupt Frequency (When fc = 16MHz)

TBTCK	Time base timer interrupt frequency [Hz]
000	1.91
001	7.63
010	244.14
011	976.56
100	1953.12
101	3906.25
110	7812.50
111	31250

2.4 Watchdog Timer (WDT)

The watchdog timer is a fail-safe function, which detects misoperation (runaway) of the CPU caused by, for example, noise or deadlock, and returns it to normal operation.

Runaway signals detected by the watchdog timer, selectable by program, can be either reset output or pseudo non-maskable interrupt request. Note that this selection can be mode only once. At reset release, initialized to reset output.

When the watchdog timer is not used for detecting runaway, it can be used as a timer which generates interrupts at a fixed cycle.

2.4.1 Configuration of Watchdog Timer

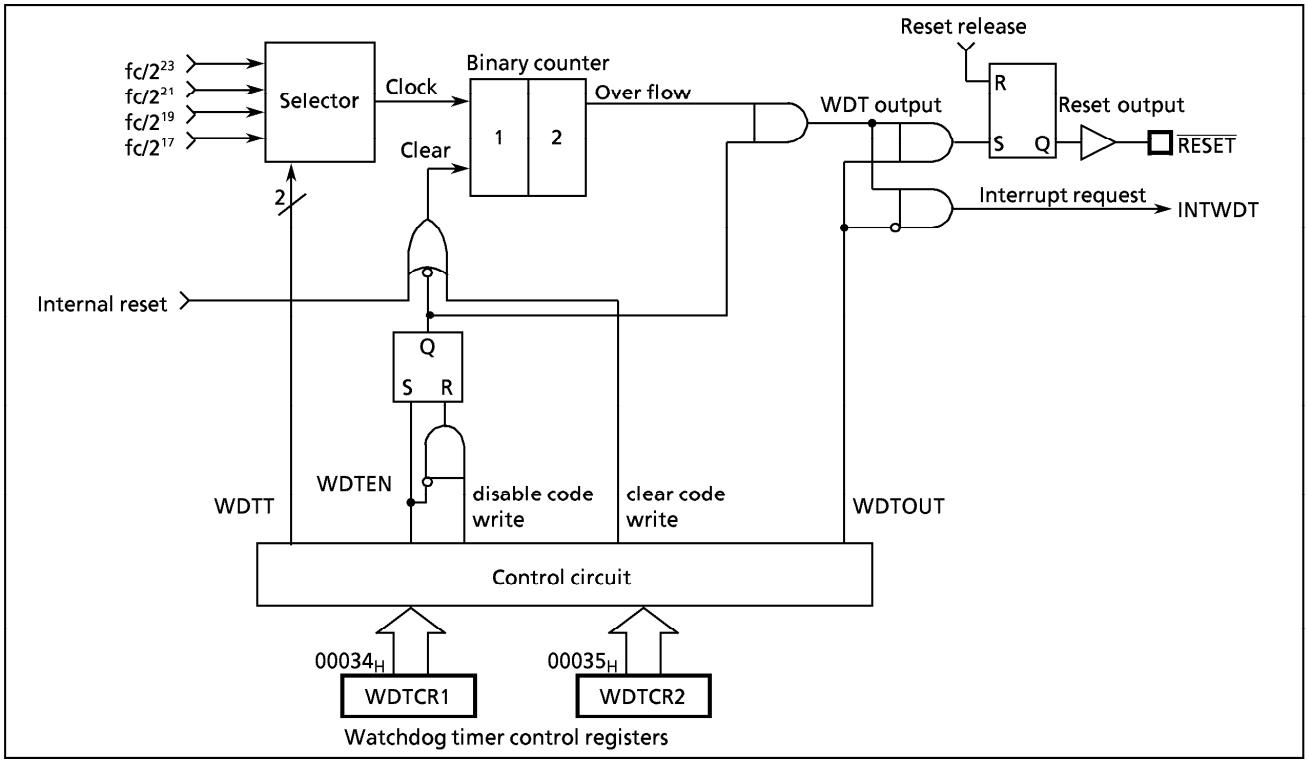


Figure 2-12. Configuration of Watchdog Timer

2.4.2 Watchdog Timer Control

Figure 2-13 shows the watchdog timer control registers. Releasing reset enables the watchdog timer.

(1) **How to detect runaway using the watchdog timer**

CPU runaway is detected as follows:

① Set detection time, select output, and clear the binary counter.

② Repeat clearing of the binary counter within every set detection time.

If runaway or deadlock occurs, and the binary counter is not cleared, the binary counter overflows causing the watchdog timer output (WDTOUT) to be active. At this time, if WDTOUT = 1, reset signals are output from the $\overline{\text{RESET}}$ pin and the internal hardware is reset. If WDTOUT = 0, a watchdog timer interrupt (INTWDT) is generated.

In STOP (including warm up) or IDLE mode, the watchdog timer temporarily stops counting. Releasing STOP or IDLE mode automatically restarts the watchdog timer.

Example : Set watchdog timer detection time to 2^{21}/fc [s] and resets runaway detection.

```
        LD      (WDTCR2), 4EH           ; Clears binary counter.
        LD      (WDTCR1), 00001101B     ; WDTT←10, WDTOUT←1
        LD      (WDTCR2), 4EH           ; Clears binary counter.
Within WDT                              (Always clears immediately before and
detection                               after WDTT change.)
time
        LD      (WDTCR2), 4EH           ; Clears binary counter.
Within WDT
detection
time
        LD      (WDTCR2), 4EH           ; Clears binary counter.
```

Watchdog timer control register 1

WDTCR1 (00034_H)

7	6	5	4	3	2	1	0
				WDT EN	WDTT		WDT OUT

(Initial value : **** 1001)

WDTEN	Enables/Disables watchdog timer.	0 : Disable (Write disable code in WDTCR2.) 1 : Enable	Write only
WDTT	Sets watchdog timer detection time unit : s	00 : 2^{25}/fc 01 : 2^{23}/fc 10 : 2^{21}/fc 11 : 2^{19}/fc	
WDTOUT	Selects watchdog timer output.	0 : Interrupt request 1 : Reset output	

Note 1 : Once WDTOUT is zero-cleared, it cannot be set to 1 again by program.
*Note 2 : fc : High-frequency clock [Hz] * : Don't care*
Note 3 : WDTCR1 is write-only. Read-modify-write instructions such as bit manipulation cannot access it.
Note 4 : Disable the watchdog timer or clear the counter just before switching to STOP mode. When the counter is cleared just before switching to STOP mode, clear the counter again subsequently to releasing STOP mode.

Watchdog timer control register 2

WDTCR2 (00035_H)

7	6	5	4	3	2	1	0

(Initial value : **** ****)

WDTCR2	Writes watchdog timer control code.	$4E_H$: Clears watchdog timer binary counter. (clear code) $B1_H$: Disables watchdog timer. (disable code) Other : Invalid	Write only

Note 1 : Disable code invalidates write other than when WDTEN = 0
*Note 2 : * : Don't care*
Note 3 : Do not clear the WDT binary counter using the interrupt task.

Figure 2-13. Watchdog Timer Control Registers

(2) **Watchdog timer enable**

Setting 1 in WDTEN (bit 3 in WDTCR1) enables the watchdog timer. Resetting initializes WDTEN to 1; thus, releasing reset immediately starts the watchdog timer.

(3) **Watchdog timer disable**

Zero-clearing WDTEN (bit 3 in WDTCR1) and writing disable code ($B1_H$) in WDTCR2 disables the watchdog timer. Note that first writing disable code in WDTCR2 then zero-clearing WDTEN do not disable the watchdog timer. While the watchdog timer is disabled, the watchdog timer binary counter is cleared.

Example : Disable watchdog timer.

```
LDW     (WDTCR1), 0B101H        ;  WDTEN←0, WDTCR2←disable code
```

Table 2-2. Watchdog Timer Detection Time (When fc = 16 MHz)

WDTT	Watchdog Timer Detection Time [s]
00	2.097
01	524.288 m
10	131.072 m
11	32.768 m

2.4.3 Watchdog Timer Interrupt (INTWDT)

Watchdog timer interrupts are pseudo non-maskable. They are accepted regardless of the contents in the interrupt enable register. However, if another watchdog timer interrupt or software interrupt is being processed, the new watchdog timer interrupt must wait until processing of the current interrupt is complete (RETN instruction execution completes).

Set the stack pointer before setting watchdog timer output as the interrupt source in WDTOUT.

Example : Set Watchdog timer interrupt.

```
LD      SP, 0043FH              ;  Sets SP.
LD      (WDTCR1), 00001000B     ;  WDTOUT←0
```

2.4.4 Watchdog Timer Reset

Low level is output from the $\overline{\text{RESET}}$ pin and, at the same time, internal hardware is reset. Reset timer is 8/fc to 24/fc [s] (0.5 to 1.5 μs at fc = 16 MHz). The $\overline{\text{RESET}}$ pin is sink open-drain I/O with a pull-up resistor.

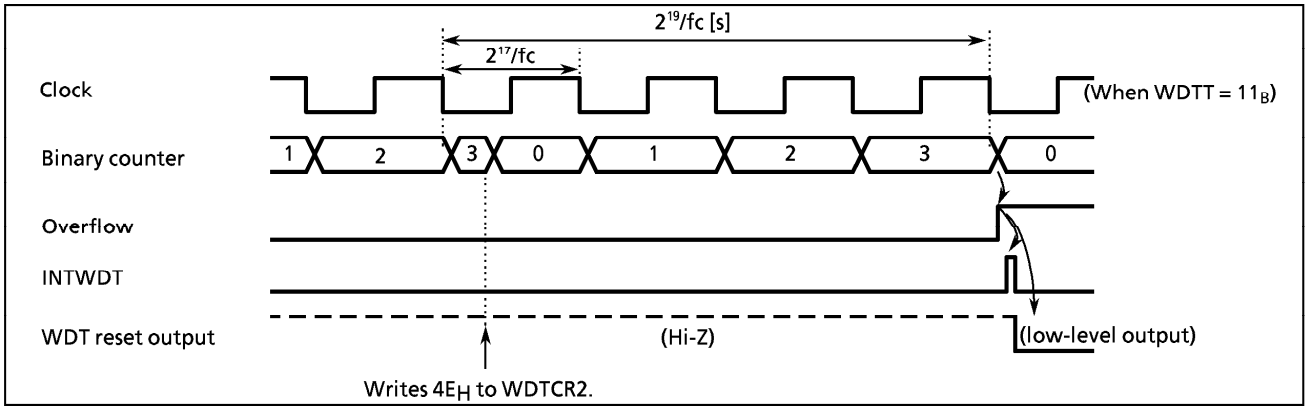


Figure 2-14. Watchdog Timer Interrupt and Reset

2.5 Divider Output ($\overline{DVO}$)

The timing generator divider outputs approx. 50 %-duty pulses, which can be used for driving a buzzer. The pulses are output to the P15 ($\overline{DVO}$) pin. First set the output latch for P15 to 1, then set it to output mode.

Timing generator control register

TBTCR (00036_H)

7	6	5	4	3	2	1	0
DVOEN	DVOCK		(DV7CK)	(TBTEN)	(TBTCK)		

(Initial value : 0**0 0***)

DVOEN	Enables/disables divider output.	0 : Disable 1 : Enable	R/W
DVOCK	Selects divider output ($\overline{DVO}$ pin) frequency.	00 : $fc/2^{13}$ 01 : $fc/2^{12}$ 10 : $fc/2^{11}$ 11 : $fc/2^{10}$	

*Note : fc : High-frequency clock [Hz] * : Don't care*

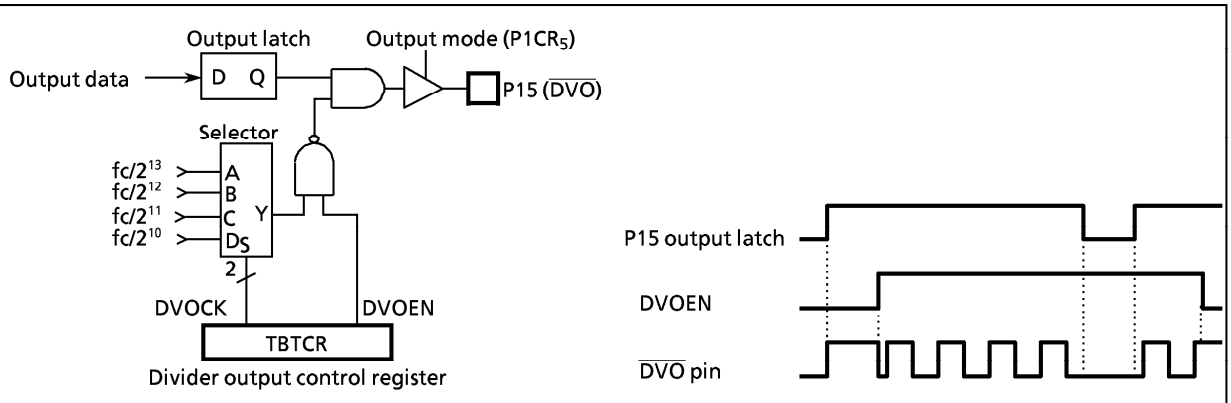
Figure 2-15. Divider Output Control Register

Example : Output 1.953 kHz pulses (when fc = 16 MHz).

```
SET     (P1). 5             ;  Sets P15 output latch to 1.
LD      (P1CR), 00100000B   ;  Sets P15 to output mode.
LD      (TBTCR), 10000000B  ;  DVOEN←1, DVOCK←00
```

Table 2-3. Divider output frequency (When fc = 16 MHz)

DVOCK	Divider output frequency [kHz]
00	1.953
01	3.906
10	7.812
11	15.625



(a) Configuration of divider output circuit (b) Divider output timing chart

Figure 2-16. Divider Output

2.7 16-Bit Timer/Counter 2 (TC2)

2.7.1 Configuration

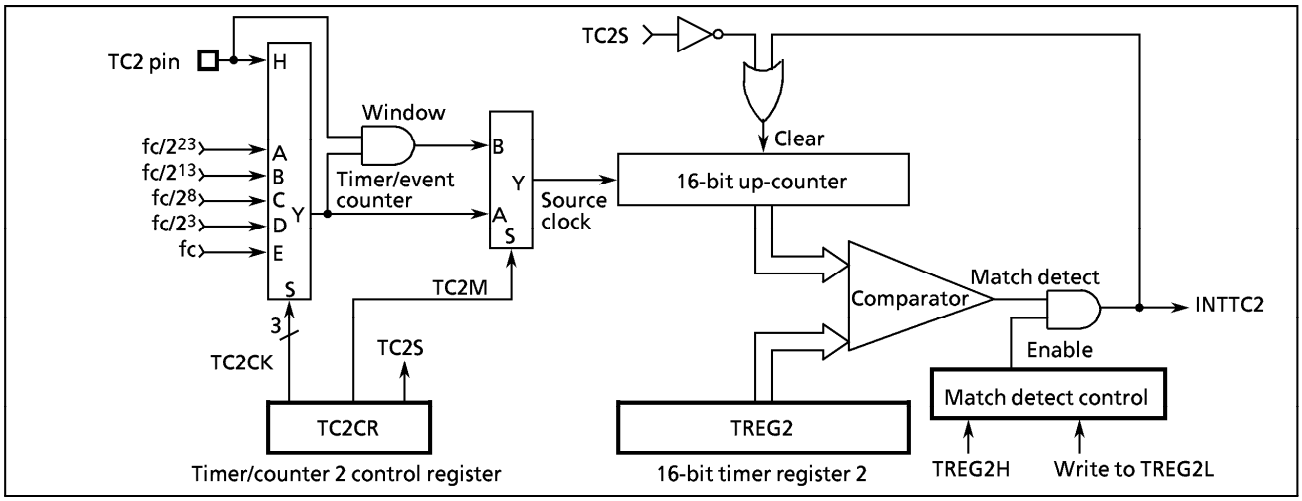


Figure 2-26. Timer/Counter 2 (TC2)

2.7.2 Control

Timer/counter 2 is controlled by timer/counter 2 control register (TC2CR) and 16-bit timer register 2 (TREG2).

Timer register 2

TREG2 (00016, 00017$_H$)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TREG2$_H$ (0017$_H$)								TREG2$_L$ (0016$_H$)							

Write only

Timer/counter 2 control register

TC2CR (00015$_H$)

7	6	5	4	3	2	1	0
		TC2S	TC2CK				TC2M

(Initial value : **00 00*0)

TC2M	Selects timer/counter 2 operating mode.	0 : Timer/event counter mode 1 : Window mode	Write only
TC2CK	Selects timer/counter 2 source clock.	000 : Internal clock fc/2^23 [Hz] 001 : 〃 fc/2^13 010 : 〃 fc/2^8 011 : 〃 fc/2^3 100 : reserved 101 : reserved 110 : reserved 111 : External clock (TC2 pin input)	
TC2S	Controls timer/counter 2 starts.	0 : Stops and clears TC2. 1 : Starts TC2.	

*Note 1 : fc : High-frequency clock [Hz] * : Don't care*

Note 2 : When writing to the lower bits (TREG2$_L$) starts, match detect stops temporarily until writing to the upper bits (TREG2$_H$) ends. Note that match detect is still ignored within 1 cycle after writing to the upper bis (during instruction execution).

Note 3 : Set mode and source clock with a stop (TC2S = 0) state.

Note 4 : The values set in the timer register must satisfy the following conditions.
TREG2 > 0 (TREG2$_{15\ to\ 1}$ 1 at warm up)

Note 5 : TC2CR is write-only. Do not access it using read-modify-write instructions such as bit manipulation.

Figure 2-27. Timer/Counter 2 Timer Register and Control Register

2.7.3 Functions

Timer/counter 2 supports three operating modes: timer, event counter, and window. When switching modes from SLOW to NORMAL, use timer/counter 2 in timer mode.

(1) **Timer mode**

TC2 counts up using the internal clock. A match between the counter value and the value set in timer register 2 (TREG2) generates INTTC2 and clears the counter. After the counter is cleared, it continues counting.

Table 2-5. Internal Clock Sources for Timer/Counter 2

Source clock	Resolution	Maximum set time
NORMAL or IDLE mode	When fc = 16 MHz	
$fc/2^{23}$ [Hz]	524 ms	9.5 ms
$fc/2^{13}$	512 μs	33.6 min
$fc/2^{8}$	16 μs	1.05 ms
$fc/2^{3}$	0.5 μs	32.75 ms

Example : Set to timer mode with source clock = $fc/2^3$ [Hz] and generate interrupts every 25 ms (fc = 16 MHz)

```
LDW     (TREG2), C350H      ;  Sets TREG2. (25 ms ÷ 2^3/fc = C350H)
SET     (EIRE). EF17        ;  Enables INTTC2.
EI
LD      (TC2CR), 00101100B  ;  Starts TC2.
```

(2) **Event counter mode**

TC2 counts up at the rising edge of input to the TC2 pin. A match between the counter value and the value set in TREG2 generates INTTC2 and clears the counter. The applicable maximum frequency for the TC2 pin is $fc/2^4$ [Hz] (in NORMAL or IDLE mode). For both high and low levels, the pulse width must be 2 machine cycles or more.

Example : Set to event counter mode and generate INTTC2 after 640 counts.

```
LDW     (TREG2), 640        ;  Sets TREG2.
SET     (EIRE). EF17        ;  Enables INTTC2.
EI
LD      (TC2CR), 00111100B  ;  Starts TC2.
```

(3) **Window mode**

TC2 counts up using the internal clock while input to the TC2 external pin (window pulse) is at high level. A match between the counter value and the value set in TREG2 generates INTTC2 and clears the counter. The applicable maximum frequency for the TC2 pin must be sufficiently slower than the set internal clock.

Example : When a high-level pulse of 120 ms or longer is input, generate an interrupt (when fc = 16 MHz).

```
LDW     (TREG2), 00EAH      ;  Sets TREG2. (120 ms ÷ 2^13/fc = 00EAH)
SET     (EIRE). EF17        ;  Enables INTTC2.
EI
LD      (TC2CR), 00100101B  ;  Starts TC2.
```

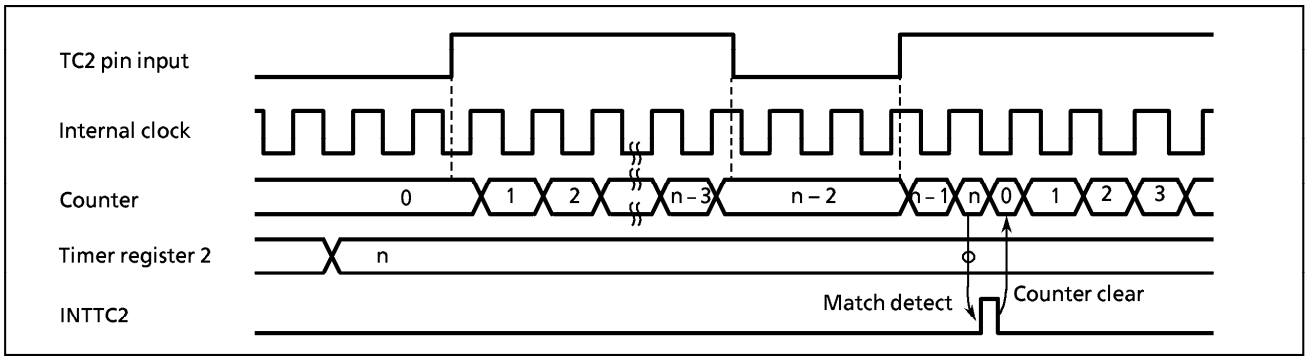


Figure 2-28. Window Mode Timing Chart

2.8 8-Bit Timer/Counter 3 (TC3)

2.8.1 Configuration

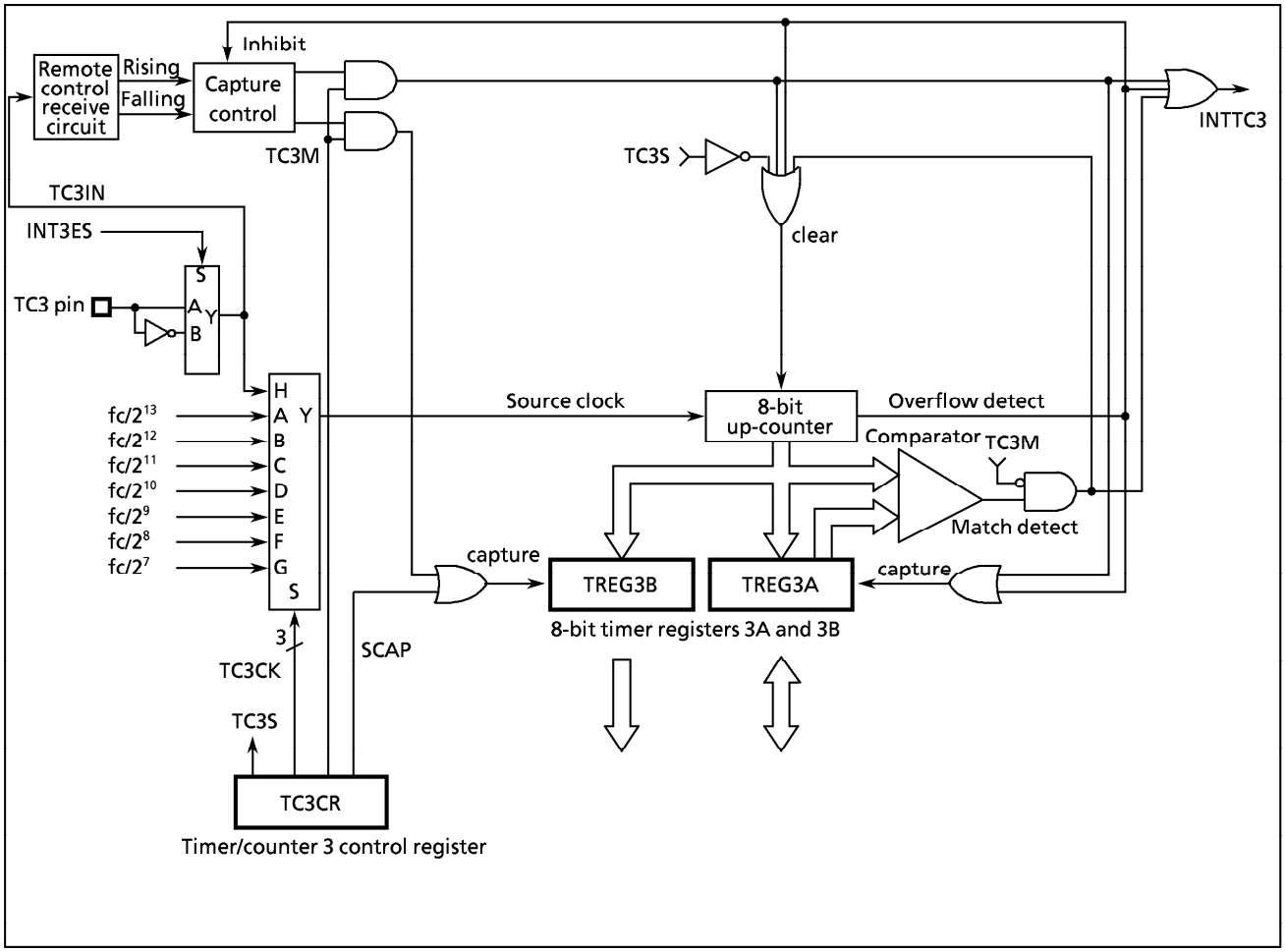


Figure 2-29. Timer/Counter 3 (TC3)

2.8.2 Control

Timer/counter 3 is controlled by timer/counter 3 control register (TC3CR) and tow 8-bit timer registers (TREG3A and TREG3B).

Timer register 3

	7	6	5	4	3	2	1	0	
TREG3A (00018_H)									Read/write
TREG3B (00019_H)									Read only

Timer/counter 3 control register

	7	6	5	4	3	2	1	0	
TC3CR ($0001A_H$)		SCAP		TC3S	TC3CK			TC3M	(Initial value : *0*0 0000)

TC3M	Selects timer/counter 3 operating mode.	0 : Timer/event counter mode 1 : Capture mode	Write only
TC3CK	Selects timer/counter 3 source clock.	000 : fc/2^{13} [Hz] 001 : fc/2^{12} 010 : fc/2^{11} 011 : fc/2^{10} 100 : fc/2^{9} 101 : fc/2^{8} 110 : fc/2^{7} 111 : External clock (TC3 pin input)	
TC3S	Controls timer/counter 3 start.	0 : Stops and clears TC3. 1 : Starts TC3.	
SCAP	Controls software capture.	0 : – 1 : Software capture	

*Note 1 : fc : High-frequency clock [Hz] * : Don't care*

Note 2 : Set mode, source clock, and edge (INT3ES) with a stop (TC3S = 0) state.

Note 3 : The values set in timer register 3A must satisfy the following conditions.
TREG3A > 0 (in timer or event counter mode)

Mote 4 : Software capture is only supported in timer or event counter mode.

Note 5 : TC3CR is write-only. Do not access it using read-modify-write instructions such as bit manipulation.

Figure 2-30. Timer/Counter 3 Timer Registers and Control Register

2.8.3 Functions

Timer/counter 3 supports three operating modes: timer, event counter, and window. In capture mode, noise rejection time can be set for input to TC3 input using the remote receive control register.

(1) **Timer mode**

TC3 counts up using the internal clock. A match between the counter value and the value set in timer register 3A (TREG3A) generates INTTC3 and clears the counter. Setting SCAP (bit 6 in TC3CR) to 1 loads the data in the up-counter to timer register 3B (TREG3B). SCAP is automatically zero-cleared.

Table 2-6. Internal Clock Sources for Timer/Counter 3
(Example: when fc = 16 MHz)

TC3CK	In NORMAL or IDLE mode	
	Resolution [μs]	Maximum set time [ms]
000	512	131.1
001	256	65.3
010	128	32.6
011	64	16.3
100	32	8.2
101	16	4.1
110	8	2.0

(2) **Event counter mode**

TC3 starts counting at the input edge of the TC3 pin (rising or falling edge selection also selects the INT3 pin edge). A match between the counter value and the value set in TREG3A generates INTTC3 and clears the counter.

The applicable maximum frequency is as shown in Table 2-7. For both high and low levels, the pulse width must be 2 machine cycles or more.

Setting SCAP to 1 loads the data in the up-counter to TREG3B (software capture). After software capture, SCAP is automatically zero-cleared.

Example : Input a pulse of 50 Hz to the TC3 pin and generate an interrupt every 0.5 s.

```
LD      (TREG3A), 19H          ;  0.5 s ÷ 1/50 = 25 = 19H
LD      (TC3CR), 00011110B     ;  Starts TC3.
```

Table 2-7. Timer/Counter 3 External Clock Source

applicable maximum frequency [Hz]
In NORMAL or IDLE mode
$fc/2^4$

(3) **Capture mode**

Capture mode is used to measure pulse width, cycle, and duty of input to the TC3 pin. It is used for decoding remote control signals and identifying 50/60 Hz AC. the counter free-runs using the internal clock. The counter value is loaded to TREG3A at the rising (falling) edge of input to the TC3 pin (rising of falling edge selection also selects the INT3 pin edge), the counter is cleared, then an interrupt is generated. The counter value is also loaded to TREG3B at the falling (rising) edge of input to the TC3 pin. In this case, the counter continues counting, the counter value is loaded to TREG3A, the counter is cleared, and an interrupt is generated. If the counter overflows before edge detection, FF_H is set in TREG3A and INTTC3 is generated simultaneously. Reading TREG3A with the interrupt processing determines overflow or no overflow. After the interrupt is generated (capture to TREG3A or overflow detect), capture or overflow detect is disabled until TREG3A is read. The counter continues counting. Reading TREG3A resumes capture or overflow detect ; TREG3B is usually read first.

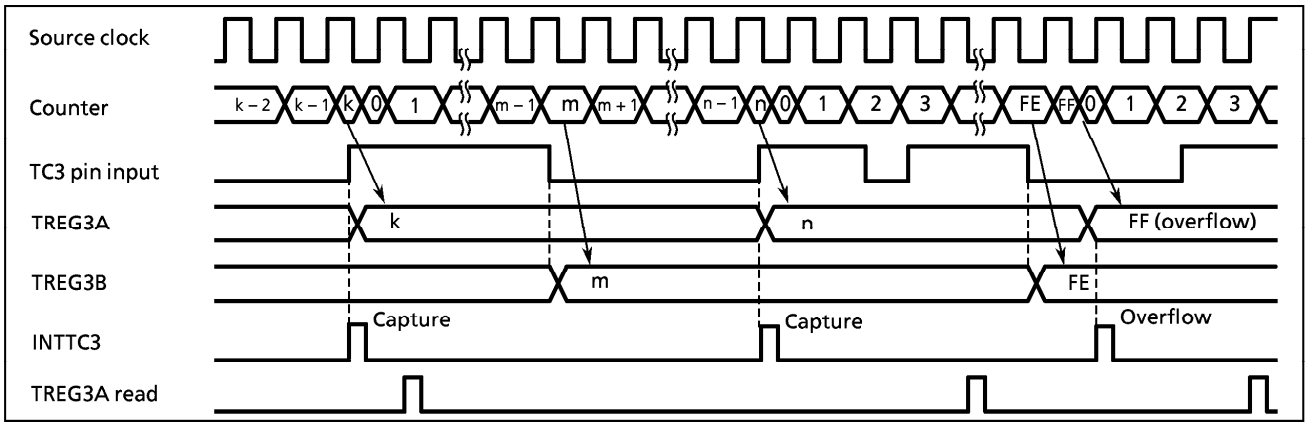


Figure 2-31. Capture Mode Timing Chart (INT3ES = 0)

The edge of input to the TC3 pin is detected using the remote control receive circuit shared by the noise rejection circuit. The remote control receive circuit is controlled by the remote control register (RCCR). The remote control status register (RCSR) is also used as the remote control register; it monitors polarity selection and noise rejection circuit status.

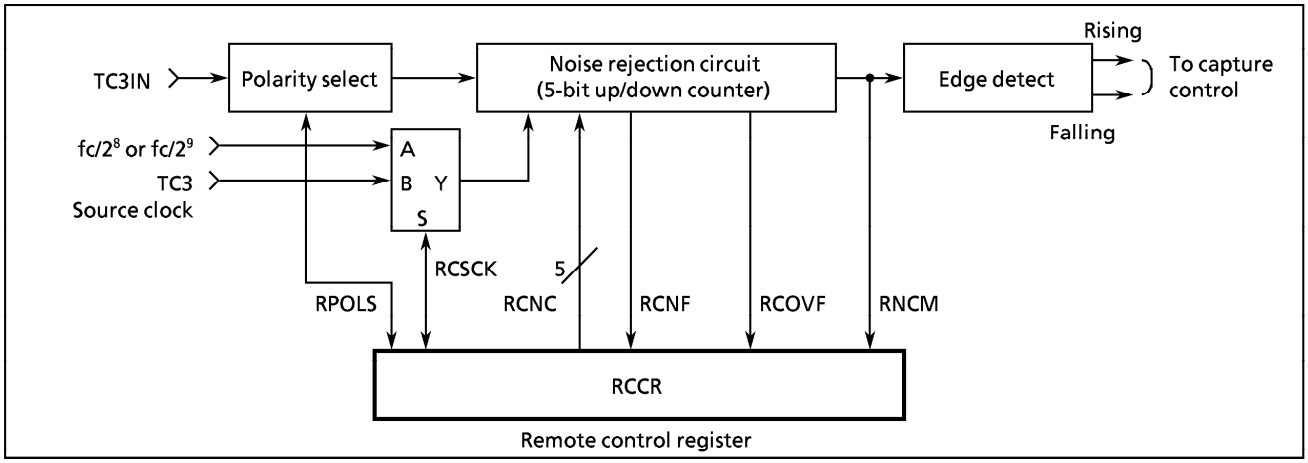


Figure 2-32. Remote Control Receive Circuit

Remote control register

RCCR ($0001F_H$)

| | | RPOLS | RCSCK | | | RCNC | | |

)Initial value : *001 1111(

RPOLS	Selects remote control signal polarity	0 : Positive polarity 1 : Negative polarity	R/W
RCSCK	Selects noise rejection circuit source clock.	0 : 2^8/fc 1 : TC3CK	
RCNC	Selects noise rejection time. $02_H \leqq RCNC \leqq 1F_H$	(source clock) × (RCNC−1) [s]	Write only

Note 1 : Set RPOLS and RCSCK with the timer counter stopped (TC3S = 0).
Note 2 : Timer/counter 3 source clock
*Note 3 : fc : High-frequency clock [Hz] * : Don't care*
Note 4 : Since RCCR includes a write-only bit, do not access RCCR using read-modify-write instructions such as bit manipulation.

Remote control status register

RCSR ($0001F_H$)

RCNF	RPOLS	RCSCK	RCOVF	RNCM			

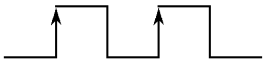
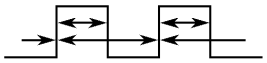
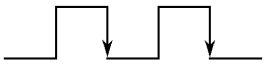
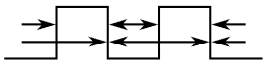
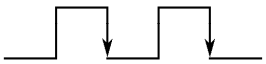
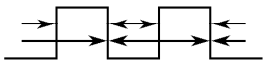
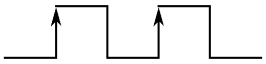
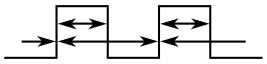
(Initial value : 0000 0***)

RCNF	Noise/no-noise monitor flag	0 : No noise 1 : Noise		Read only
RPOLS	Selects remote control signal polarity.	0 : Positive polarity 1 : Negative polarity		R/W
RCSCK	Selects noise rejection circuit source clock.	0 : 2^8/fc 1 : TC3CK		
RCOVF	Noise rejection circuit overflow flag	0 : Determines as signal, because noise rejection time RCNC is overwritten. 1 : Other than above		Read only
RNCM	Monitors remote control signal after passing through noise rejection circuit.		INT3ES = 0	INT3ES = 1
		0	0	1
		1	1	0

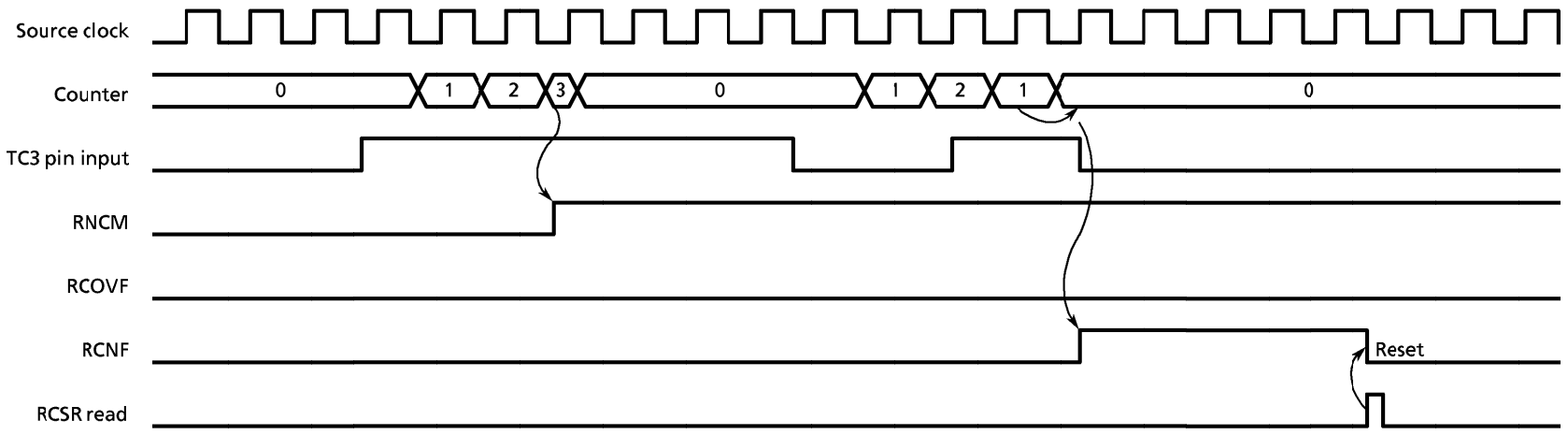
Note 1 : Reading RCSR resets RCNF and RCOVF.
Note 2 : Timer/counter 3 source clock
Note 3 : RCNF determines as noise when the 5-bit up/down counter counts up, counts down, then reaches 0.
*Note 4 : fc : High-frequency clock [Hz] * : Don't care*

Figure 2-33. Remote Control Register and Remote Control Status Register

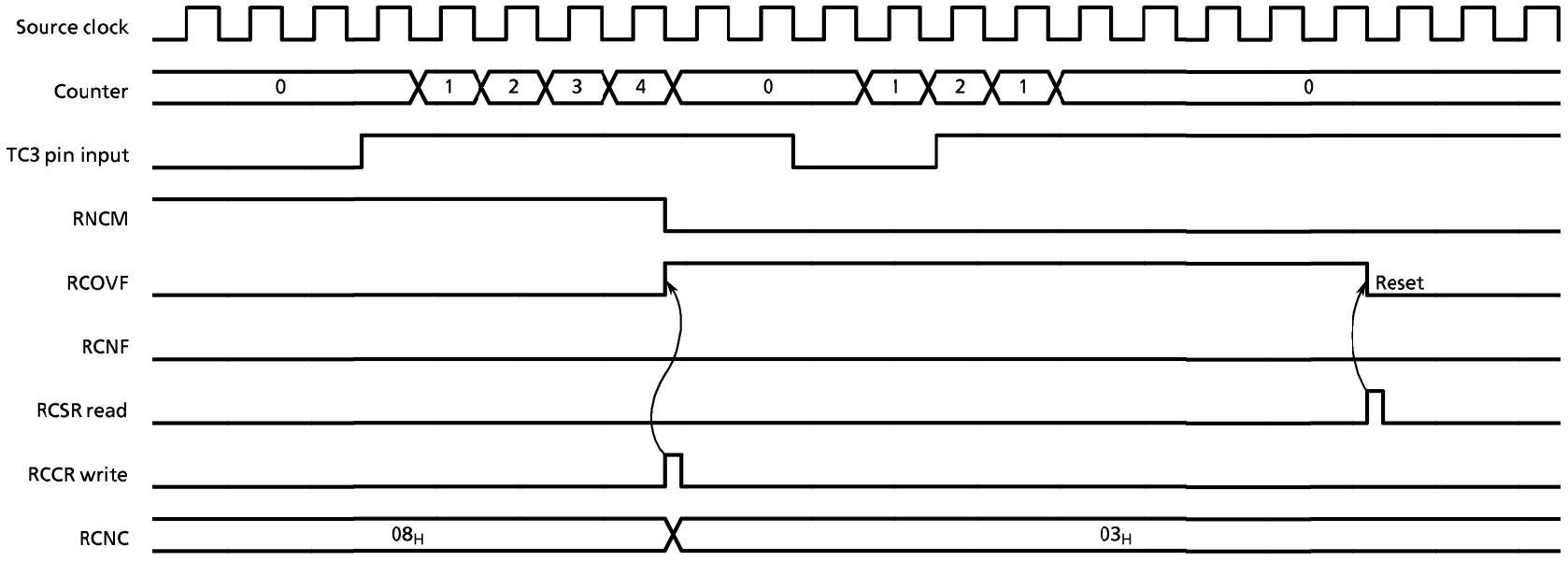
Table 2-8. Correspondence Between Polarity and Edge

RPOLS	INT3ES	TC3 pin input waveform (arrow: interrupt generation)	Measurement
0	0		
	1		
1	0		
	1		

Note 1 : When TC3CK is selected in RCSCK, select any source clock except external clock in TC3CK.
Note 2 : Starting remote control receive first detections an edge where an interrupt is generated.



(a) Example with noise (INT3ES = 0, RPOLS = 0, RCNC = 03_H)



(b) Example of noise rejection circuit overflow flag (INT3ES = 0, RPOLS = 1, RCNC = $08_H \rightarrow 03_H$)

Figure 2-34. Operation Timings of Remote Control Receive Circuit

2.9 8-Bit Timer/Counter 4 (TC4)

2.9.1 Configuration

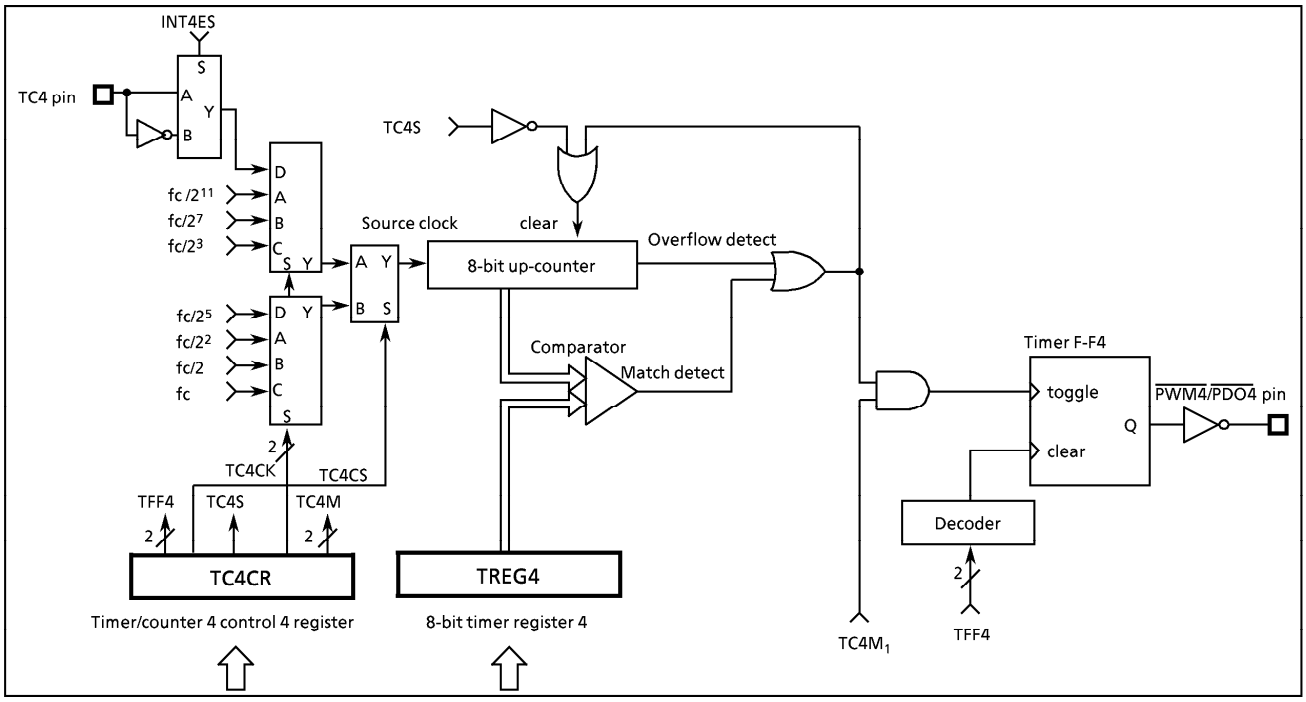


Figure 2-35. Timer/Counter 4 (TC4)

2.9.2 Control

Timer/counter 4 is controlled by timer/counter 4 control register (TC4CR) and timer register 4 (TREG4).

Timer register 4

TREG4 ($0001B_H$)

7	6	5	4	3	2	1	0

Write only

Timer/counter 4 control register

TC4CR ($0001C_H$)

7	6	5	4	3	2	1	0
TFF4		TC4CS	TC4S	TC4CK		TC4M	

(Initial value : 0000 0000)

TC4M	Selects timer/counter 4 operating mode.	0* : reserved 10 : Programmable divider output (PDO) mode 11 : Pulse width modulation (PWM) output mode		Write only
TC4CK	Selects timer/counter 4 source clock.	A mode (TC4CS = 0) 00 : $fc/2^{11}$ 01 : $fc/2^{7}$ 10 : $fc/2^{3}$ 11 : reserved	B mode (TC4CS = 1) 00 : $fc/2^{5}$ 01 : $fc/2^{2}$ 10 : fc/2 11 : fc	
TC4S	Controls start of timer/counter 4.	0 : Stops and clears TC4. 1 : Starts TC4.		
TC4CS	Selects timer/counter 4 source clock mode.	0 : A mode 1 : B mode		
TFF4	Controls timer F-F4.	00 : Clears timer F-F4. 11 : Reserved		

*Note 1 : fc : High-frequency clock [Hz] * : Don't care*

Note 2 : Set mode, source clock, edge (INT4ES), and timer F-F4 control using stop (TC4S = 0) state.

Note 3 : In B mode, set TFF4 to 11.

Note 4 : The value set in the timer register must satisfy the following conditions.

(a) In PWM output mode : $5 < TREG4 < 251$

(b) In other than PWM output mode : $0 < TREG4$

Note 5 : Source clock $fc/2^2$, fc/2 or fc cannot be used in other than PWM output mode.

Note 6 : TC4CR is write-only. Do not attempt access using read-modify-write instructions such as bit manipulation.

Figure 2-36. Timer/Counter 4 Timer Registers and Control Register

2.9.3 Functions

Timer/counter 4 supports two operating modes: programmable divider output and pulse width modulation output.

(1) **Programmable divider output (PDO) mode**

TC4 counts up using the internal clock. A match between the counter value and the value set in TREG4 inverts the timer F-F4 output and clears TC4. The inverted timer F-F4 output is output to the P52 ($\overline{PDO4}$) pin. For programmable divider output, set P52 output latches to 1. PDO mode can be used for approx. 50 % duty pulse output. Timer F-F4 can be initialized by program. At reset, timer F-F4 is initialized to 0.

```
Example :  Output 1024 Hz pulse (fc = 8 MHz)
           SET     (P5). 2              ;  Sets P52 output latch to 1.
           LD      (TREG4), 1EH         ;  1/2048 ÷ 2^7/fc = 1E_H
           LD      (TC4CR), 00010110B   ;  Starts TC4.
```

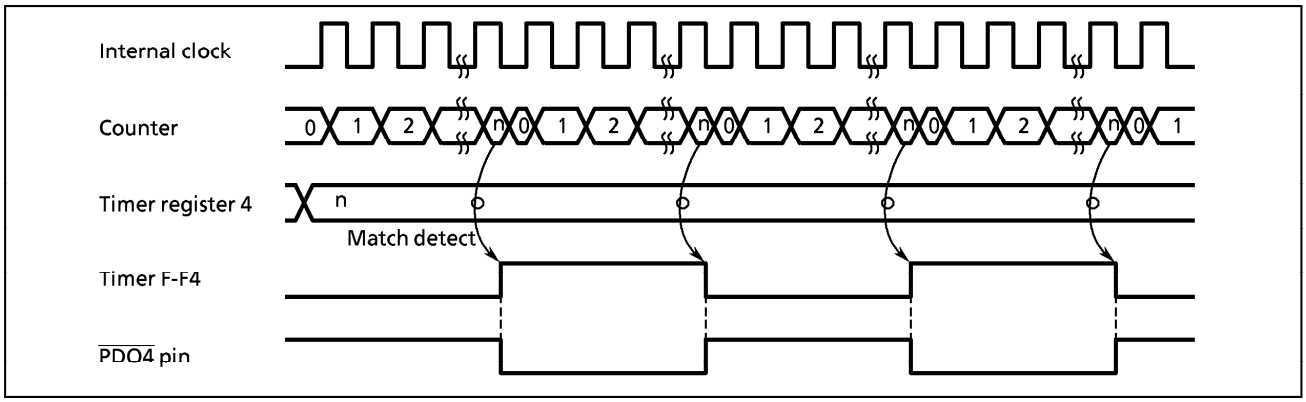


Figure 2-37. PDO Mode Timing Chart

(2) **Pulse width modulation (PWM) output mode**

Resolution of 8-bit PWM output can be performed. TC4 counts up using the internal clock. A match between the counter value and the value set in TREG4 inverts timer F-F4 output. TC4 continues counting up; an overflow inverts timer F-F4 output again, and clears TC4. The inverted timer F-F4 output is output to the P52 ($\overline{PWM4}$) pin. For PWM output, set the P52 output latch to 1.

TREG4 is a shift register (2 steps). Overwriting TREG4 during PWM output does not change output until output for one cycle is completed; thus, output can be changed continuously. First data are set in TREG4, then shifted at the start by TC4CR.

If data are overwritten during the cycle, the latest value is valid.

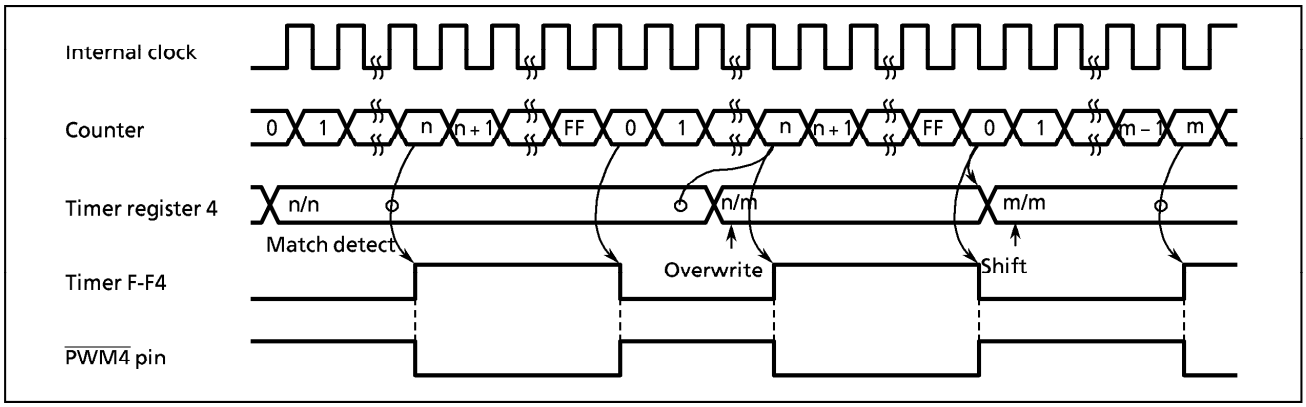


Figure 2-38. PWM Output Mode Timing Chart

Table 2-9. PWM Output Mode

Source clock		Resolution	Repeat cycle
Mode	NORMAL or IDLE	When fc = 16 MHz	
A	$fc/2^{11}$ [Hz]	128 μs	32.8 ms
	$fc/2^{7}$	8 μs	2 ms
	$fc/2^{3}$	0.5 μs	128 μs
B	$fc/2^{5}$ [Hz]	2 μs	512 μs
	$fc/2^{2}$	250 ns	64 μs
	fc/2	125 ns	32 μs
	fc	62.5 ns	16 μs

2.11 8-Bit Timer/Counter 6 (TC6)

2.11.1 Configuration

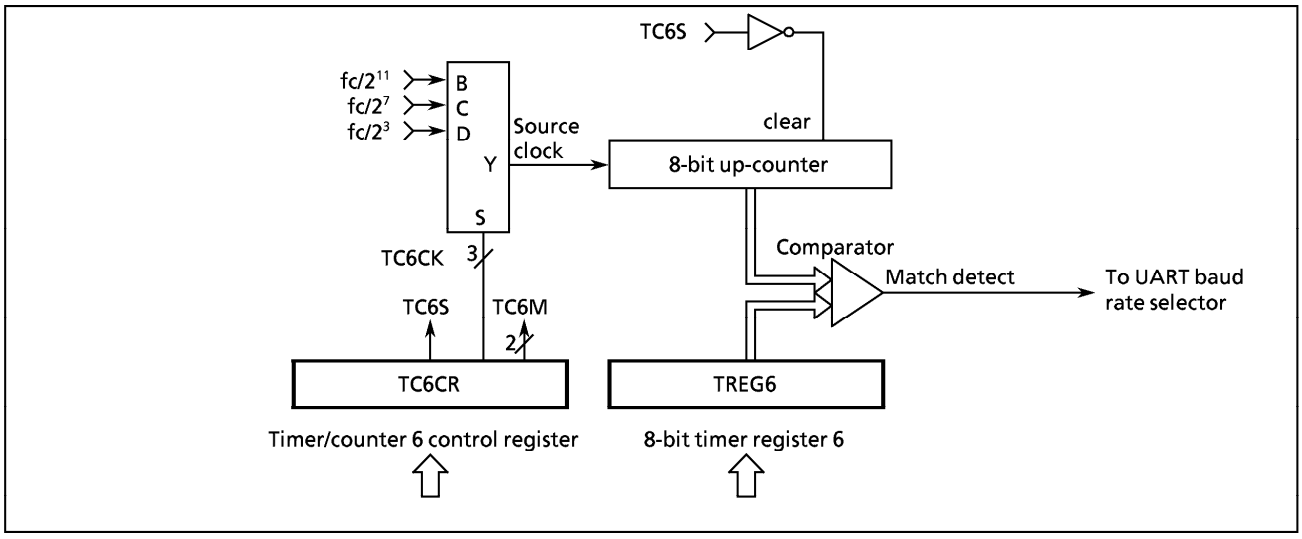


Figure 2-43. Timer/Counter 6 (TC6)

2.11.2 Control

Timer/counter 6 is controlled by timer/counter 6 control register (TC6CR) and timer register 6 (TREG6).

Timer register 6

TREG6 ($00FFE_H$)

7	6	5	4	3	2	1	0

write only

Timer/counter 6 control register

TC6CR ($00FFF_H$)

7	6	5	4	3	2	1	0
		TC6S	TC6CK				

(Initial value : **00 00**)

TC6CK	Selects timer/counter 6 source clock. unit : Hz	000 : Reserved 001 : $fc/2^{11}$ 010 : $fc/2^{7}$ 011 : $fc/2^{3}$ 1** : Reserved	write only
TC6S	Controls timer/counter 6 start.	0 : Stops and clears TC6. 1 : Starts TC6.	

*Note 1 : fc : High-frequency clock[Hz] * : Don't care*

Note 2 : The values set in the timer register must satisfy the following condition. TREG>6

Note 3 : Set operating mode or source clock using stop (TC6S = 0) state.

Figure 2-44. Timer/Counter 6 Timer Register and Control Register

2.11.3 Functions

TMP88CK49/M49 timer/counter 6 can only be used as the UART baud rate generator.

(1) UART baud generator mode

TC6 counts up using the internal clock. A match between the counter value and the value set in timer register 6 can be used as the UART transfer clock.

When using UART baud rate generator mode, set BRG in the UART control register (UARTCR) to 110.

The UART transfer clock and transfer rate are determined as follows:

$$\text{Transfer clock} = \frac{\text{TC6 source clock}}{\text{value set in TREG6}}$$

$$\text{Transfer rate} = \frac{\text{Transfer clock}}{16}$$

2.13 UART (asynchronous serial interface)

TMP88CK49/M49 features a built-in channel for UART (asynchronous serial interface). UART is connected to external devices via RxD and TxD. RxD is also used as P43; TxD, as P44. To use P43 or P44 as the RxD or TxD pin, set P4 port output latches to 1.

2.13.1 Configuration

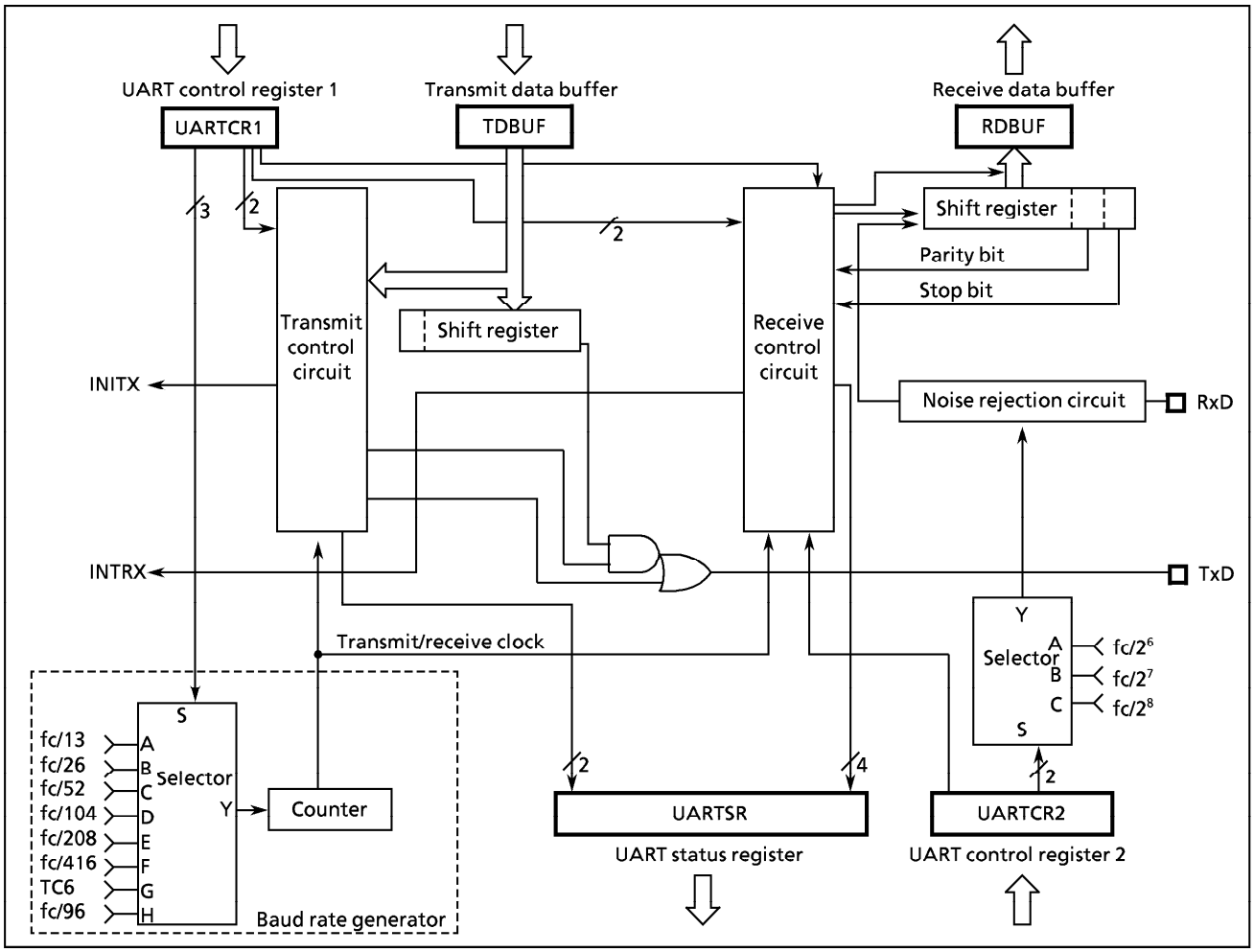


Figure 2-50. UART (asynchronous serial interface)

2.13.2 Control

UART is controlled by the UART control register (UARTCR). The operating status can be monitored using the UART status register (UARTSR).

UART control register

UARTCR ($00FFC_H$)

7	6	5	4	3	2	1	0
TXE	RXE	STBT	EVEN	PE	BRG		

(Initial value : 0000 0000)

BRG	Selects transfer clock.	000 : fc/13 [Hz] 001 : fc/26 010 : fc/52 011 : fc/104 100 : fc/208 101 : fc/416 110 : TC6 111 : fc/96	write only
PE	Parity addition	0 : No parity 1 : Parity	
EVEN	Even-numbered parity	0 : Odd-numbered parity 1 : Even-numbered parity	
STBT	Transmit stop bit length	0 : 1 bit 1 : 2 bit	
RXE	Data receive	0 : Disable 1 : Enable	
TXE	Data transmit	0 : Disable 1 : Enable	

Note 1 : When operation is disabled by setting the TXE or RXE bit to 0, the setting becomes valid when data transmit or receive is complete. If the transmit data are stored in the transmit data buffer, the data are not transmitted. Even if data transmit is enabled, until new data are written to the transmit data buffer, the current data are not transmitted.

Note 2 : The transfer clock and parity are common to transmit and receive.

UARTCR2 ($00FFD_H$)

7	6	5	4	3	2	1	0
					RXDNC		STOPBR

(Initial value : **** *000)

STOPBR	Receive stop bit length	0 : 1 bit 1 : 2 bits	write only
RXDNC	Selection of RXD input noise rejection time	00 : No noise rejection (hysteresis input) 01 : Rejects pulses shorter than 31/fc [s] as noise. 10 : Rejects pulses shorter than 63/fc [s] as noise. 11 : Rejects pulses shorter than 127/fc [s] as noise.	

Note 3 : When RXDNC = 01, pulses longer than 96/fc [s] are always regarded as signals; when RXDNC = 10, longer than 192/fc [s]; and when RXDNC = 11, longer than 384/fc [s].

UART Control Register

UART status register

UARTSR ($00FFC_H$)

7	6	5	4	3	2	1	0
PERR	FERR	OERR	RBFL	TEND	TBEP		

(Initial value : 0000 11**)

TBEP	Transmit data buffer empty flag	1 : Transmit data buffer empty	read only
TEND	Transmit end flag	0 : Transmitting 1 : Transmit end	
RBFL	Receive data buffer full flag	0 : – 1 : Receive data buffer full	
OERR	Overrun error flag	0 : No overrun error 1 : Overrun error	
FERR	Framing error	0 : No framing error 1 : Framing error	
PERR	Parity error flag	0 : No parity error 1 : Parity error	

UART receive data buffer

RDBUF ($00FFB_H$)

7	6	5	4	3	2	1	0

read only
(Initial value : 0000 0000)

UART transmit buffer

TDBUF ($00FFB_H$)

7	6	5	4	3	2	1	0

write only
(Initial value : 0000 0000)

Figure 2-51. UART Status Register and Data Buffer Registers

2.13.3 Transfer Data Format

With UART, a one-bit start bit (low level), stop bit (bit length selectable at high level, in STBT), and parity (select parity in PE; even- or odd-numbered parity in EVEN) are added to the data to be transferred. Shown below are the transfer data formats.

Table 2-16. Transfer Data Formats

PE	STBT	Frames 1 2 3 ------- 8 9 10 11 12
0	0	Start bit 0 bit 1 ----- bit 6 bit 7 Stop 1
0	1	Start bit 0 bit 1 ----- bit 6 bit 7 Stop 1 Stop 2
1	0	Start bit 0 bit 1 ----- bit 6 bit 7 Parity Stop 1
1	1	Start bit 0 bit 1 ----- bit 6 bit 7 Parity Stop 1 Stop 2

2.13.4 Transfer Rate

Set the UART transfer rate (baud rate) in BRG (bits 0, 1, and 2 in UARTCR). Listed below are the transfer rates.

Table 2-17. UART Transfer Rates (Examples)

BRG	Source clock		
	16 MHz	8 MHz	4 MHz
000	76800 [baud]	38400 [baud]	19200 [baud]
001	38400	19200	9600
010	19200	9600	4800
011	9600	4800	2400
100	4800	2400	1200
101	2400	1200	600

When TC6 is used as the UART transfer rate (when BRG = 110), the transfer clock and transfer rate are determined as follows:

$$\text{Transfer clock} = \frac{\text{TC6 source clock}}{\text{TREG6 set value}}$$

$$\text{Transfer rate} = \frac{\text{Transfer clock}}{16}$$

2.13.5 Data Sampling

The UART receiver keeps sampling input until a start bit is detected in the RxD pin input, using the clock selected by BRG (bits 0, 1, and 2 in UARTCR). RT clock detects the falling edge of the RxD pin and start. Once a start bit is detected, the start bit, data bits, stop bit (s), and parity bit are sampled three times at 7RT, 8RT, and 9RT during one receiver clock interval (RT1 clock). (RT0 is the position where the bit supposedly starts.) Bits are determined according to majority rule (the data are the same twice or more out of three samplings).

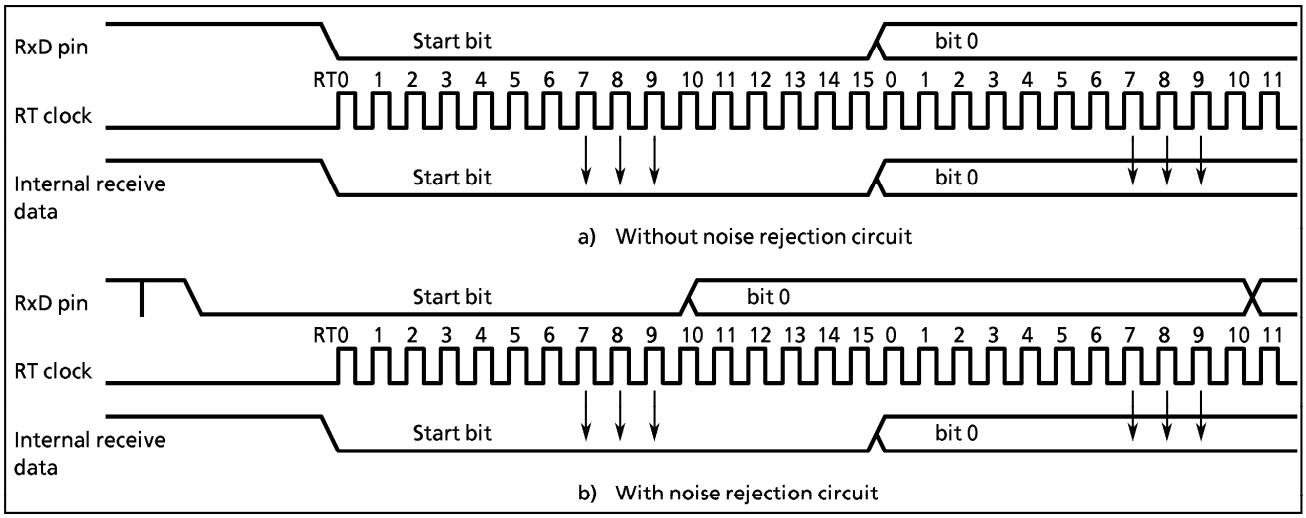


Figure 2-52. Data Sampling

2.13.6 Stop Bit Length

Select a transmit stop bit length (1 or 2 bits) in STBT (bit 5 in UARTCR).

2.13.7 Parity

Set parity/no parity in PE; set parity type (odd- or even-numberred) in EVEN (bit 4 in UARTCR).

2.13.8 Transmit/Receive

(1) **Data transmit**

Set TXE (bit 7 in UARTCR) to 1. Read UARTSR to check TBEP = 1, then write data in TDBUF (transmit data buffer). Writing data in TDBUF zero-clears TBEP, transfers the data to the transmit shift register and the data are sequentially output from the TxD pin. The data output include a one-bit start bit, stop bits whose number is specified in STBT (bit 5 in UARTCR), and a parity bit if parity addition is specified. Select the data transfer baud rate using bits 0 to 2 in UARTCR. When data transmit starts, transmit buffer empty flag TBEP is zero-cleared and interrupt INTTX is generated.

When transmitting data, first read UARTSR, then write data in TDBUF. Otherwise, TBEP is not zero-cleared and transmit does not start.

(2) **Data receive**

Set RXE (bit 6 in UARTCR) to 1. When data are received via the RxD pin, the receive data are transferred to RDBUF (receive data buffer). At this time, the data transmitted include a start bit and stop bit (s), and a parity bit if parity bit if parity addition is specified. When stop bit (s) are received, data only are extracted and transferred to RDBUF (receive data buffer). Then the receive buffer full flag RBFL is set and interrupt INTRX is generated. Select the data transfer baud rate using BRG (bits 0 to 2 in UARTCR).

If an overrun error (OERR) occurs when data are received, the data are not transferred to RDBUF (receive data buffer) but discarded; data in the RDBUF are not affected.

2.13.9 Status Flag

(1) **Parity error**

When parity determined using the receive data bits differs from the received parity bit, parity error flag PERR is set in UARTSR. Reading UARTSR the RDBUF clears PERR.

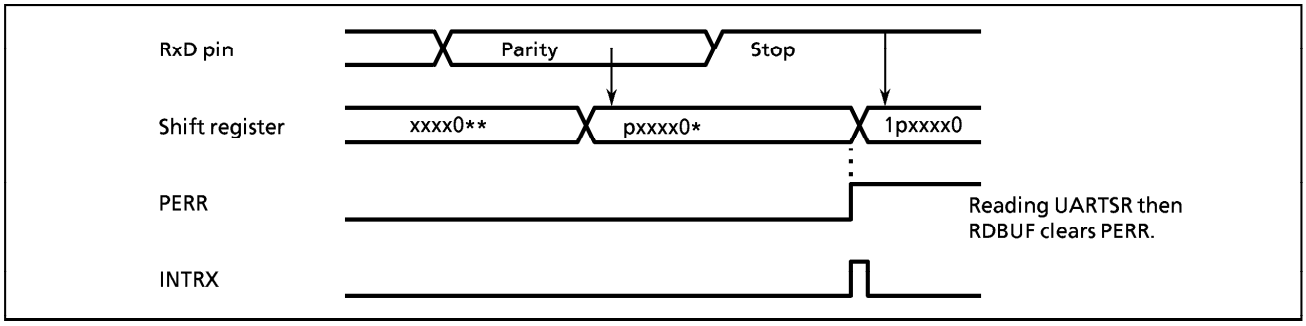


Figure 2-53. Generation of Parity Error

(2) **Framing error**

When 0 is sampled as the stop bit in the receive data, framing error flag FERR is set. Reading UARTSR then RDBUF clears FERR.

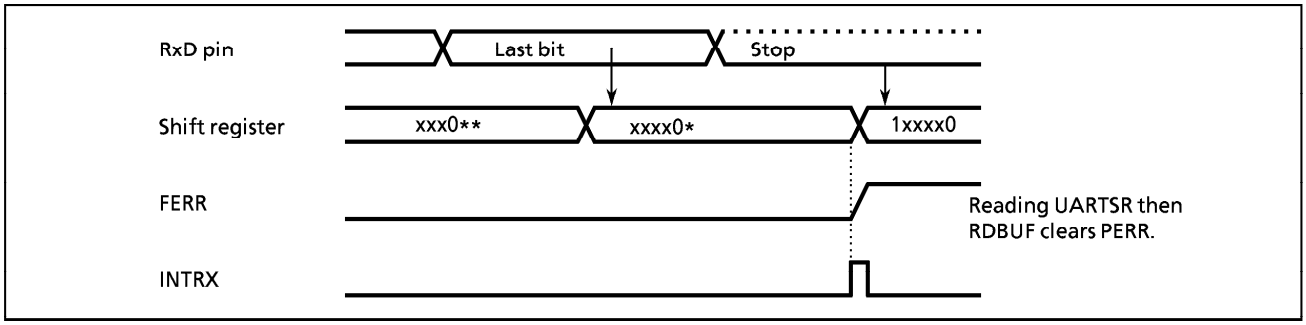


Figure 2-54. Generation of Framing Error

(3) **Overrun error**

When all bits in the next data are received while unread data are still in RDBUF, overrun error flag OERR is set. The receive data are discarded; data in RDBUF are not affected. Reading UARTSR then RDBUF clears OERR.

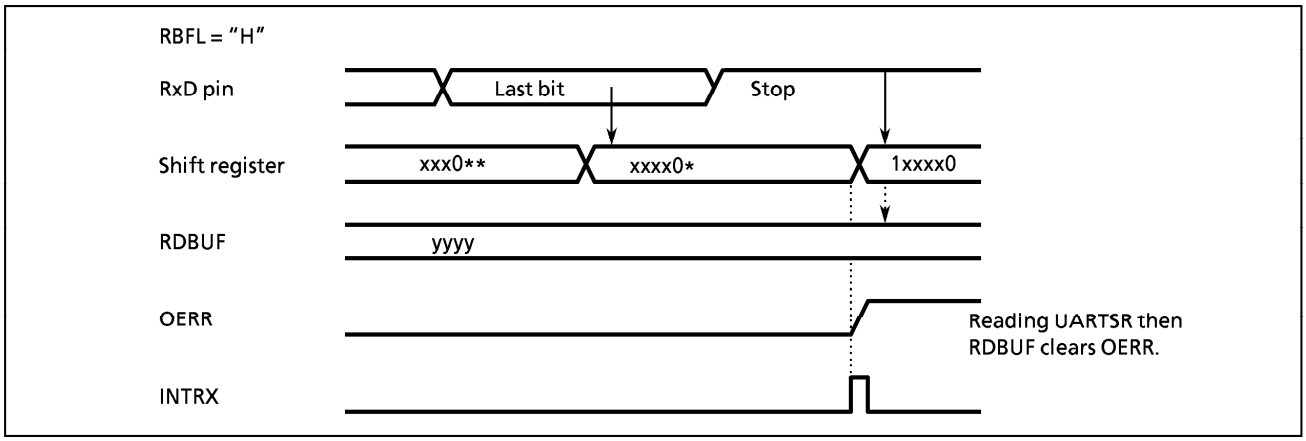


Figure 2-55. Generation of Overrun Error

(4) **Receive data buffer full**

Loading the receive data in RDBUF sets receive data buffer full flag RBFL. Reading UARTSR then RDBUF clears RBFL.

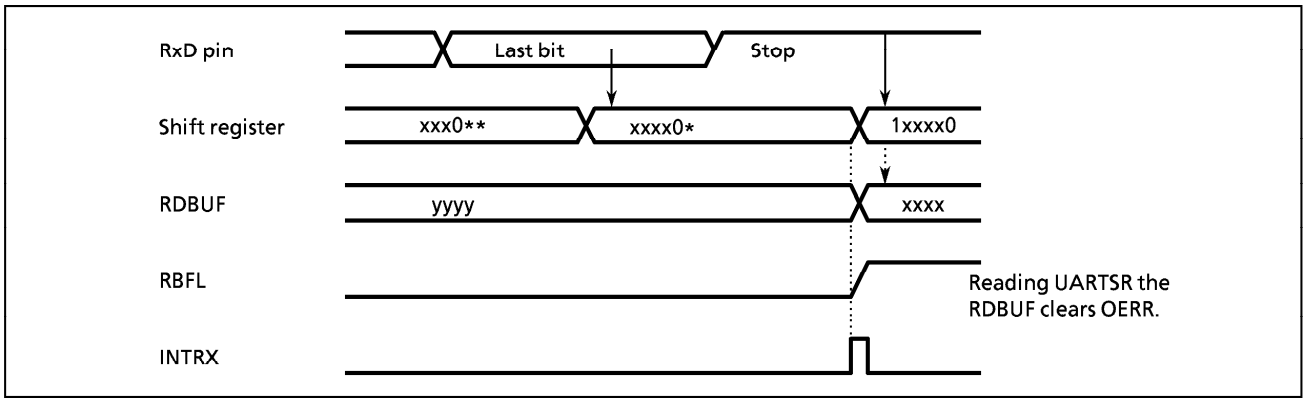


Figure 2-56. Generation of Receive Buffer Full

(5) **Transmit data buffer empty**

When there are no data in transmit data buffer TDBUF, that is, when data in TDBUF are transferred to the transmit shift register and data transmit starts, transmit data buffer empty flag TBEP is set. Reading UARTSR then writing the data to TDBUF clears TBEP.

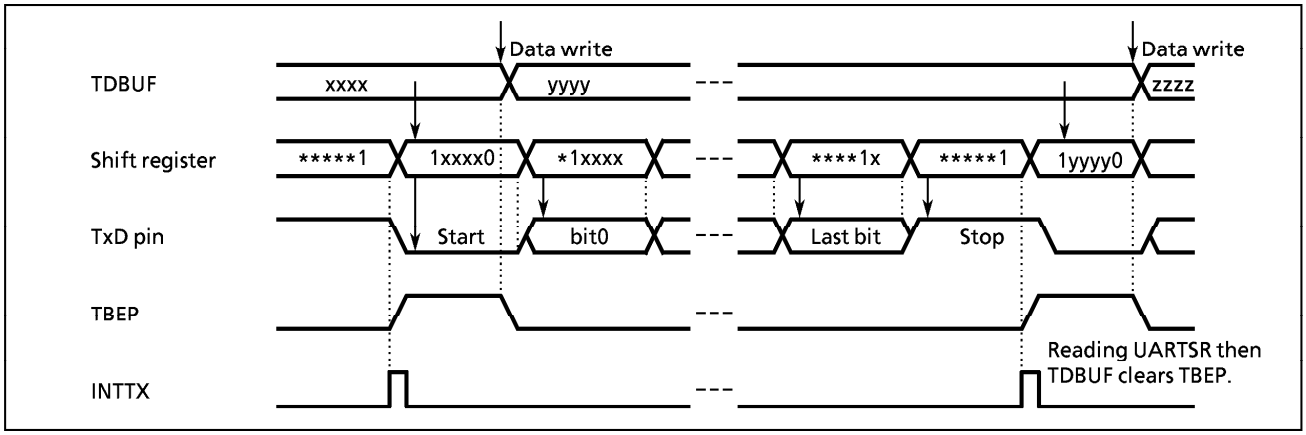


Figure 2-57. Generation of Transmit Buffer Empty

(6) **Transmit end flag**

When data are transmitted and there are no data in TDBUF (TBEP = 1), transmit end flag TEND is set. Writing data to TDBUF then starting data transmit clears TEND.

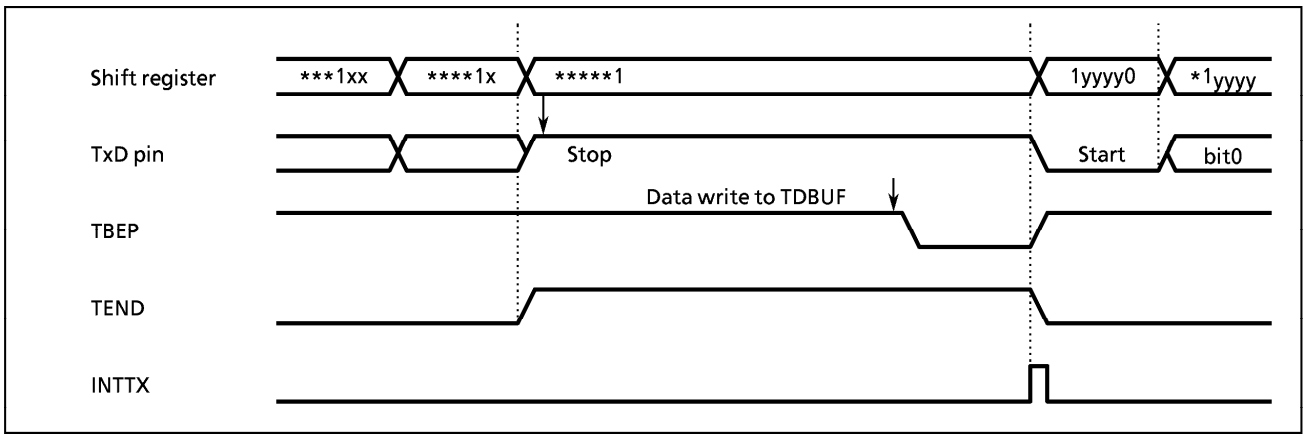


Figure 2-58. Generation of Transmit Buffer Empty

2.16 8-Bit High-Speed PWM ($\overline{\text{HPWM0}}$, $\overline{\text{HPWM1}}$)

TMP88CK49/M49 features two channels for high-speed PWM. High-speed PWM outputs different waveforms by writing data in the channel data register.

High-speed PWM uses P53 ($\overline{\text{HPWM0}}$) and P54 ($\overline{\text{HPWM1}}$). To use these pins for high-speed PWM, set the P53 and P54 output latches to 1.

2.16.1 Configuration

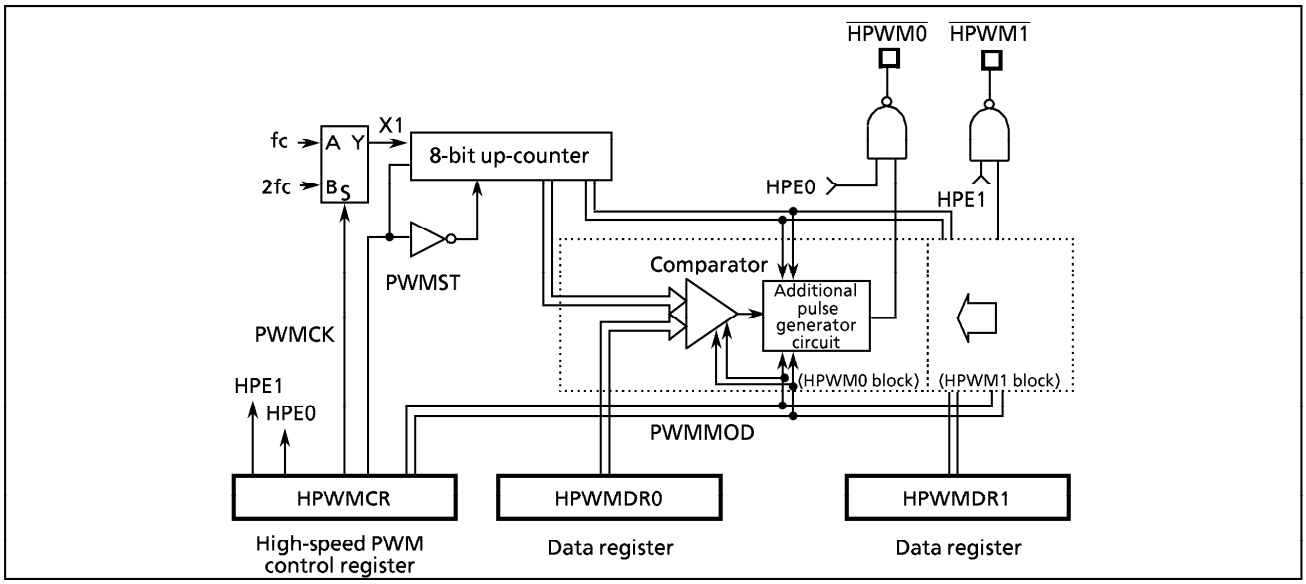


Figure 2-89. High-Speed PWM ($\overline{\text{HPWM0}}$ and $\overline{\text{HPWM1}}$)

2.16.2 Control

Control register

HPWMCR (00026_H)

7	6	5	4	3	2	1	0
HPE1	HPE0			PWMST	PWMCK	PWMMOD	

write only (Initial value : 00** 0000)

PWMMOD	Selects PWM mode.	00 : Mode 0 (8 bits) 01 : Mode 1 (7 bits) 10 : Mode 2 (6 bits) 11 : Unused	write only
PWMCK	Selects PWM source clock (X1)	0 : fc 1 : 2fc (only in mode 0)	
PWMST	8-bit up-counter run/stop	0 : STOP 1 : RUN	
HPE0	Controls HPWM0 output.	0 : Disable 1 : Enable	
HPE1	Controls HPWM1 output.	0 : Disable 1 : Enable	

Data registers

HPWMDR1 (00027_H)

7	6	5	4	3	2	1	0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

write only (Initial value : **** ****)

HPWMDR2 (00028_H)

7	6	5	4	3	2	1	0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

write only (Initial value : **** ****)

Figure 2-90. High-Speed PWM Control Register and Data Registers

2.16.3 Operation

High-speed PWM is controlled by the control register (HPWMCR) and data registers (HPWMR0, 1). To write to these registers, set HPWMCR<PWMST> = 1 to enable setting. Setting HPWMCR<PWMST> = 0 resets the control registers, resetting high-speed PWM by software.

(1) **Operating mode**

High-speed PWM supports following three operating modes:

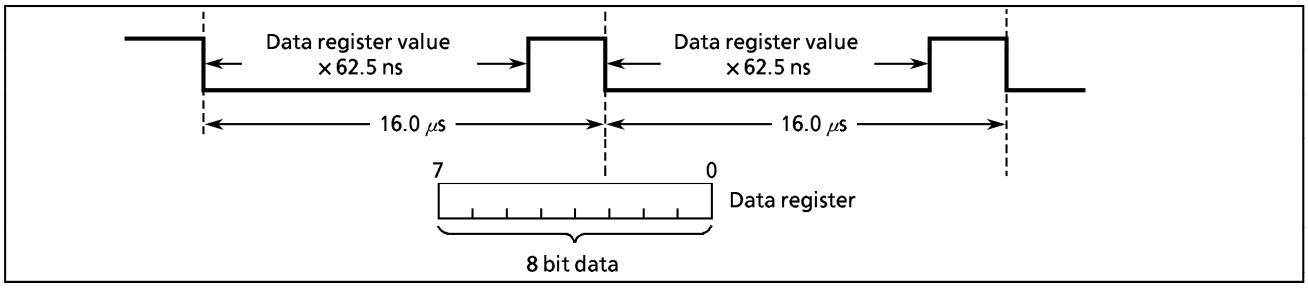
* 8-bit mode : (T = 28 × clock cycle, f ≒32 kHz, f ≒*64 kHz)
* 7-bit mode : (T = 27 × clock cycle, f ≒64 kHz)
* 6-bit mode : (T = 26 × clock cycle, f ≒128 kHz)

*Note : A numeral following * indicates when the source clock (X1) operates at 16 MHz (2fc = 8 MHz)*

Set the operating mode using HPWMCR<PWMMOD>. The operating mode is common to the channels: two operating modes cannot be set simultaneously.

① 8-bit mode

In 8-bit mode, pulses with 16.05 s cycle and approx. 64 kHz frequency (X1 = 16 MHz).



The minimum pulse width is 62.5 ns (data: 1); the maximum pulse width is 15.05 s (data: F0).

Pulse width = 8-bit data × 62.5 ns

Figure 2.91 shows examples of waveforms. (Numerals are when X1 = 16 MHz)

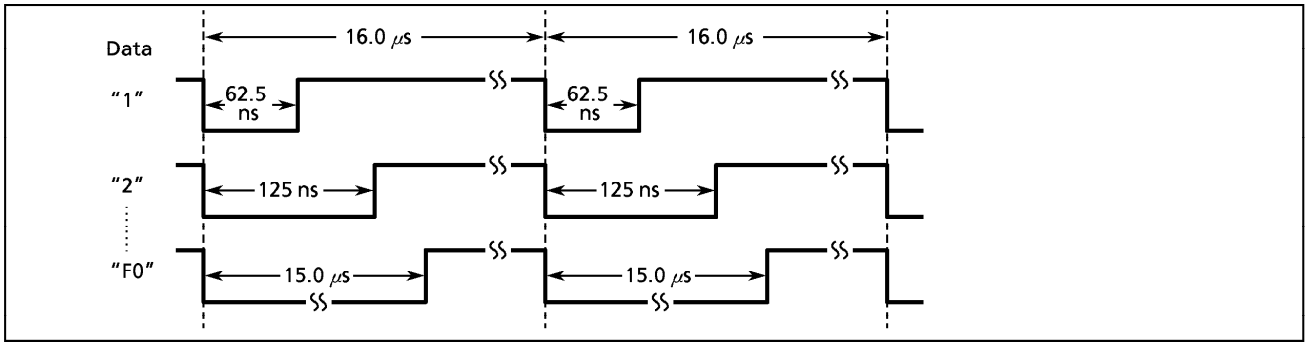
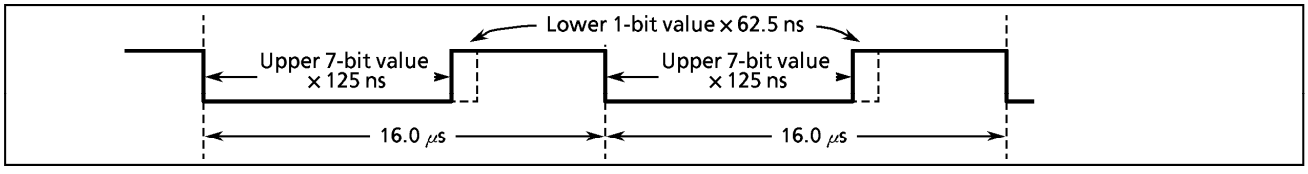


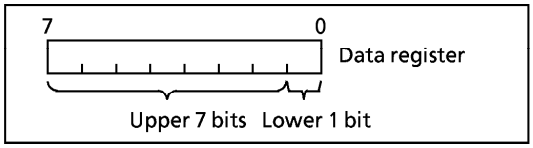
Figure 2-91. 8-Bit Mode

② 7-bit mode

In 7-bit mode, pulses with 16.05 s cycle and frequency of 64 kHz (X1 = 16 MHz) are output.



In 7-bit mode, 7 bits are used for the cycle (cycle = 27 × 125 ns) and the remaining bit is used for 62.5 ns resolution (half of source clock (X1) cycle). Thus, when the lower 1 bit = 1, + 62.5 ns pulse is output. The minimum pulse width is 62.5 ns (data: 1); the maximum pulse width is 15.06255 s (data: F1).



Pulse width = (upper 7-bit data × 125 ns) + (lower 1-bit data × 62.5 ns)
Figure 2.69 is an example of the waveform. (Numerals are when X1 = 8 MHz.)

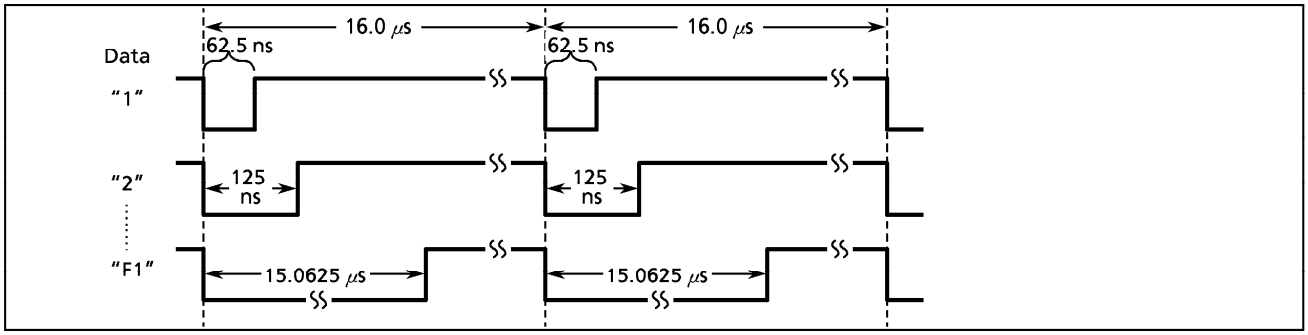
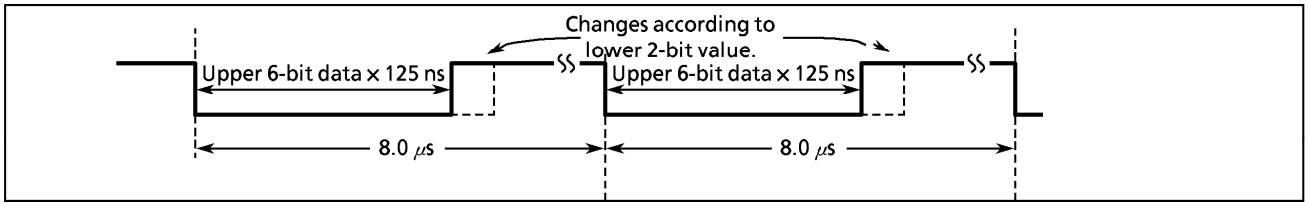
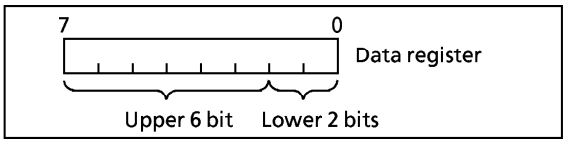


Figure 2-92. 7-bit mode

③ 6-bit mode
In 6-bit mode, pulses with 8.05 s cycle and frequency of 128 kHz (X1 = 8 MHz) are output.



In 6-bit mode, 6 bits (cycle = 26 × 125 ns) are used for the cycle and the remaining 2 bits are used for 31.25 ns resolution. However, the actual resolution is 62.5 ns, so the resolution of 31.25 ns is implemented in a pseudo way. To obtain a resolution of 31.25 ns, pulses are output with an additional 62.5 ns the first time; 0 ns the second time; and with additional 62.5 ns the third time. The minimum equivalent pulse width is 31.25 ns (data: 1); the maximum equivalent pulse width is 7.6255 s (data: F3).



Pulse width = (upper 6-bit data × 125 ns) + (* lower 2-bit data)
* The equivalent plus time for lower 2-bit data is as listed below:

2-bit data	Equivalent pulse time
0 0	0 ns
0 1	31.25 ns
1 0	62.5 ns
1 1	93.75 ns

Figure 2-79 shows waveform. (Numerals are when X1 = 8 MHz).

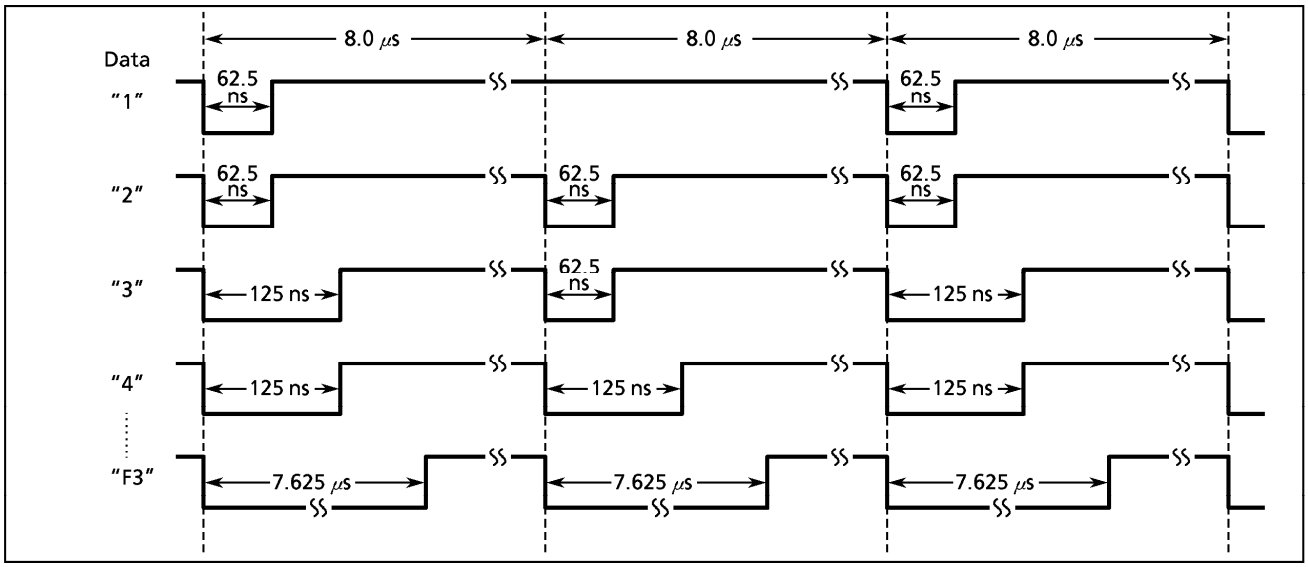
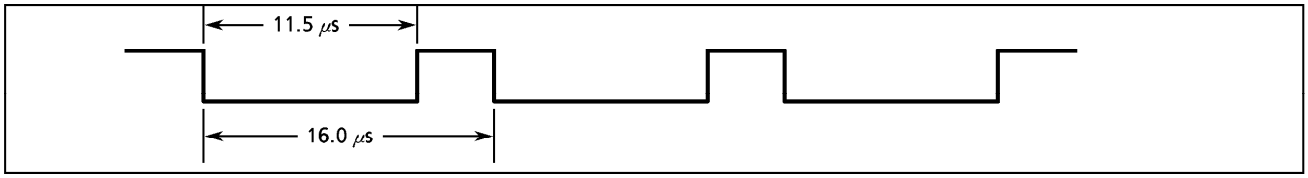


Figure 2-93. 6-Bit Mode

(2) **Output data setting**

Set output data by writing to the data register (HPWMDR0, 1).

Example : When source clock (X1) = 8 MHz, output 11.55 s waveform in 7-bit mode using $\overline{\text{HPWM0}}$.



Since resolution in 7-bit mode is 62.5 ns, to output a 11.5 ns pulse, set the

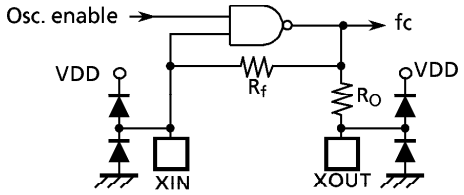
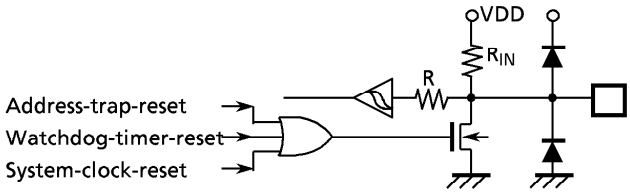
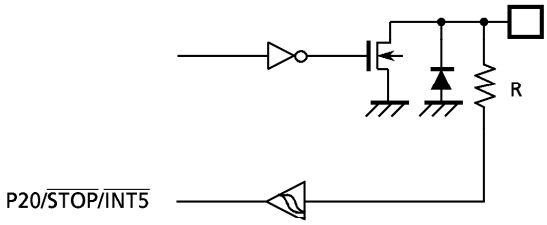
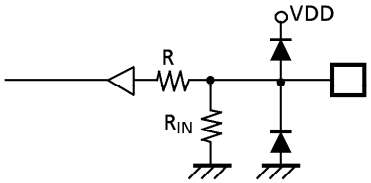
11.5μs ÷ 62.5 ns = 184 = B8H

following in data register HPWMDR0.

Pin I/O Circuit

(1) Control pins

The I/O circuits for the TMP88CK49/M49 control pins are as shown below:

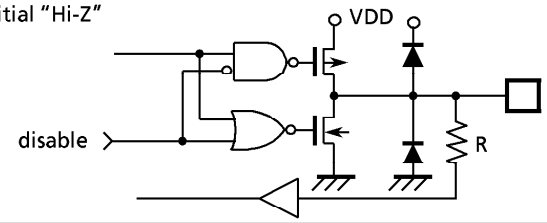
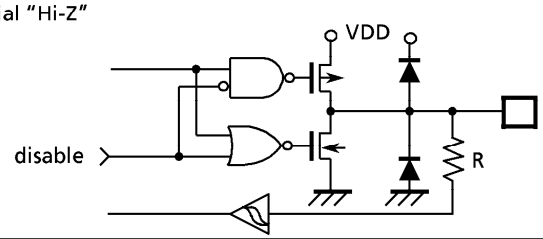
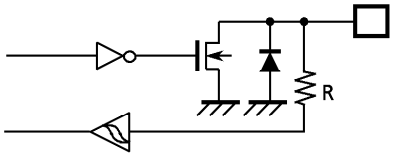
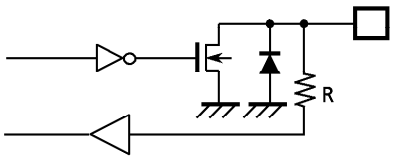
Control pin	I/O	Circuit	Notes
XIN XOUT	Input Output		Resonator connecting Pins (high-frequency) R_f = 1.2 MΩ (typ.) R_O = 1.5 kΩ (typ.)
$\overline{\text{RESET}}$	I/O		Sind open-drain output Hysteresis input Built-in pull-down resistor R_{IN} = 220 kΩ (typ.) R = 1 kΩ (typ.)
$\overline{\text{STOP}}$/$\overline{\text{INT5}}$	Input		Hysteresis input R = 1 kΩ (typ.)
TEST	Input		Built-in pull-down resistor R_{IN} = 70 kΩ (typ.) R = 1 kΩ (typ.)

Note 1 : The TMP88PS49 TEST pin has no pull-down resistor. Must be fixed to low level.

Note 2 : Insert a protection diode between V_{SS} or V_{DD} as close to the package as possible.

(2) I/O ports

I/O circuits for TMP88CK49/M49 I/O ports are as shown below:

Port	I/O	I/O circuit	Notes
P0 P6 P7	I/O	initial "Hi-Z" 	Tri-state I/O R = 1 kΩ (typ.)
P1	I/O	initial "Hi-Z" 	Tri-state I/O Hysteresis input R = 1 kΩ (typ.)
P2 P4 P5	I/O	initial "Hi-Z" 	Sink open drain output R = 1 kΩ (typ.)
P3	I/O	initial "Hi-Z" 	Sink open drain output High current output R = 1 kΩ (typ.)

Note : Insert a protection diode between V_{SS} or V_{DD} as close to the package as possible.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	P21, P22, $\overline{RESET}$, Tri-state, Push-Pull Port	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	P20, Sink Open Drain Port	– 0.3 to 5.5	V
Output Current	I_{OUT1}	P1, P2, P4, P5, P6, P7 Port	3.2	mA
	I_{OUT2}	P0 Port	20	
	I_{OUT3}	P3 Port	30	
Output Current	ΣI_{OUT1}	P1, P2, P4, P5, P6, P7 Port	120	mA
	ΣI_{OUT2}	P0 Port	60	
	ΣI_{OUT3}	P3 Port	120	
Power Dissipation [Topr = 70 °C]	PD	TMP88CK49N/TMP88CM49N	600	mW
		TMP88CK49F/TMP88CM49F	350	
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 40 to 85	°C

RECOMMENDED OPEATING CONDITIONS (V_{SS} = 0 V, Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS		Min.	Max.	UNIT
Supply Voltage	V_{DD}		fc = 16.0 MHz	NORMAL mode	4.5	5.5	V
				IDLE mode			
				STOP mode			
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		8.0	16.0	MHz

Note : Clock frequency fc : The condition of supply voltage range is the value in NORMAL and IDLE modes.

D.C. CHARACTERISTICS (V_{SS} = 0 V, Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis inputs		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Sink Open Drain, Tri-state Port					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Low-Level Input Current	I_{IL}	Push-Pull Port	V_{DD} = 5.5 V, V_{IN} = 0.4 V	–	–	– 2	mA
Input Resistor (*)	R_{IN1}	P7 Port with pull-up		20	70	170	kΩ
	R_{IN2}	$\overline{RESET}$		90	220	510	
Output Leakage Current	I_{OL}	Sink Open Drain, Tri-state Port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V	–	–	± 2	μA
Output High Voltage	V_{OH1}	Push-Pull Port	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	–	–	V
	V_{OH2}	Tri-state Port	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	
Output Low Current	I_{OL1}	Except XOUT, and ports P0 and P3.	V_{DD} = 4.5 V, V_{OL} = 0.4 V	–	1.6	–	mA
	I_{OL2}	P0 Port	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	10	–	
	I_{OL3}	P3 Port		–	20	–	
Supply Current in NORMAL Mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V fc = 16.0 MHz	–	20	32	mA
Supply Current in IDLE Mode				–	10	16	mA
Supply Current in STOP Mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	–	0.5	20	μA

Note 1 : Typical values show those at Topr = 25 °C , V_{DD} = 5 V.
Note 2 : Input Current IIN1, IIN3; The current through pull-up or pull-down registor is not included.
Note 3 : IDD does not include IREF.

A/D CONVERSION CHARACTERISTICS (Topr = – 40 to 85 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.			UNIT
					ADCDR1	ADCDR2		
						ACK = 0	ACK = 1	
Analog Reference Supply Voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq 3.5$ V	V_{DD} – 1.0	—	V_{DD}			V
	V_{ASS}		V_{SS}	—	1.0			
Analog Input Voltage Range	V_{AIN}		V_{ASS}	—	V_{AREF}			V
Analog Reference Voltage Supply Current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	—	0.5	1.0			mA
Non-linearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V	—	—	± 1	± 3	± 2	LSB
Zero-Point Error			—	—	± 1	± 3	± 2	
Full-Scale Error			—	—	± 1	± 3	± 2	
Total Error			—	—	± 2	± 6	± 4	

Note 1 : ADCDR1: 8-bit A/D conversion value (1LSB = ΔV_{AREF}/256)
ADCDR2: 10-bit A/D conversion value (1LSB = ΔV_{AREF}/1024)
Note 2 : Total error includes all errors except quantization error.