

Networking Clock Source

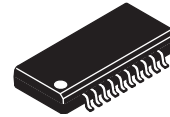
The MPC926508 is a low cost, low jitter, high performance clock synthesizer for networking applications. Using analog Phase-Locked Loop (PLL) techniques, the device accepts an input to produce multiple output clocks for networking chips, PCI devices, SDRAM, and ASICs. The MPC926508 outputs all have 0 ppm synthesis error.

Features

- Packaged in 20 pin narrow (150 mil) SSOP (QSOP)
- 25 or 125 MHz fundamental clock input or 25 MHz crystal input
- Two output clocks
- SDRAM frequencies of 100 and 133 MHz
- Zero ppm synthesis error in all clocks
- Full CMOS output swing with 25 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 3.3V operating voltage

MPC926508

NETWORKING CLOCK SOURCE



SD SUFFIX
20 LEAD SSOP
CASE 1461

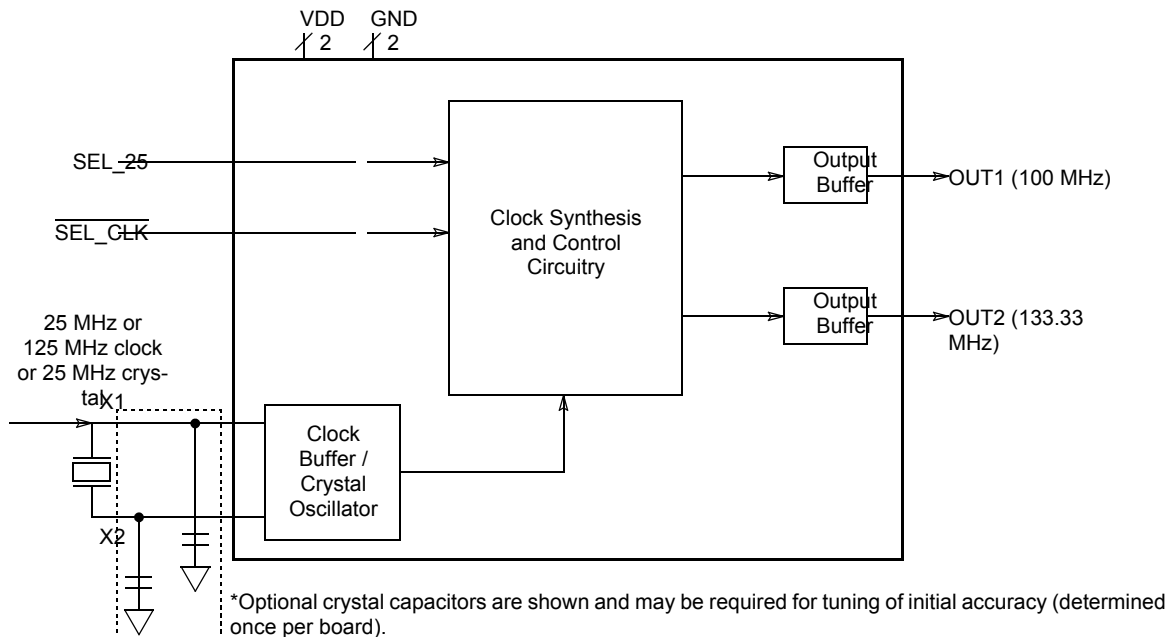


Table 1. Function table

Control	Default	0	1
SEL_25	1	125	25
SEL_CLK	1	XTAL	REF_CLK

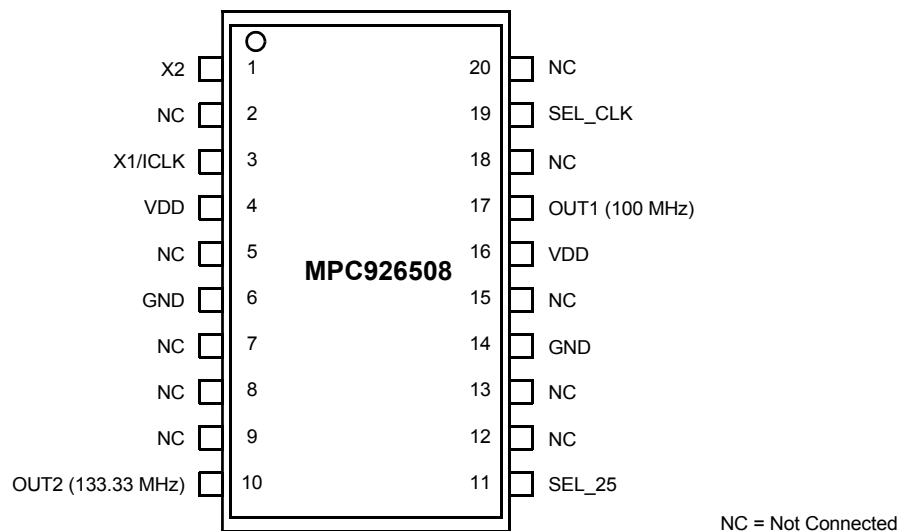


Figure 1. MPC926508 Pin Assignment

Table 2. Pin Description

Number	Name	Type	Description
1	X2	XO	Crystal connection. Connect to a crystal or leave unconnected for a clock input.
2	NC	-	Not Connected
3	X1/ICLK	XI	Crystal connection. Connect to a fundamental crystal or clock input.
4	VDD	P	Connect to +3.3 V. Must be same as other VDD.
5	NC	-	Not Connected
6	GND	P	Connect to ground.
7	NC	-	Not Connected
8	NC	-	Not Connected
9	NC	-	Not Connected
10	OUT1 (133.33 MHz)	O	133.33 MHz Output
11	SEL_25	I	REF_CLK or XTAL Input Selection.
12	NC	-	Not Connected
13	NC	-	Not Connected
14	GND	P	Connect to ground.
15	NC	-	Not Connected
16	VDD	P	Connect to +3.3 V. Must be same as other VDD.
17	OUT2 (100 MHz)	O	100 MHz Output
18	NC	-	Not Connected
19	SEL_CLK	I	25 or 125 MHz REF_CLK Selection.
20	NC	-	Not Connected

Key: XI, XO = crystal connections; I = Input with internal pull-up resistor; O = Output; P = power supply connection.

Table 3. ABSOLUTE MAXIMUM RATINGS^a

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{DD}	Supply Voltage			3.9	V	Referenced to GND
	Inputs and Clock Outputs	-0.5		V _{DD} + 0.5	V	Referenced to GND
T _A	Ambient Operating Temperature	0		70	°C	
T _A	Ambient Operating Temperature, I version	-40		85	°C	Industrial temp
T _{SOL}	Soldering Temperature			260	°C	Max of 20 seconds
T _S	Storage Temperature	-65		150	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. DC CHARACTERISTICS (V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V _{IH}	Input High VoltageX1 pin only all I type inputs	V _{DD} /2+1 2	V _{DD} /2		V V	
V _{IL}	Input Low VoltageX1 pin only all I type inputs		V _{DD} /2	V _{DD} /2-1 0.8	V V	
V _{OH}	Output High Voltage	2.4			V	I _{OH} =-25 mA
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 25 mA
V _{OH}	Output High Voltage, CMOS level	V _{DD} - 0.4			V	I _{OH} =-8 mA
I _{DD}	Operating Supply Current		35		mA	No Load
	Short Circuit Current		90		mA	Each Output
	Internal Pull-Up Resistor		200		kΩ	SEL_25, SEL_CLK

Table 5. AC CHARACTERISTICS (V_{DD} = 3.3V ± 10%, T_A = -40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f _{REF}	Input Frequency	12	25	27	MHz	Crystal Oscillator
f _{REF}	Input Frequency		125		MHz	External Input
t _r	Output Clock Rise Time		1		ns	0.8 to 2.0V
t _f	Output Clock Fall Time		1		ns	2.0 to 0.8V
DC _O	Output Clock Duty Cycle	40	50	60	%	At V _{DD} /2
	Frequency Error			0	ppm	All clocks
t _{JIT(CC)}	Jitter (Cycle-to-Cycle)		300		ps	Variation from mean

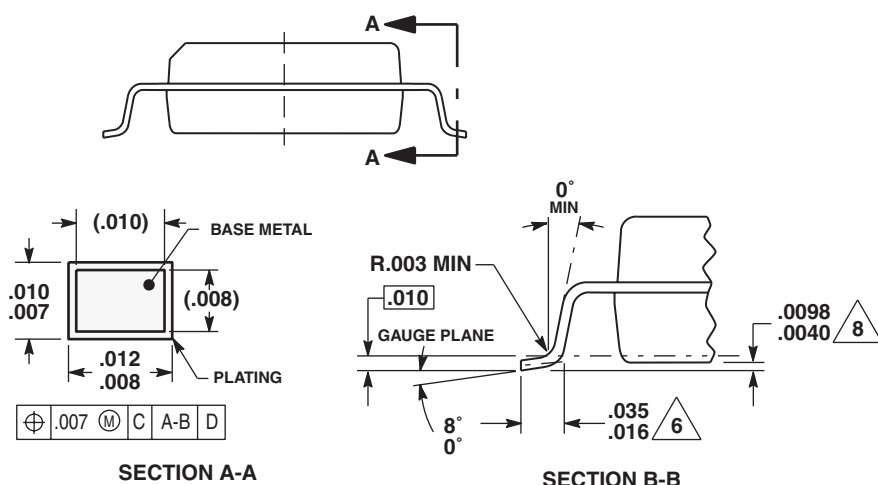
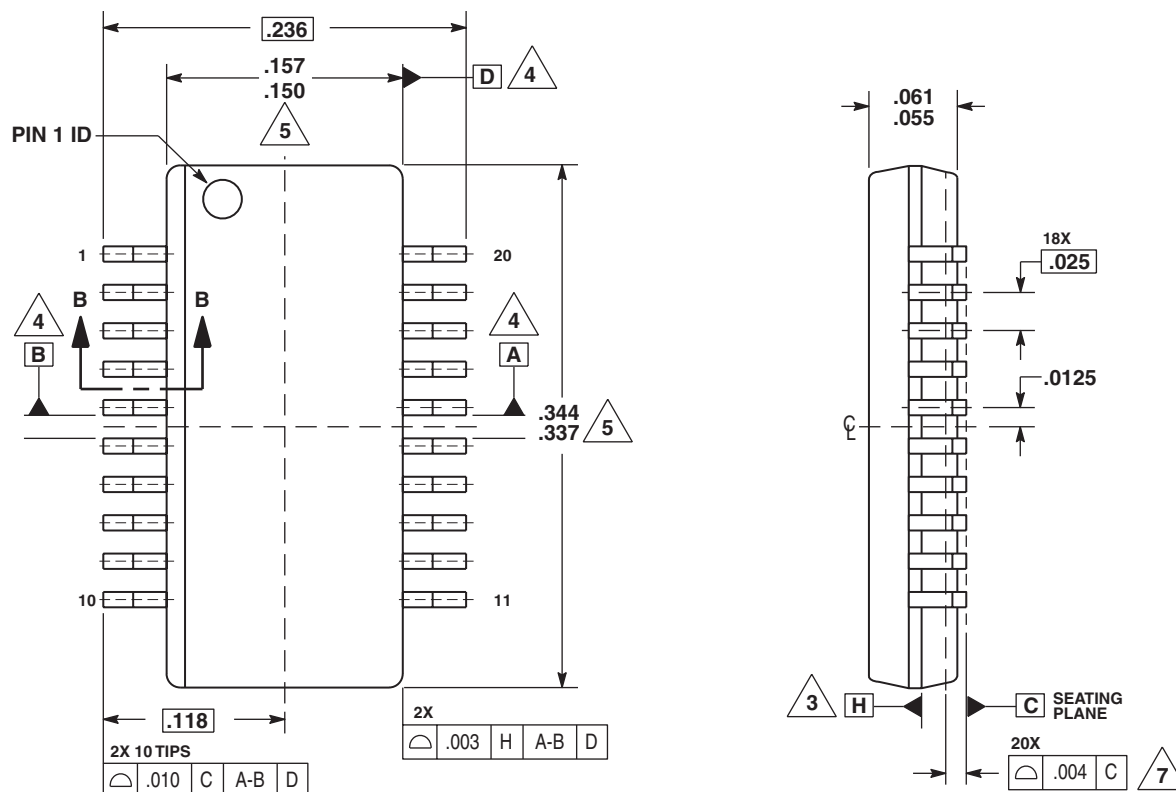
APPLICATIONS INFORMATION

External Components

The MPC926508 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01 μ F should be connected between each VDD and GND (pins 4 and 6, pins 16 and 14), as close to the MPC926508 as possible. A series termination resistor of 33 Ω may be used for each clock output. The crystal must be connected as close to the chip as possible. The crystal should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation, where C_L is the crystal load capacitance: Crystal caps (pF) = $(C_L - 6) \times 2$. So for a crystal with 16 pF load capacitance, two 20 pF caps should be used.

PACKAGE DIMENSIONS

SD SUFFIX
20-LEAD SSOP PACKAGE
CASE 1461-01
ISSUE O



NOTES:

1. DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5m, 1994.
3. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
4. DATUM A, B AND D TO BE DETERMINED WHERE CENTERLINE BETWEEN LEADS EXITS PLASTIC BODY AT DATUM PLANE H.
5. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES FOR ENDS AND .008 INCHES FOR SIDES.
6. THIS DIMENSION IS LENGTH OF TERMINAL FOR SOLDERING A SUBSTRATE.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004 INCHES AT SEATING PLANE.
8. THIS DIMENSION IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

CASE 1467-01
ISSUE O

DATE 11/20/02

NOTES

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MPC926508

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