

# MC10EP131, MC100EP131

## 3.3V / 5V ECL Quad D Flip-Flop with Set, Reset, and Differential Clock

The MC10/100EP131 is a Quad Master-slaved D flip-flop with common set and separate resets. The device is an expansion of the E131 with differential common clock and individual clock enables. With AC performance faster than the E131 device, the EP131 is ideal for applications requiring the fastest AC performance available.

Each flip-flop may be clocked separately by holding Common Clock ( $C_C$ ) LOW and  $\overline{C_C}$  HIGH, then using the differential Clock Enable inputs for clocking ( $C_{0-3}$ ,  $\overline{C_{0-3}}$ ).

Common clocking is achieved by holding the differential inputs  $C_{0-3}$  LOW and  $\overline{C_{0-3}}$  HIGH while using the differential Common Clock ( $C_C$ ) to clock all four flip-flops. When left floating open, any differential input will disable operation due to input pulldown resistors forcing an output default state.

Individual asynchronous resets ( $R_{0-3}$ ) and an asynchronous set (SET) are provided.

Data enters the master when both  $C_C$  and  $C_{0-3}$  are LOW, and transfers to the slave when either  $C_C$  or  $C_{0-3}$  (or both) go HIGH.

The 100 Series contains temperature compensation.

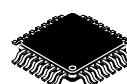
- 460 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- Differential Individual and Common Clocks
- Individual Asynchronous Resets
- Asynchronous Set
- PECL Mode Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$
- Open Input Default State
- Safety Clamp on Inputs
- Q Output Will Default LOW with Inputs Open or at  $V_{EE}$



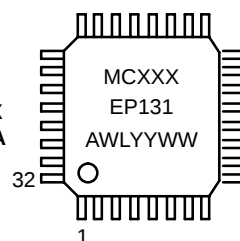
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM\*



LQFP-32  
FA SUFFIX  
CASE 873A



XXX = 10 or 100  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

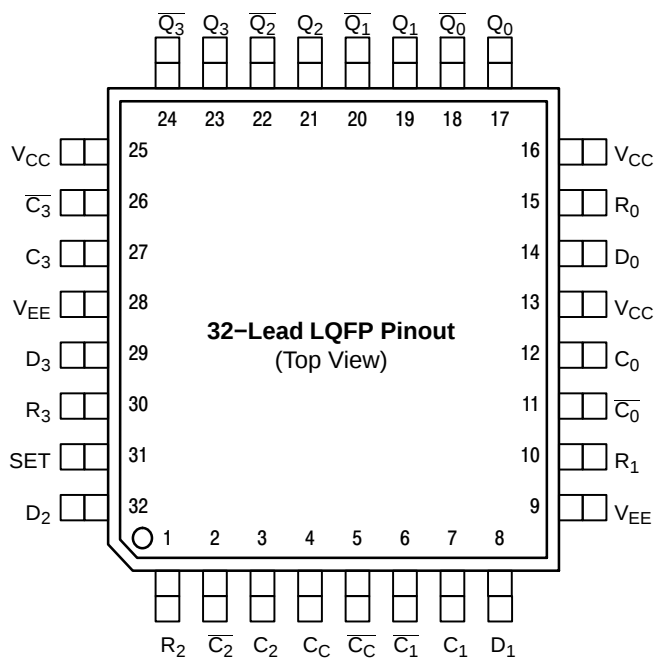
\*For additional information, see Application Note AND8002/D

### ORDERING INFORMATION

| Device         | Package | Shipping†        |
|----------------|---------|------------------|
| MC10EP131FA    | LQFP-32 | 250 Units/Tray   |
| MC10EP131FAR2  | LQFP-32 | 2000 Tape & Reel |
| MC100EP131FA   | LQFP-32 | 250 Units/Tray   |
| MC100EP131FAR2 | LQFP-32 | 2000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# MC10EP131, MC100EP131



Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32-Lead LQFP Pinout (Top View)

## PIN DESCRIPTION

| PIN                               | FUNCTION                  |
|-----------------------------------|---------------------------|
| $D_{0-3}^*$                       | ECL Data Inputs           |
| $C_{0-3}^*, \overline{C}_{0-3}^*$ | ECL Separate Clock Inputs |
| $C_C^*, \overline{C}_C^*$         | ECL Common Clock Inputs   |
| $R_{0-3}^*$                       | ECL Asynchronous Reset    |
| SET*                              | ECL Asynchronous Set      |
| $Q_{0-3}, \overline{Q}_{0-3}$     | ECL Data Outputs          |
| $V_{CC}$                          | Positive Supply           |
| $V_{EE}$                          | Negative Supply           |

\* Pins will default LOW when left open.

## TRUTH TABLE

| D | S* | R* | CLK | Q     |
|---|----|----|-----|-------|
| L | L  | L  | Z   | L     |
| H | L  | L  | Z   | H     |
| X | H  | L  | X   | H     |
| X | L  | H  | X   | L     |
| X | H  | H  | X   | Undef |

Z = LOW to HIGH Transition

\* Pins will default low when left open.

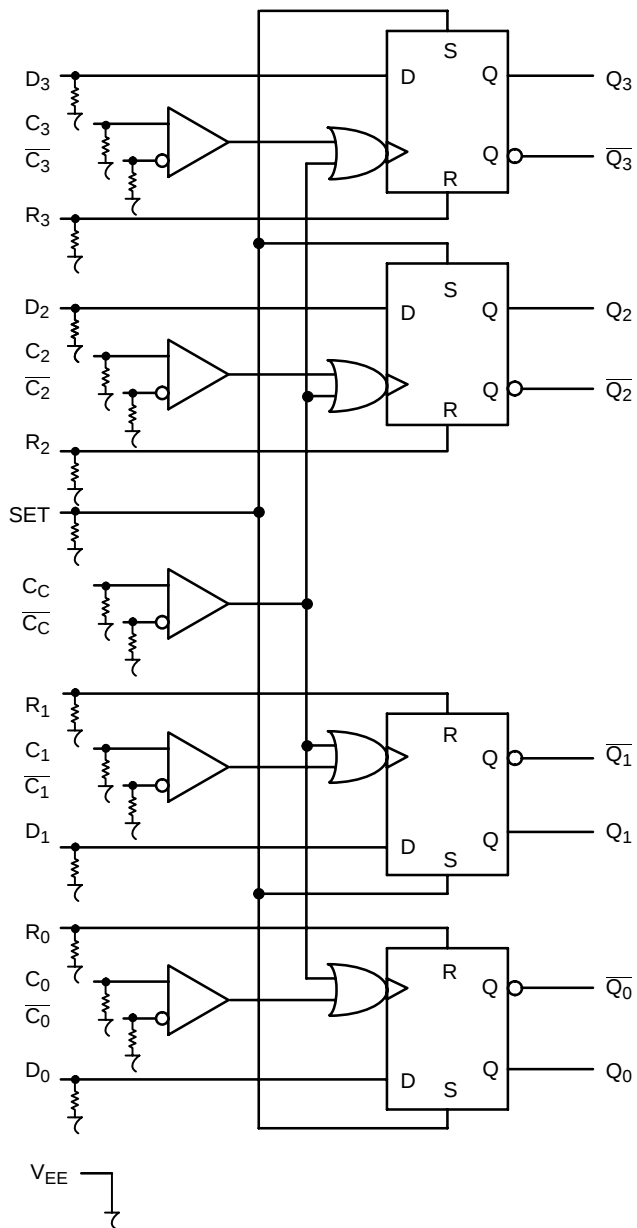


Figure 2. Logic Diagram

# MC10EP131, MC100EP131

## ATTRIBUTES

| Characteristics                                        | Value                                                     |
|--------------------------------------------------------|-----------------------------------------------------------|
| Internal Input Pulldown Resistor                       | 75 k $\Omega$                                             |
| Internal Input Pullup Resistor                         | N/A                                                       |
| ESD Protection                                         | Human Body Model<br>Machine Model<br>Charged Device Model |
|                                                        | > 2 kV<br>> 100 V<br>> 2 kV                               |
| Moisture Sensitivity (Note 1)                          | Level 2                                                   |
| Flammability Rating                                    | Oxygen Index: 28 to 34                                    |
|                                                        | UL 94 V-0 @ 0.125 in                                      |
| Transistor Count                                       | 935 Devices                                               |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test |                                                           |

1. For additional information, see Application Note AND8003/D.

## MAXIMUM RATINGS (Note 2)

| Symbol           | Parameter                                          | Condition 1                                    | Condition 2                                                          | Rating      | Units        |
|------------------|----------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------|-------------|--------------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |                                                                      | 6           | V            |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |                                                                      | -6          | V            |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> ≤ V <sub>CC</sub><br>V <sub>I</sub> ≥ V <sub>EE</sub> | 6<br>-6     | V<br>V       |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |                                                                      | 50<br>100   | mA<br>mA     |
| I <sub>BB</sub>  | V <sub>BB</sub> Sink/Source                        |                                                |                                                                      | ± 0.5       | mA           |
| T <sub>A</sub>   | Operating Temperature Range                        |                                                |                                                                      | -40 to +85  | °C           |
| T <sub>stg</sub> | Storage Temperature Range                          |                                                |                                                                      | -65 to +150 | °C           |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 LFPM<br>500 LFPM                             | 32 LQFP<br>32 LQFP                                                   | 80<br>55    | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | std bd                                         | 32 LQFP                                                              | 12 to 17    | °C/W         |
| T <sub>sol</sub> | Wave Solder                                        | > 2 to 3 sec @ 248°C                           |                                                                      | 265         | °C           |

2. Maximum Ratings are those values beyond which device damage may occur.

# MC10EP131, MC100EP131

## 10EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 3)

| Symbol      | Characteristic                                               | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|--------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|             |                                                              | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                         | 70    | 95   | 120  | 70   | 95   | 120  | 70   | 95   | 120  | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 4)                                 | 2165  | 2290 | 2415 | 2230 | 2355 | 2480 | 2290 | 2415 | 2540 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 4)                                  | 1365  | 1490 | 1615 | 1430 | 1555 | 1680 | 1490 | 1615 | 1740 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                            | 2090  |      | 2415 | 2155 |      | 2480 | 2215 |      | 2540 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                             | 1365  |      | 1690 | 1460 |      | 1755 | 1490 |      | 1815 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 5) | 2.0   |      | 3.3  | 2.0  |      | 3.3  | 2.0  |      | 3.3  | V             |
| $I_{IH}$    | Input HIGH Current                                           |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                            | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

4. All loading with 50  $\Omega$  to  $V_{CC}$ -2.0 volts.

5.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## 10EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 6)

| Symbol      | Characteristic                                               | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|--------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|             |                                                              | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                         | 70    | 95   | 120  | 70   | 95   | 120  | 70   | 95   | 120  | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 7)                                 | 3865  | 3990 | 4115 | 3930 | 4055 | 4180 | 3990 | 4115 | 4240 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 7)                                  | 3065  | 3190 | 3315 | 3130 | 3255 | 3380 | 3190 | 3315 | 3440 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                            | 3790  |      | 4115 | 3855 |      | 4180 | 3915 |      | 4240 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                             | 3065  |      | 3390 | 3130 |      | 3455 | 3190 |      | 3515 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 8) | 2.0   |      | 5.0  | 2.0  |      | 5.0  | 2.0  |      | 5.0  | V             |
| $I_{IH}$    | Input HIGH Current                                           |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                            | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

7. All loading with 50  $\Omega$  to  $V_{CC}$ -2.0 volts.

8.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## 10EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$ , $V_{EE} = -5.5\text{ V}$ to -3.0 V (Note 9)

| Symbol      | Characteristic                                                | -40°C        |       |       | 25°C         |       |       | 85°C         |       |       | Unit          |
|-------------|---------------------------------------------------------------|--------------|-------|-------|--------------|-------|-------|--------------|-------|-------|---------------|
|             |                                                               | Min          | Typ   | Max   | Min          | Typ   | Max   | Min          | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current                                          | 70           | 95    | 120   | 70           | 95    | 120   | 70           | 95    | 120   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 10)                                 | -1135        | -1010 | -885  | -1070        | -945  | -820  | -1010        | -885  | -760  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 10)                                  | -1935        | -1810 | -1685 | -1870        | -1745 | -1620 | -1810        | -1685 | -1560 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                             | -1210        |       | -885  | -1145        |       | -820  | -1085        |       | -760  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                              | -1935        |       | -1610 | -1870        |       | -1545 | -1810        |       | -1485 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 11) | $V_{EE}+2.0$ |       | 0.0   | $V_{EE}+2.0$ |       | 0.0   | $V_{EE}+2.0$ |       | 0.0   | V             |
| $I_{IH}$    | Input HIGH Current                                            |              |       | 150   |              |       | 150   |              |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                             | 0.5          |       |       | 0.5          |       |       | 0.5          |       |       | $\mu\text{A}$ |

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

9. Input and output parameters vary 1:1 with  $V_{CC}$ .

10. All loading with 50  $\Omega$  to  $V_{CC}$ -2.0 volts.

11.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# MC10EP131, MC100EP131

## 100EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 12)

| Symbol      | Characteristic                                                | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|---------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|             |                                                               | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                          | 70    | 95   | 120  | 75   | 97   | 120  | 80   | 105  | 130  | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 13)                                 | 2155  | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 13)                                  | 1355  | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                             | 2075  |      | 2420 | 2075 |      | 2420 | 2075 |      | 2420 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                              | 1355  |      | 1675 | 1355 |      | 1675 | 1355 |      | 1675 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 14) | 2.0   |      | 3.3  | 2.0  |      | 3.3  | 2.0  |      | 3.3  | V             |
| $I_{IH}$    | Input HIGH Current                                            |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                             | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

12. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

13. All loading with 50  $\Omega$  to  $V_{CC}$ -2.0 volts.

14.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## 100EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 15)

| Symbol      | Characteristic                                                | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|---------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|             |                                                               | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                          | 70    | 95   | 120  | 75   | 97   | 120  | 80   | 105  | 130  | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 16)                                 | 3855  | 3980 | 4105 | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 16)                                  | 3055  | 3180 | 3305 | 3055 | 3180 | 3305 | 3055 | 3180 | 3305 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                             | 3775  |      | 4120 | 3775 |      | 4120 | 3775 |      | 4120 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                              | 3055  |      | 3375 | 3055 |      | 3375 | 3055 |      | 3375 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 17) | 2.0   |      | 5.0  | 2.0  |      | 5.0  | 2.0  |      | 5.0  | V             |
| $I_{IH}$    | Input HIGH Current                                            |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                             | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

15. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

16. All loading with 50  $\Omega$  to  $V_{CC}$ -2.0 volts.

17.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$ , $V_{EE} = -5.5\text{ V}$ to -3.0 V (Note 18)

| Symbol      | Characteristic                                                | -40°C        |       |       | 25°C         |       |       | 85°C         |       |       | Unit          |
|-------------|---------------------------------------------------------------|--------------|-------|-------|--------------|-------|-------|--------------|-------|-------|---------------|
|             |                                                               | Min          | Typ   | Max   | Min          | Typ   | Max   | Min          | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current                                          | 70           | 95    | 120   | 75           | 97    | 120   | 80           | 105   | 130   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 19)                                 | -1145        | -1020 | -895  | -1145        | -1020 | -895  | -1145        | -1020 | -895  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 19)                                  | -1945        | -1820 | -1695 | -1945        | -1820 | -1695 | -1945        | -1820 | -1695 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                             | -1225        |       | -880  | -1225        |       | -880  | -1225        |       | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                              | -1945        |       | -1625 | -1945        |       | -1625 | -1945        |       | -1625 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 20) | $V_{EE}+2.0$ |       | 0.0   | $V_{EE}+2.0$ |       | 0.0   | $V_{EE}+2.0$ |       | 0.0   | V             |
| $I_{IH}$    | Input HIGH Current                                            |              |       | 150   |              |       | 150   |              |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                             | 0.5          |       |       | 0.5          |       |       | 0.5          |       |       | $\mu\text{A}$ |

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

18. Input and output parameters vary 1:1 with  $V_{CC}$ .

19. All loading with 50  $\Omega$  to  $V_{CC}$ -2.0 volts.

20.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

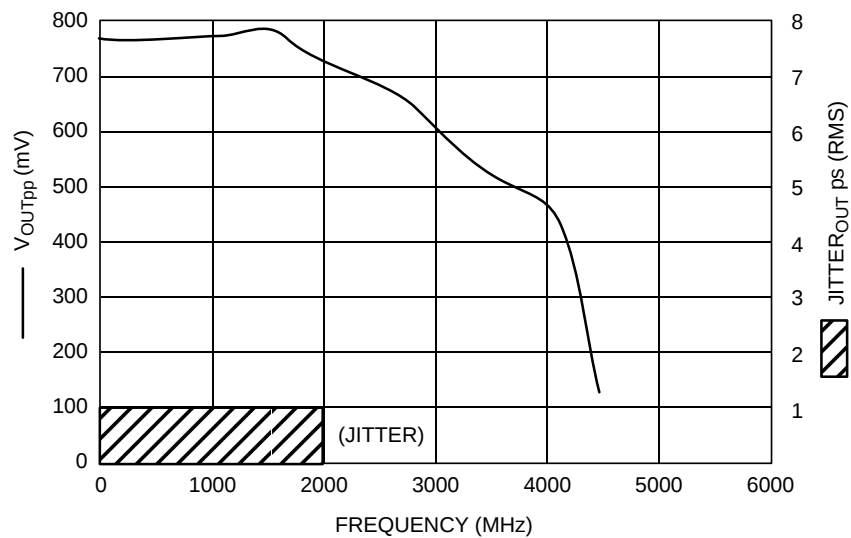
# MC10EP131, MC100EP131

**AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 21)

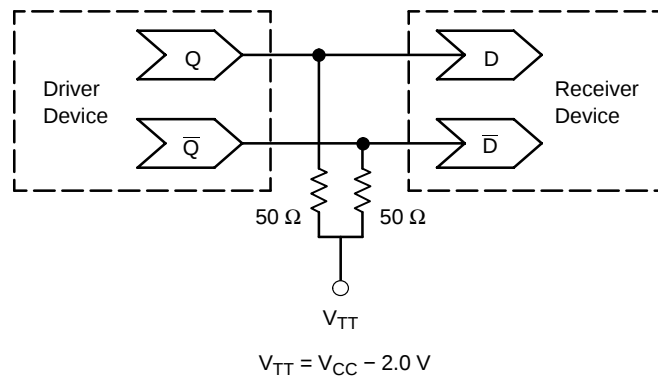
| Symbol                                 | Characteristic                                                                          | -40°C                                                         |                          |                          | 25°C                     |                          |                          | 85°C                     |                          |                          | Unit                     |    |
|----------------------------------------|-----------------------------------------------------------------------------------------|---------------------------------------------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|----|
|                                        |                                                                                         | Min                                                           | Typ                      | Max                      | Min                      | Typ                      | Max                      | Min                      | Typ                      | Max                      |                          |    |
| f <sub>max</sub>                       | Maximum Frequency<br>(See Figure 3. Frequency vs. V <sub>OUTpp</sub><br>and JITTER)     |                                                               | > 3                      |                          |                          | > 3                      |                          |                          | > 3                      |                          | GHz                      |    |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Propagation Delay to<br>Output Differential                                             | C <sub>0-3</sub><br>C <sub>C</sub><br>R <sub>0-3</sub><br>SET | 320<br>320<br>320<br>300 | 450<br>450<br>430<br>430 | 520<br>520<br>520<br>550 | 380<br>400<br>380<br>380 | 460<br>500<br>480<br>460 | 580<br>600<br>580<br>580 | 450<br>450<br>450<br>400 | 560<br>560<br>560<br>530 | 650<br>650<br>700<br>650 | ps |
| t <sub>RR</sub>                        | Set/R0-3 Recovery                                                                       |                                                               | 290                      | 210                      |                          | 290                      | 210                      |                          | 350                      | 280                      |                          | ps |
| t <sub>S</sub><br>t <sub>H</sub>       | Setup Time<br>Hold Time                                                                 |                                                               | 120                      | 80                       |                          | 120                      | 80                       |                          | 120                      | 80                       |                          | ps |
| t <sub>PW</sub>                        | Minimum Pulse Rate                                                                      | SET, R <sub>0-3</sub>                                         | 550                      | 400                      |                          | 550                      | 400                      |                          | 550                      | 400                      |                          |    |
| t <sub>JITTER</sub>                    | Cycle-to-Cycle Jitter<br>(See Figure 3. Frequency vs. V <sub>OUTpp</sub><br>and JITTER) |                                                               |                          | 0.2                      | < 1                      |                          | 0.2                      | < 1                      |                          | 0.2                      | < 1                      | ps |
| t <sub>r</sub><br>t <sub>f</sub>       | Output Rise/Fall Times<br>(20% – 80%)                                                   | Q, Q̄                                                         | 110                      | 180                      | 250                      | 125                      | 200                      | 275                      | 150                      | 230                      | 300                      | ps |

21. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50  $\Omega$  to  $V_{CC}-2.0\text{ V}$ .

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**Figure 3. Frequency vs. V<sub>OUTpp</sub> and JITTER**



**Figure 4. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020 – Termination of ECL Logic Devices.)**

### Resource Reference of Application Notes

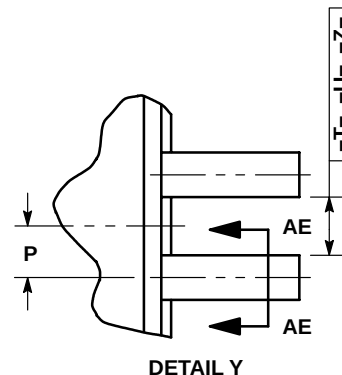
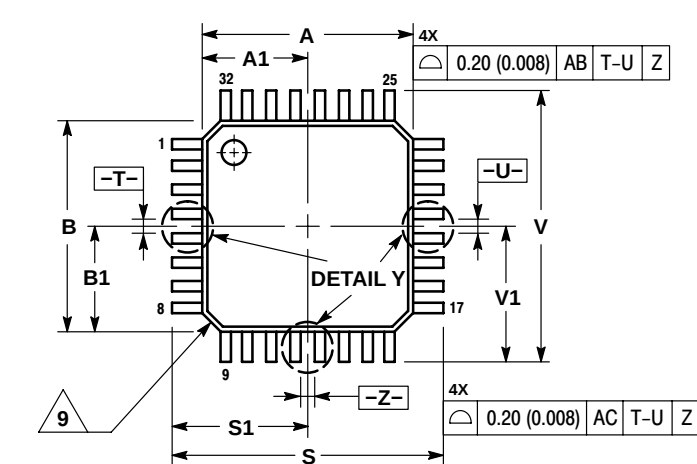
- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

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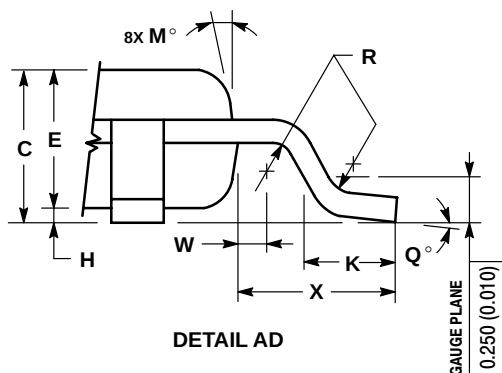
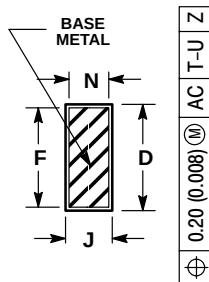
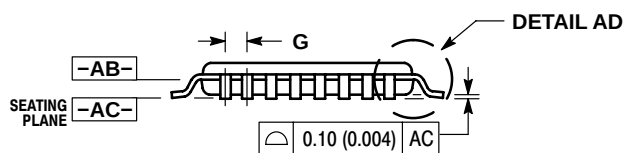
## PACKAGE DIMENSIONS

LQFP  
FA SUFFIX  
32-LEAD PLASTIC PACKAGE  
CASE 873A-02  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.



| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 7.000 BSC   |       | 0.276 BSC |       |
| A1  | 3.500 BSC   |       | 0.138 BSC |       |
| B   | 7.000 BSC   |       | 0.276 BSC |       |
| B1  | 3.500 BSC   |       | 0.138 BSC |       |
| C   | 1.400       | 1.600 | 0.055     | 0.063 |
| D   | 0.300       | 0.450 | 0.012     | 0.018 |
| E   | 1.350       | 1.450 | 0.053     | 0.057 |
| F   | 0.300       | 0.400 | 0.012     | 0.016 |
| G   | 0.800 BSC   |       | 0.031 BSC |       |
| H   | 0.050       | 0.150 | 0.002     | 0.006 |
| J   | 0.090       | 0.200 | 0.004     | 0.008 |
| K   | 0.500       | 0.700 | 0.020     | 0.028 |
| M   | 12° REF     |       | 12° REF   |       |
| N   | 0.090       | 0.160 | 0.004     | 0.006 |
| P   | 0.400 BSC   |       | 0.016 BSC |       |
| Q   | 1°          | 5°    | 1°        | 5°    |
| R   | 0.150       | 0.250 | 0.006     | 0.010 |
| S   | 9.000 BSC   |       | 0.354 BSC |       |
| S1  | 4.500 BSC   |       | 0.177 BSC |       |
| V   | 9.000 BSC   |       | 0.354 BSC |       |
| V1  | 4.500 BSC   |       | 0.177 BSC |       |
| W   | 0.200 REF   |       | 0.008 REF |       |
| X   | 1.000 REF   |       | 0.039 REF |       |

## **Notes**

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