HIGH PERFORMANCE CMOS BUS INTERFACE REGISTER

IDT54/74FCT823A/B/C

FEATURES:

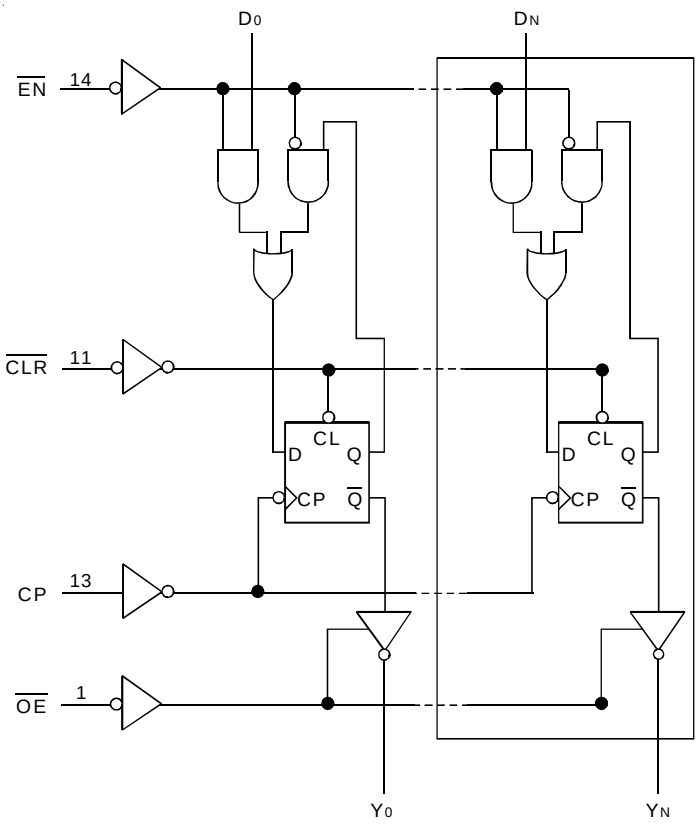
- **Equivalent to AMD's Am29823 bipolar registers in pinout/ function, speed, and output drive over full temperature and voltage supply extremes**
- **IDT54/74FCT823A equivalent to FAST™ speed**
- **IDT54FCT823B 25% faster than FAST**
- **IDT74FCT823C 40% faster than FAST**
- **Buffered common Clock Enable ($\overline{EN}$) and Asynchronous Clear Input ($\overline{CLR}$)**
- **I_{OL} = 48mA (commercial) and 32mA (military)**
- **Clamp diodes on all inputs for ringing suppression**
- **CMOS power levels (1mW typ. static)**
- **TTL input and output compatibility**
- **CMOS output level compatible**
- **Substantially lower input current levels than AMD's bilopar Am29800 series (5µA max.)**
- **MIlitary product compliant to MIL-STD-883, Class B**
- **Available in the following packages:**
  - Commercial: SOIC
  - Military: CERDIP, LCC

DESCRIPTION:

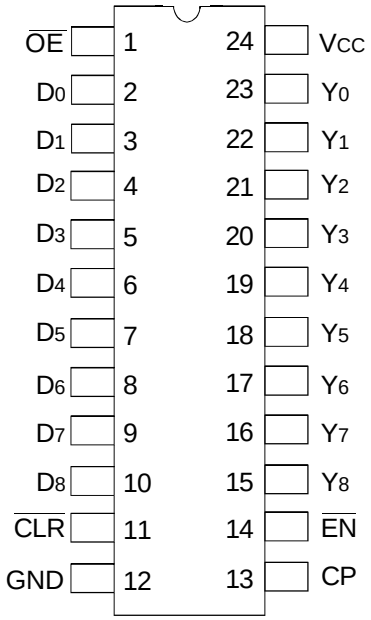
The FCT823 series is built using an advanced dual metal CMOS technology. The FCT823 bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The FCT823 is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems.

The FCT823 high-performance interface family is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

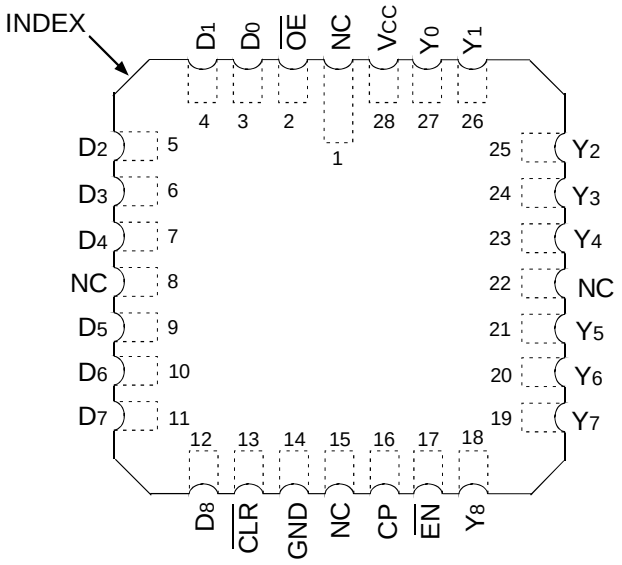
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

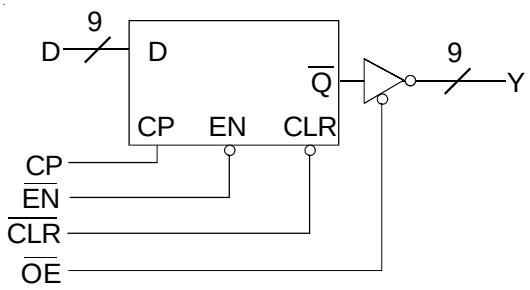


CERDIP/ SOIC
TOP VIEW



LCC
TOP VIEW

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature under BIAS	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Name	I/O	Description
Dx	I	D flip-flop data inputs
CLR	I	For both inverting and non-inverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_x outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Yx	O	Register 3-state outputs
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_I input is transferred to the Q_I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_I outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Yx outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Yx outputs.

FUNCTION TABLE[1]

Inputs					Internal/ Outputs		
OE	CLR	EN	Dx	CP	Qx	Yx	Function
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10[4]	
I_{OZL}			V_O = 0.5V	—	—	–10[4]	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–75	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –15mA MIL	2.4	4.3	—	
			I_{OH} = –24mA COM'L	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM'L	—	0.3	0.5	

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not ttested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = $\overline{EN}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND One Bit Toggling at fi = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND at fi = 2.5MHz Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for register devices (zero for non-register devices)
   fi = Input Frequency
   Ni = Number of Inputs at fi

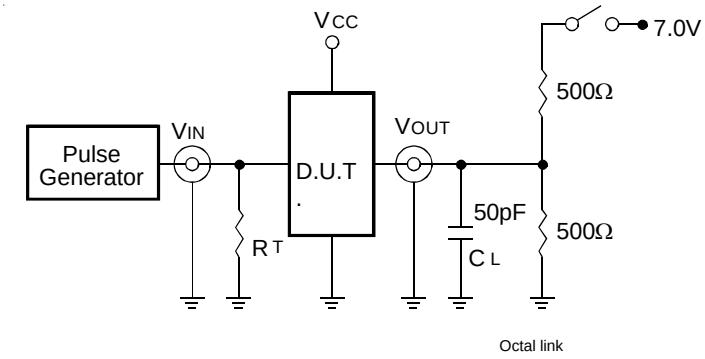
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

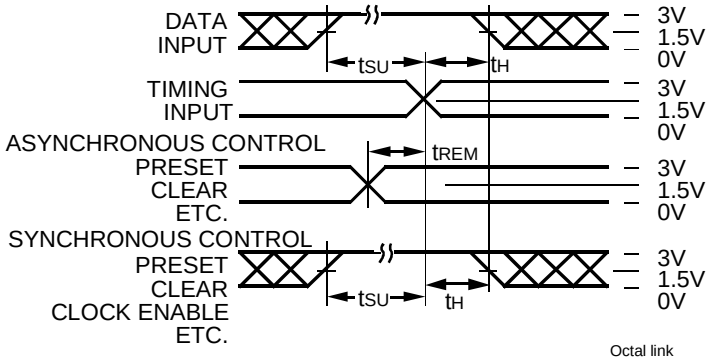
Symbol	Parameter	Condition[1]	54/74FCT823A				54FCT823B		74FCT823C		Unit
			Com'l.		Mil.		Mil.		Com'l.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Yx ($\overline{OE}$ = LOW)	C_L = 50pF R_L = 500Ω	—	10	—	11.5	—	8.5	—	6	ns
		C_L = 300pF[3] R_L = 500Ω	—	20	—	20	—	16	—	12.5	
t_{PZH} t_{PZL}	Output Enable Time, $\overline{OE}$ to Yx	C_L = 50pF R_L = 500Ω	—	12	—	13	—	9	—	7	ns
		C_L = 300pF[3] R_L = 500Ω	—	23	—	25	—	16	—	12.5	
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{OE}$ to Yx	C_L = 5pF[3] R_L = 500Ω	—	7	—	8	—	7	—	6.2	ns
		C_L = 50pF R_L = 500Ω	—	8	—	9	—	8	—	6.5	
t_{SU}	Set-up Time HIGH or LOW, Dx to CP	C_L = 50pF R_L = 500Ω	4	—	4	—	3	—	3	—	ns
	Set-up Time HIGH or LOW, $\overline{EN}$ to CP										
t_H	Hold Time HIGH or LOW, Dx to CP		2	—	2	—	1.5	—	1.5	—	ns
t_H	Hold Time HIGH or LOW, $\overline{EN}$ to CP		2	—	2	—	0	—	0	—	ns
t_{PHL}	Propagation Delay, $\overline{CLR}$ to Yx		—	14	—	15	—	9.5	—	8	ns
t_{REM}	Recovery Time, $\overline{CLR}$ to CP		6	—	7	—	6	—	6	—	ns
t_W	CP Pulse Width HIGH or LOW		7	—	7	—	6	—	6	—	ns
t_W	$\overline{CLR}$ Pulse Width HIGH or LOW		6	—	7	—	6	—	6	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

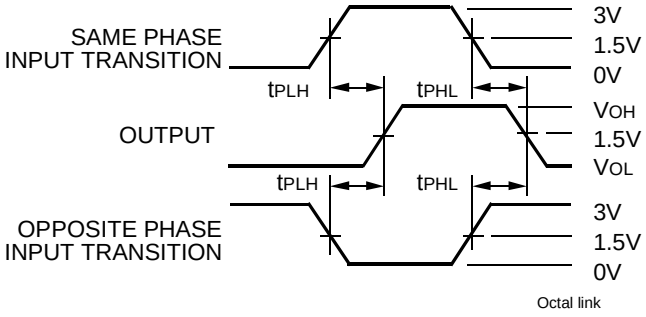
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



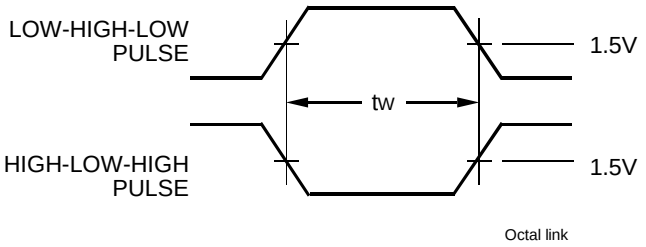
Propagation Delay

SWITCH POSITION

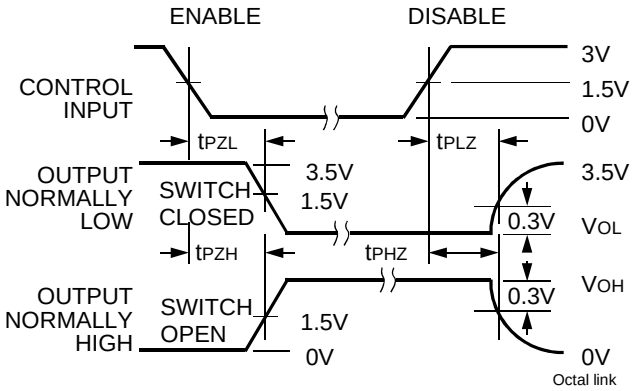
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

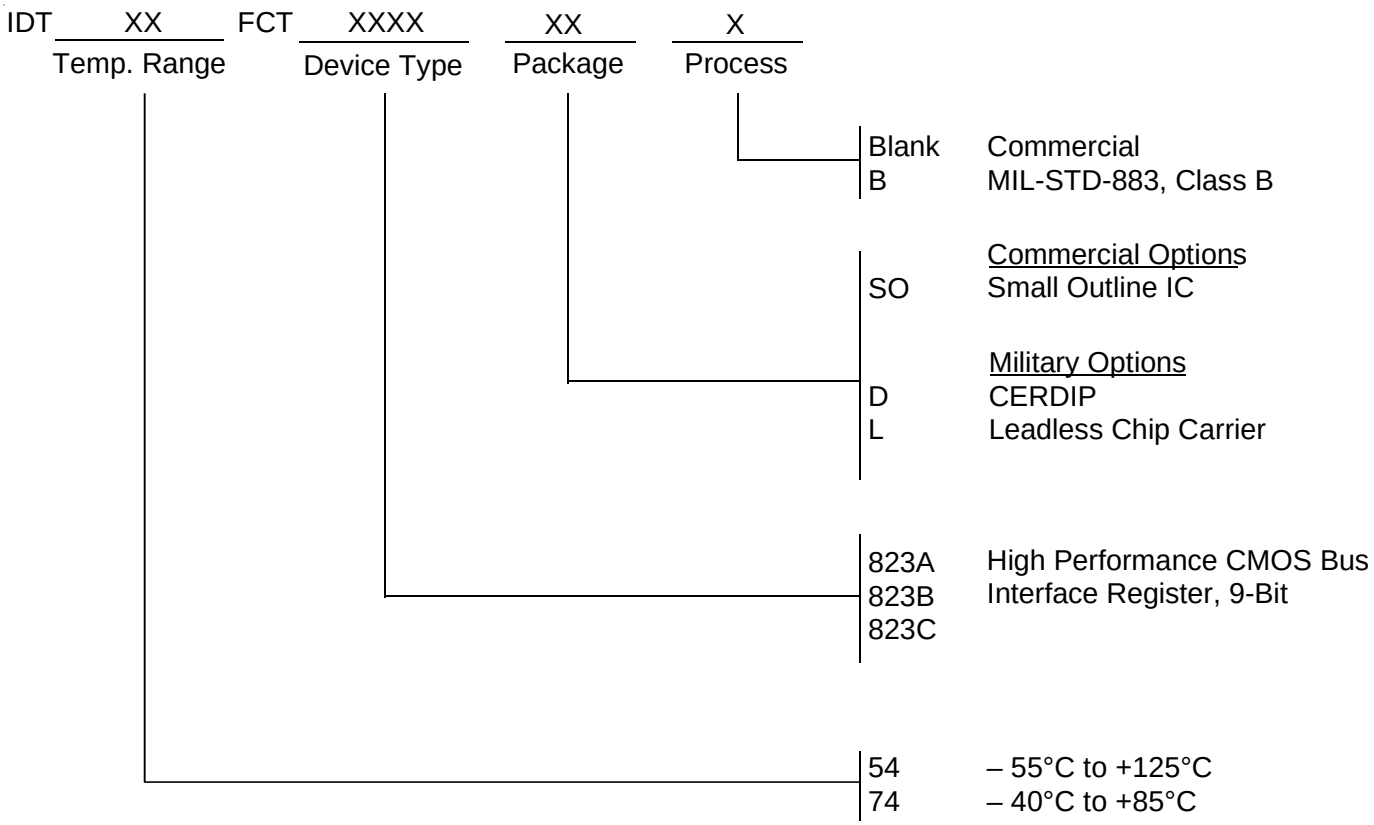


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

6/27/2002 Updated according to PDNs Logic-00-07 and Logic-01-04

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