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## FEATURES

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10  $\mu$ A (Max.) @  $V_{DS} = -60V$
- Lower  $R_{DS(ON)}$  : 0.362  $\Omega$  (Typ.)

$$BV_{DSS} = -60 V$$

$$R_{DS(on)} = 0.5 \Omega$$

$$I_D = -5.3 A$$

D-PAK

I-PAK



1. Gate 2. Drain 3. Source

## Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	-60	V
$I_D$	Continuous Drain Current ( $T_C=25^\circ C$ )	-5.3	A
	Continuous Drain Current ( $T_C=100^\circ C$ )	-3.7	
$I_{DM}$	Drain Current-Pulsed ①	21	A
$V_{GS}$	Gate-to-Source Voltage ②	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy	120	mJ
$I_{AR}$	Avalanche Current ①	-5.3	A
$E_{AR}$	Repetitive Avalanche Energy ①	2.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
$P_D$	Total Power Dissipation ( $T_A=25^\circ C$ ) *	2.5	W
	Total Power Dissipation ( $T_C=25^\circ C$ )	24	W
	Linear Derating Factor	0.19	W/ $^\circ C$
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

## Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	5.21	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient *	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

\* When mounted on the minimum pad size recommended (PCB Mount).

**Electrical Characteristics** ( $T_C=25^\circ\text{C}$  unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$BV_{DSS}$	Drain-Source Breakdown Voltage	-60	--	--	V	$V_{GS}=0V, I_D=-250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	-0.05	--	$V/^\circ\text{C}$	$I_D=-250\mu A$ <b>See Fig 7</b>
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	--	-4.0	V	$V_{DS}=-5V, I_D=-250\mu A$
$I_{GSS}$	Gate-Source Leakage, Forward	--	--	-100	nA	$V_{GS}=-20V$
	Gate-Source Leakage, Reverse	--	--	100		$V_{GS}=20V$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	-10	$\mu A$	$V_{DS}=-60V$
		--	--	-100		$V_{DS}=-48V, T_C=125^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.5	$\Omega$	$V_{GS}=-10V, I_D=-2.7A$ ④
$g_{fs}$	Forward Transconductance	--	2.2	--	S	$V_{DS}=-30V, I_D=-2.7A$ ④
$C_{iss}$	Input Capacitance	--	270	350	pF	$V_{GS}=0V, V_{DS}=-25V, f=1\text{MHz}$ <b>See Fig 5</b>
$C_{oss}$	Output Capacitance	--	90	135		
$C_{rss}$	Reverse Transfer Capacitance	--	25	35		
$t_{d(on)}$	Turn-On Delay Time	--	10	30	ns	$V_{DD}=-30V, I_D=-6.7A,$ $R_G=24\Omega$ <b>See Fig 13</b> ④⑤
$t_r$	Rise Time	--	19	50		
$t_{d(off)}$	Turn-Off Delay Time	--	21	50		
$t_f$	Fall Time	--	16	40		
$Q_g$	Total Gate Charge	--	9	11	nC	$V_{DS}=-48V, V_{GS}=-10V,$ $I_D=-6.7A$ <b>See Fig 6 &amp; Fig 12</b> ④⑤
$Q_{gs}$	Gate-Source Charge	--	1.8	--		
$Q_{gd}$	Gate-Drain("Miller") Charge	--	4.2	--		

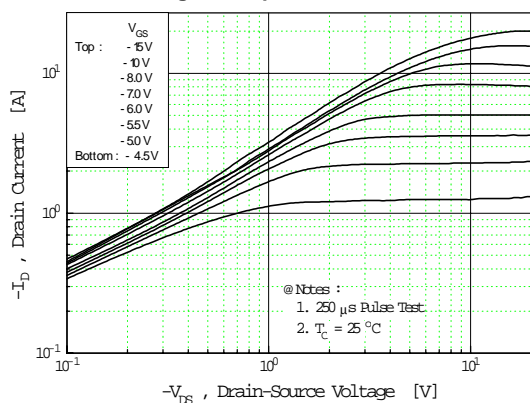
**Source-Drain Diode Ratings and Characteristics**

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$I_S$	Continuous Source Current	--	--	-5.3	A	Integral reverse pn-diode in the MOSFET
$I_{SM}$	Pulsed-Source Current ①	--	--	-21		
$V_{SD}$	Diode Forward Voltage ④	--	--	-3.8	V	$T_J=25^\circ\text{C}, I_S=-5.3A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	--	75	--	ns	$T_J=25^\circ\text{C}, I_F=-6.7A$
$Q_{rr}$	Reverse Recovery Charge	--	0.17	--	$\mu C$	$di_F/dt=100A/\mu s$ ④

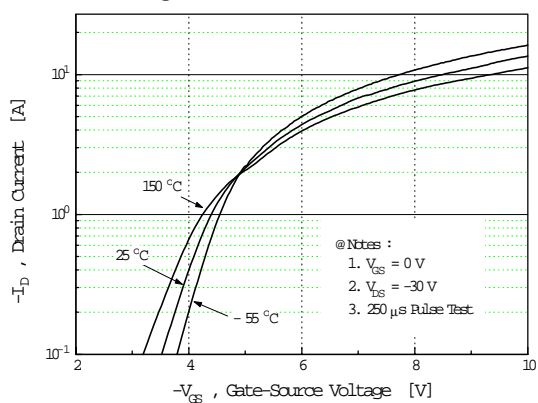
**Notes ;**

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature  
 ②  $L=5.0mH, I_{AS}=-5.3A, V_{DD}=-25V, R_G=27\Omega^*,$  Starting  $T_J=25^\circ\text{C}$   
 ③  $I_{SD}\leq -6.7A, di/dt\leq 200A/\mu s, V_{DD}\leq BV_{DSS},$  Starting  $T_J=25^\circ\text{C}$   
 ④ Pulse Test : Pulse Width =  $250\mu s,$  Duty Cycle  $\leq 2\%$   
 ⑤ Essentially Independent of Operating Temperature

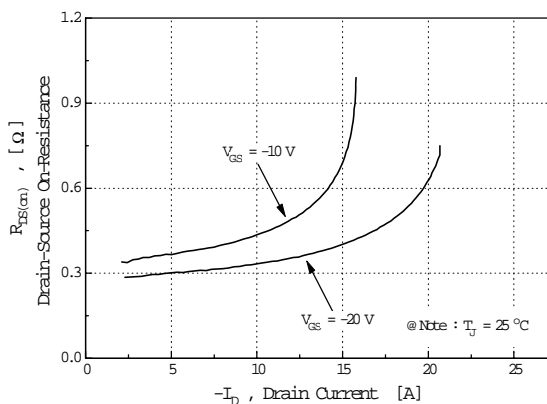
**Fig 1. Output Characteristics**



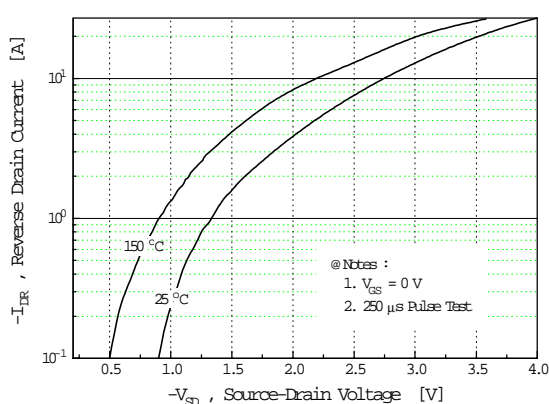
**Fig 2. Transfer Characteristics**



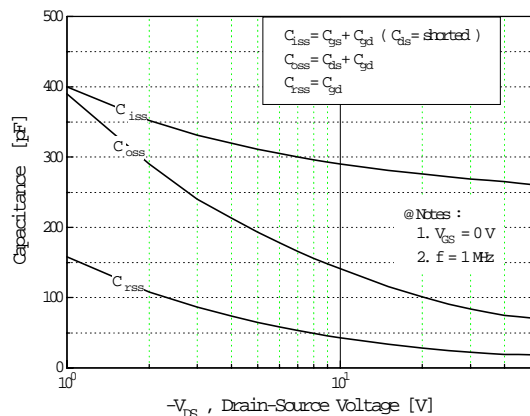
**Fig 3. On-Resistance vs. Drain Current**



**Fig 4. Source-Drain Diode Forward Voltage**



**Fig 5. Capacitance vs. Drain-Source Voltage**



**Fig 6. Gate Charge vs. Gate-Source Voltage**

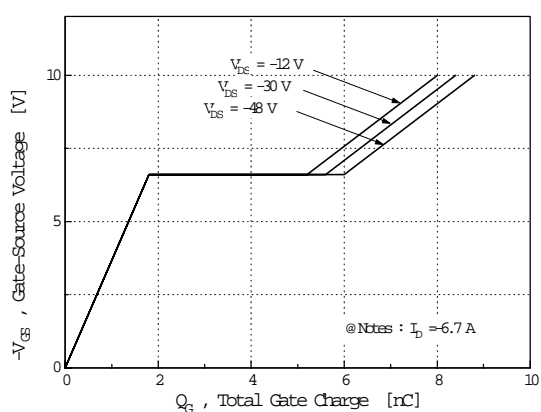


Fig 7. Breakdown Voltage vs. Temperature

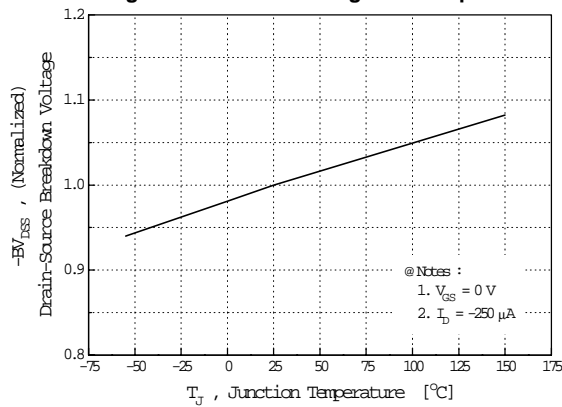


Fig 8. On-Resistance vs. Temperature

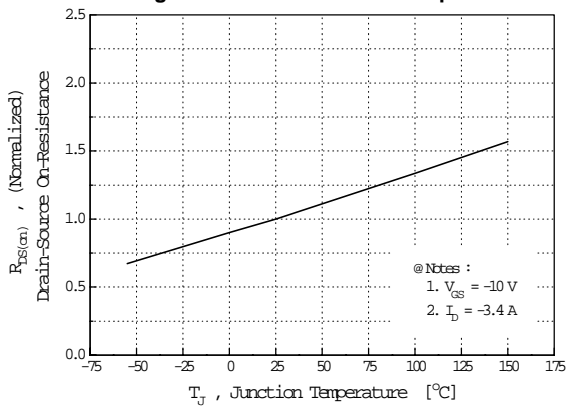


Fig 9. Max. Safe Operating Area

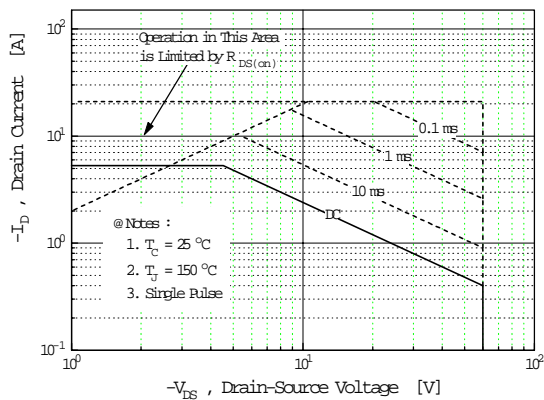


Fig 10. Max. Drain Current vs. Case Temperature

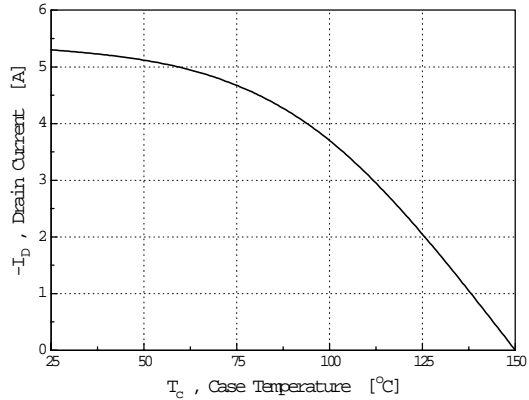
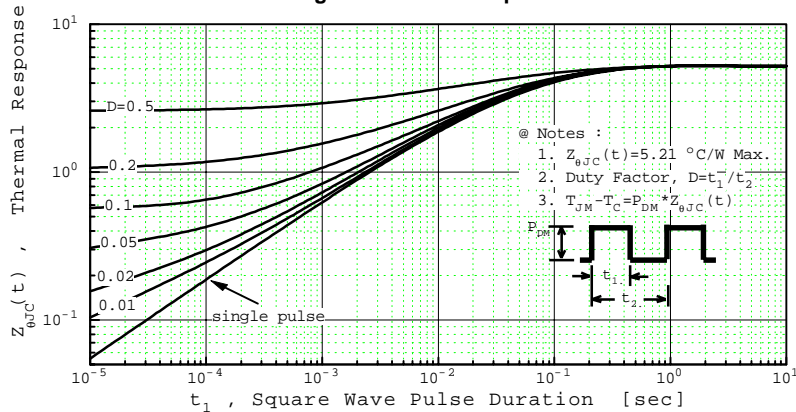
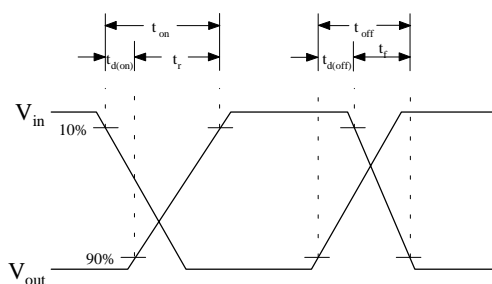
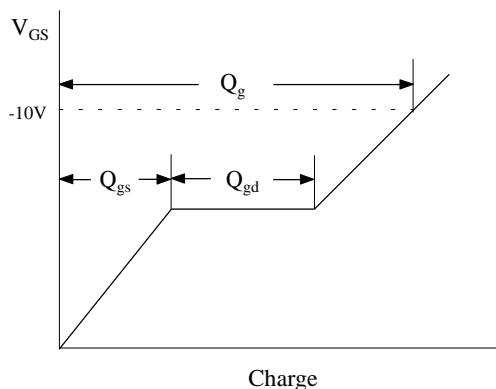


Fig 11. Thermal Response



The diagram shows a circuit for characterizing a Device Under Test (DUT). A 12V DC source is connected to a network of components: a 200nF capacitor, a 50KΩ resistor, and a 300nF capacitor. This network is connected to a MOSFET labeled "Current Regulator", which is noted to be of the "Same Type as DUT". The gate of this MOSFET is driven by a pulse source labeled  $-3mA$ . The drain of the "Current Regulator" MOSFET is connected to the gate of the DUT MOSFET, which is also labeled  $V_{GS}$ . The DUT MOSFET is of the same type as the first one. The drain of the DUT MOSFET is connected to a positive supply  $V_{DS}$  through a resistor  $R_2$ . The source of the DUT MOSFET is connected to ground through a resistor  $R_1$ . The current through  $R_1$  is labeled "Current Sampling ( $I_G$ ) Resistor", and the current through  $R_2$  is labeled "Current Sampling ( $I_D$ ) Resistor".



Vary  $t_p$  to obtain required peak  $I_D$

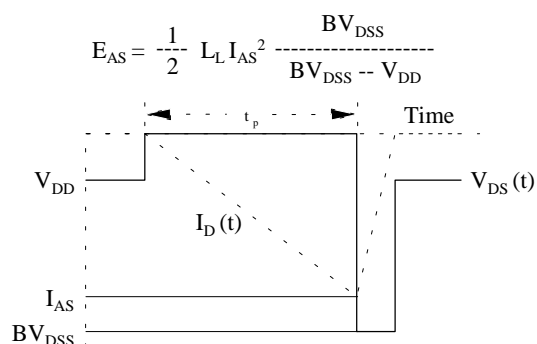
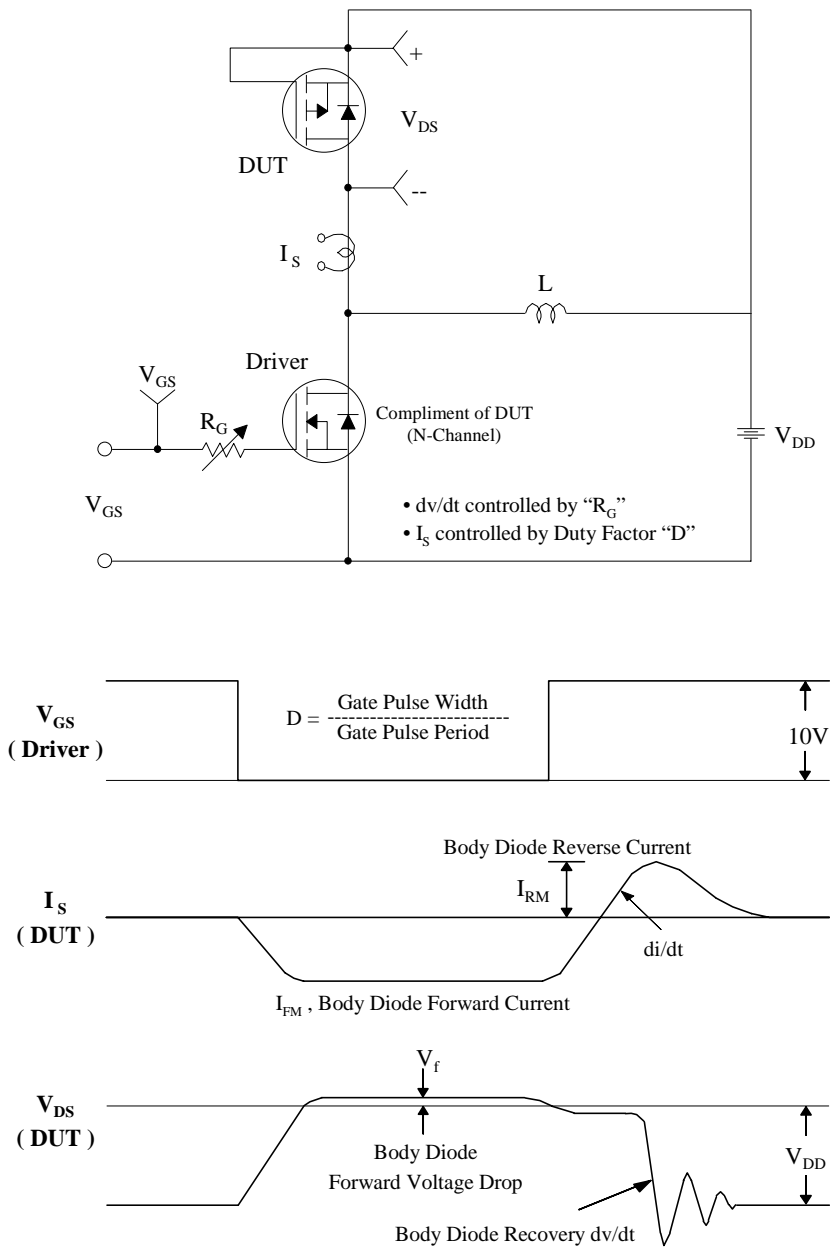


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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