M5M41000BP,J,L,VP,RV-7,-8,-10

FAST PAGE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 1-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of triple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the $\overline{RAS}$-only refresh mode, the hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

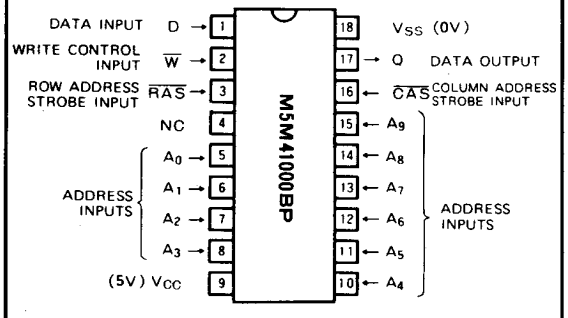
Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M41000B-7	70	20	35	140	230
M5M41000B-8	80	20	40	160	200
M5M41000B-10	100	25	50	190	175

- High performance CMOS technology
- Standard 18 pin DIP, 26 pin SOJ, 20 pin ZIP, 24 pin TSOP
- Single 5V±10% supply
- Low standby power dissipation
  2.75mW (Max) . . . . . CMOS Input level
- Low operating power dissipation
  M5M41000B-7 . . . . . 440mW (Max)
  M5M41000B-8 . . . . . 385mW (Max)
  M5M41000B-10 . . . . . 330mW (Max)
- Unlatched output enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-Modify-write, $\overline{RAS}$-only-Refresh, Fast-Page-Mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All inputs, output TTL compatible and low capacitance.
- 512 refresh cycles every 8ms
- $\overline{CAS}$ controlled output allows hidden refresh
- Wide $\overline{RAS}$ low pulse width for
  Fast-Page-Mode . . . . . 100μs Max

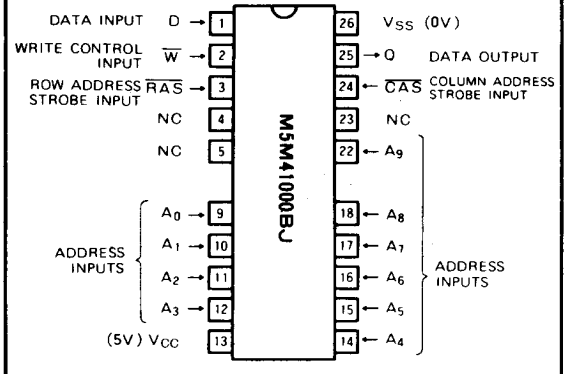
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

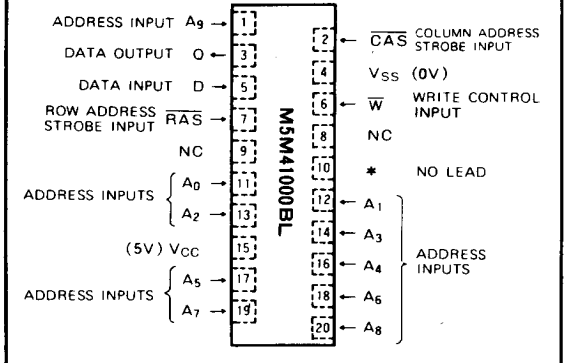
PIN CONFIGURATION (TOP VIEW)



Outline 18P4Y (DIP)



Outline 26P0J (SOJ)



Outline 20P5L-A(ZIP)

NC: NO CONNECTION

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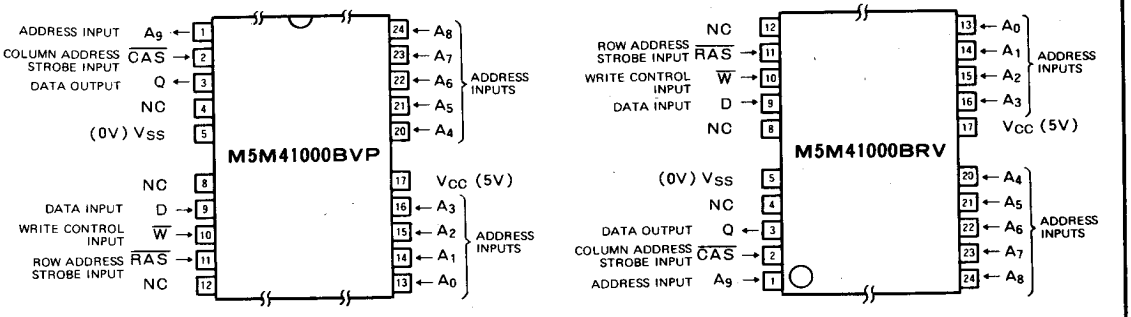
FAST PAGE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

PIN CONFIGURATION (TOP VIEW)



Outline 24P3B-C (TSOP)

Outline 24P3B-D (TSOP)

NC: NO CONNECTION

FUNCTION

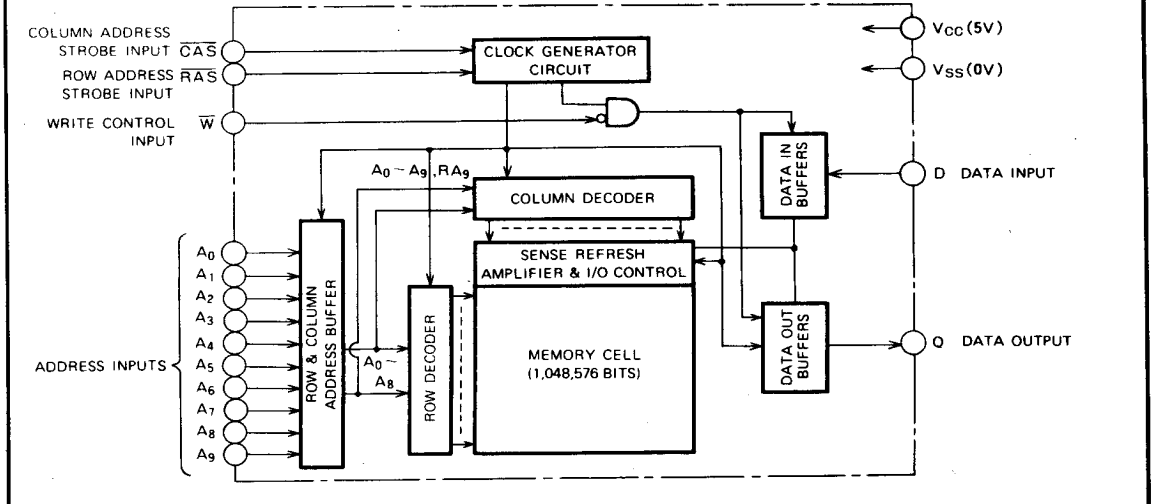
The M5M41000BP, J, L, VP, RV provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open

BLOCK DIAGRAM



FAST PAGE MODE 1048576-BIT(1048576-WORD BY 1-BIT)DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1～7	V
V_I	Input voltage		−1～7	V
V_O	Output voltage		−1～7	V
I_O	Output current		50	mA
P_d	Power dissipation	T_a = 25°C	1000	mW
T_{opr}	Operating temperature		0～70	°C
T_{stg}	Storage temperature		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−1.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (T_a = 0～70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current		0V ≦ V_{IN} ≦ 6.5, Other input pins = 0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	M5M41000B-7	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min, output open			80	mA
		M5M41000B-8				70	
		M5M41000B-10				60	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open			2	mA
			$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.5, output open			0.5	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	M5M41000B-7	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min, output open			80	mA
		M5M41000B-8				70	
		M5M41000B-10				60	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast page mode (Note 3, 4)	M5M41000B-7	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling t_{PC} = min, output open			70	mA
		M5M41000B-8				60	
		M5M41000B-10				50	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M41000B-7	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min, output open			80	mA
		M5M41000B-8				70	
		M5M41000B-10				60	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (T_a = 0～70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs (Note 5)	V_I = V_{SS} f = 1MHz V_I = 25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input				5	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
C_O	Output capacitance	V_O = V_{SS}, f = 1MHz, V_I = 25mVrms			7	pF

Note 5: $C_{I(A)}$ of ZIP is 6pF (max).

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SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V, unless otherwise noted) (Note 6)

Symbol	Parameter		Limits						Unit
			M5M41000B-7		M5M41000B-8		M5M41000B-10		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7, 8)		20		20		25	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7, 9)		70		80		100	ns
t_{CAA}	Column address access time	(Note 7, 10)		35		40		50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		40		45		55	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	20	0	20	0	25	ns

Note 6: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper devise operation is achieved.

7: Measured with a load circuit equivalent to 2TTL loads and 100pF.

8: Assume that $t_{RCD(max)} \leqq t_{RCD}$ and $t_{ASC} \geqq t_{ASC(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.

10: Assume that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assume that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OFF(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(T_a = 0 ~ 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V, unless otherwise noted, see notes 13, 14)

Symbol	Parameter		Limits						Unit
			M5M41000B-7		M5M41000B-8		M5M41000B-10		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ns
t_{RP}	$\overline{RAS}$ high pulse width		60		70		80		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	20	50	25	60	25	75	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 16)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 17)	15	35	20	40	20	50	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	10	0	15	0	20	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		15		15		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low or $\overline{W}$ low		15		20		20		ns
t_T	Transition time	(Note 19)	3	50	3	50	3	50	ns

Note 13: The timing requirements are assumed t_T = 5ns.

14: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

15: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA} as shown in notes 8, 10.

16: t_{CRP} requirement is applicable for all $\overline{RAS}$/$\overline{CAS}$ cycles.

17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAA}.

18: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M41000B-7		M5M41000B-8		M5M41000B-10		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		140		160		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width		70	10000	80	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		20		25		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time		35		40		50		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time		0		0		0		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle

Symbol	Parameter		Limits						Unit
			M5M41000B-7		M5M41000B-8		M5M41000B-10		
			Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time		140		160		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width		70	10000	80	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		20		25		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 23)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		15		15		20		ns
t_{WP}	Write pulse width		15		15		20		ns
t_{DS}	Data setup time		0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low		15		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M41000B-7		M5M41000B-8		M5M41000B-10		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read-Write cycle time (Note 21)	165		185		220		ns
t_{RMWC}	Read-Modify-Write cycle time (Note 22)	165		185		220		ns
t_{RAS}	$\overline{RAS}$ low pulse width	95	10000	105	10000	130	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	45	10000	45	10000	55	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	95		105		130		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	45		45		55		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to write low (Note 23)	20		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to write low (Note 23)	70		80		100		ns
t_{CWL}	$\overline{CAS}$ hold time after write low	20		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	20		20		25		ns
t_{WP}	Write pulse width	15		15		20		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after write low	15		15		20		ns
t_{AWD}	Delay time, address to write low (Note 23)	35		40		50		ns

Note 21: t_{RWC} is specified as $t_{RWC(min)} = t_{RCD(max)} + t_{CWD(min)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.
22: t_{RMWC} is specified as $t_{RMWC(min)} = t_{RAC(max)} + t_{RWL(min)} + t_{RP(min)} + 3t_T$.
23: t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} do not define the limits of operation, but are included as electrical characteristics only.
When $t_{WCS} \geqq t_{WCS(min)}$, an early-write cycle is performed, and the data output keeps the high-impedance state. When $t_{RWD} \geqq t_{RWD(min)}$, $t_{CWD} \geqq t_{CWD(min)}$ and $t_{AWD} \geqq t_{AWD(min)}$, a read-write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above condition is satisfied, the condition of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

Fast Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycles)

Symbol	Parameter	Limits						Unit
		M5M41000B-7		M5M41000B-8		M5M41000B-10		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast Page mode cycle time	45		50		60		ns
t_{RWPC}	Fast Page mode R/W, R/M/W cycle time	70		75		90		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read, write cycle	115	100000	130	100000	160	100000	ns
t_{CAS}	$\overline{CAS}$ low pulse width for read cycle	20	10000	20	10000	25	10000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 24)	10	25	10	25	10	25	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		20		25		ns

Note 24: $t_{CP(max)}$ is specified as a reference point only. If $t_{CP(max)} \leqq t_{CP}$, access time is assumed by t_{CAC}.

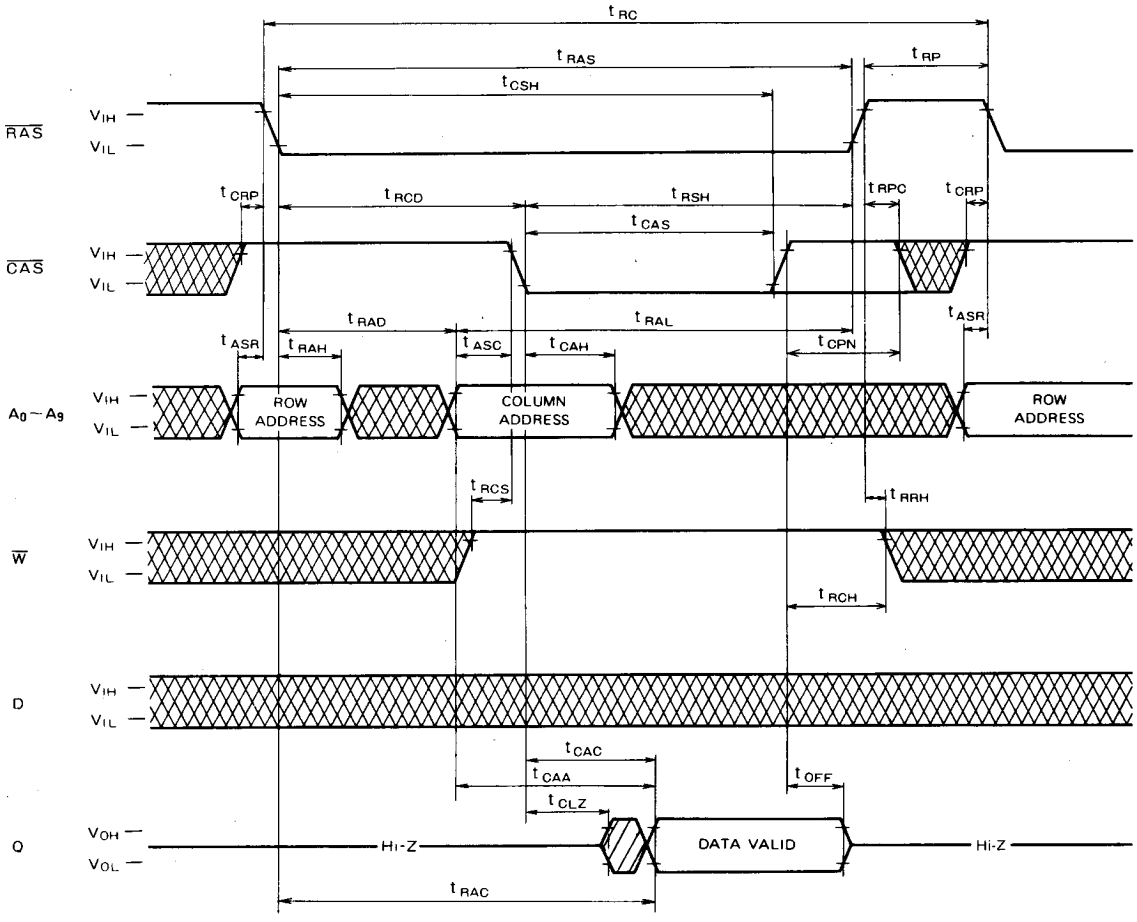
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 25)

Symbol	Parameter	Limits						Unit
		M5M41000B-7		M5M41000B-8		M5M41000B-10		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	15		15		20		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

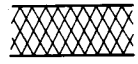
Note 25: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 26)

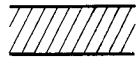
Read Cycle



Note 26



Indicates the don't care input.
$V_{IH(min)} \leqq V_{IN} \leqq V_{IH(max)}$ or $V_{IL(min)} \leqq V_{IN} \leqq V_{IL(max)}$



Indicates the invalid output.

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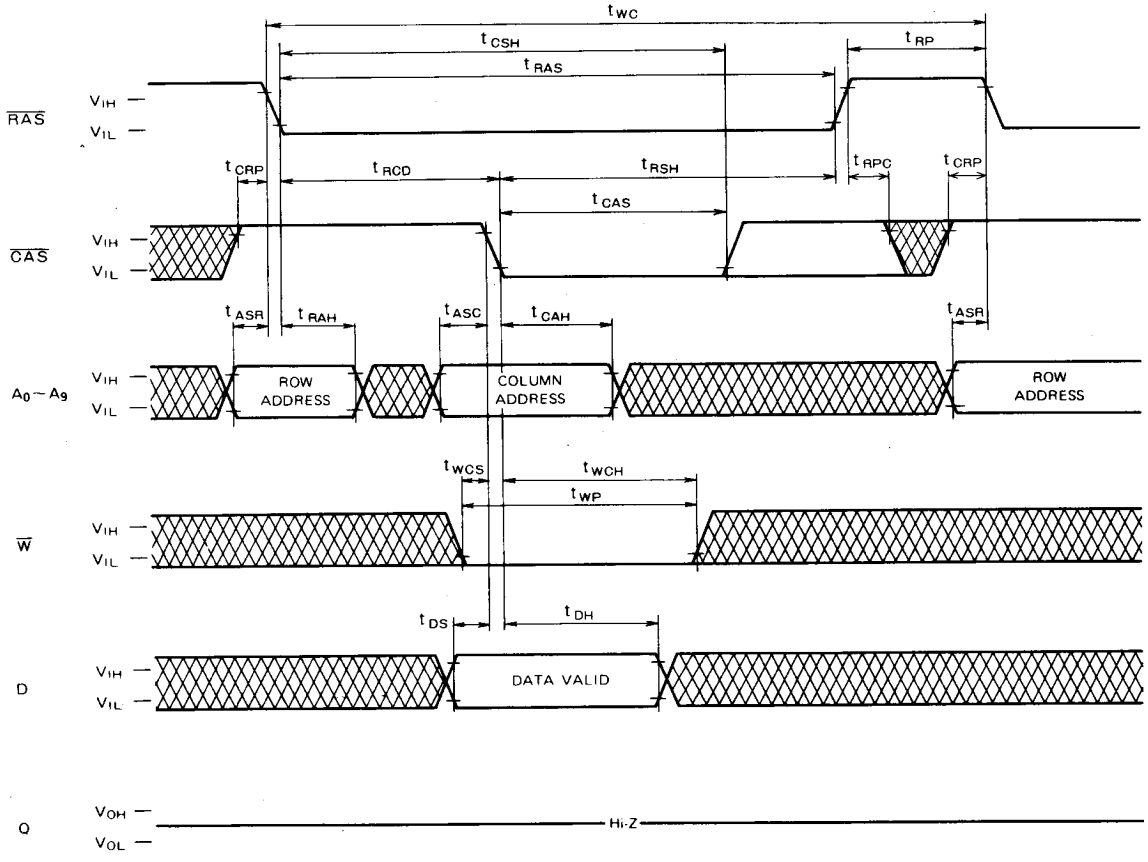
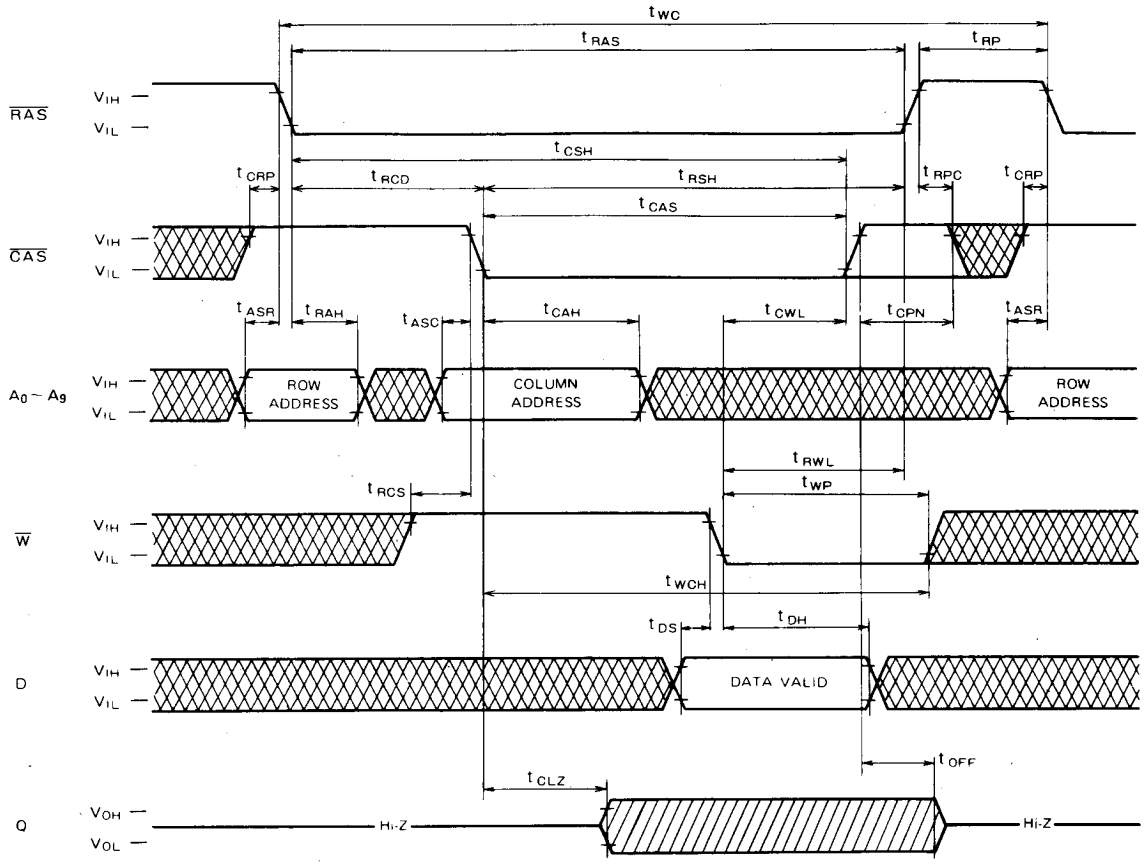
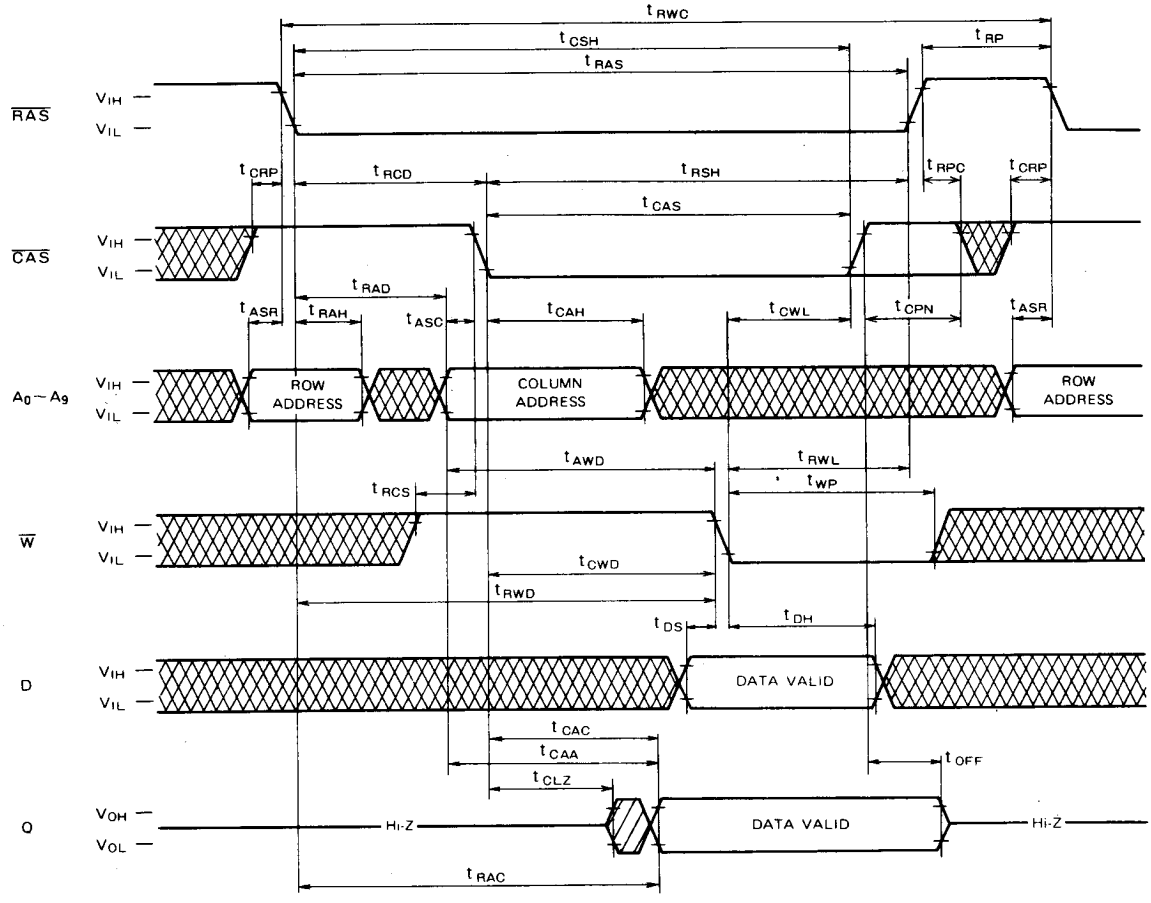
Write Cycle (Early write)



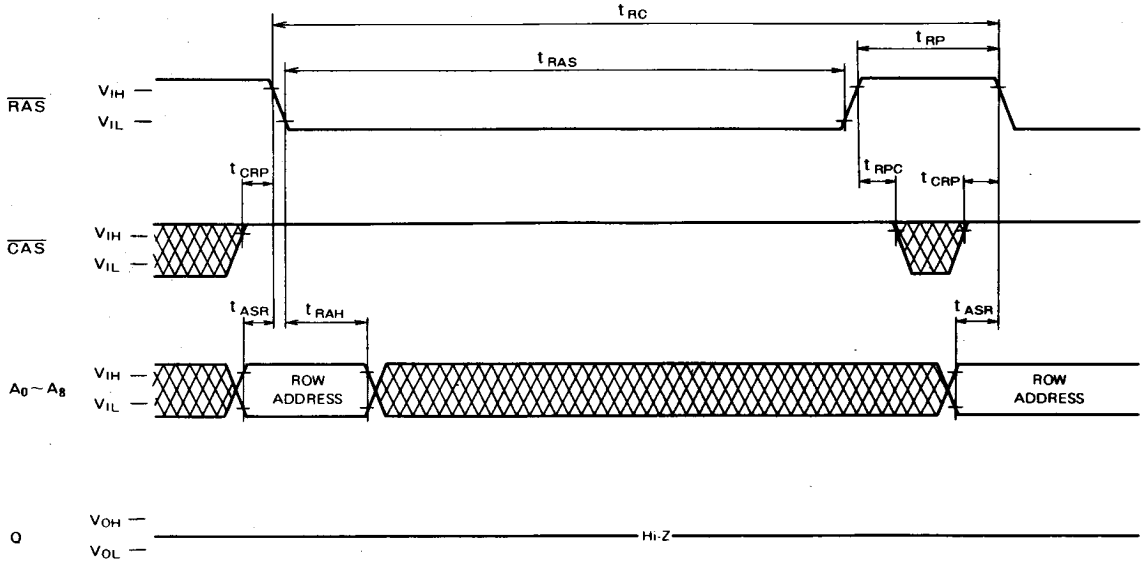
Write Cycle (Delayed Write)



Read-Write, Read-Modify-Write Cycle

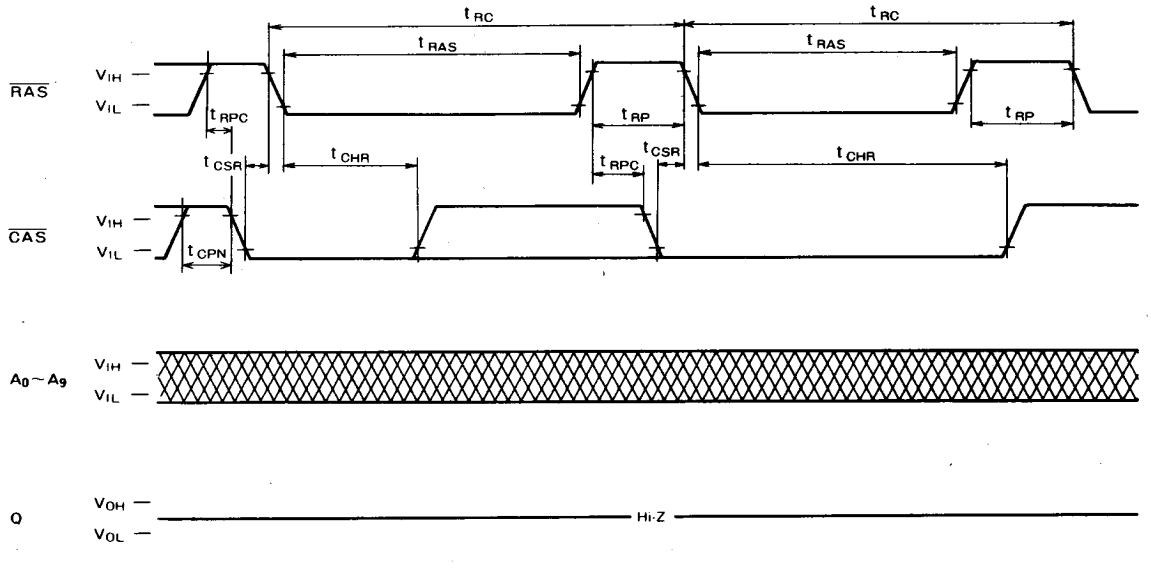


$\overline{RAS}$-only Refresh Cycle (Note 27)



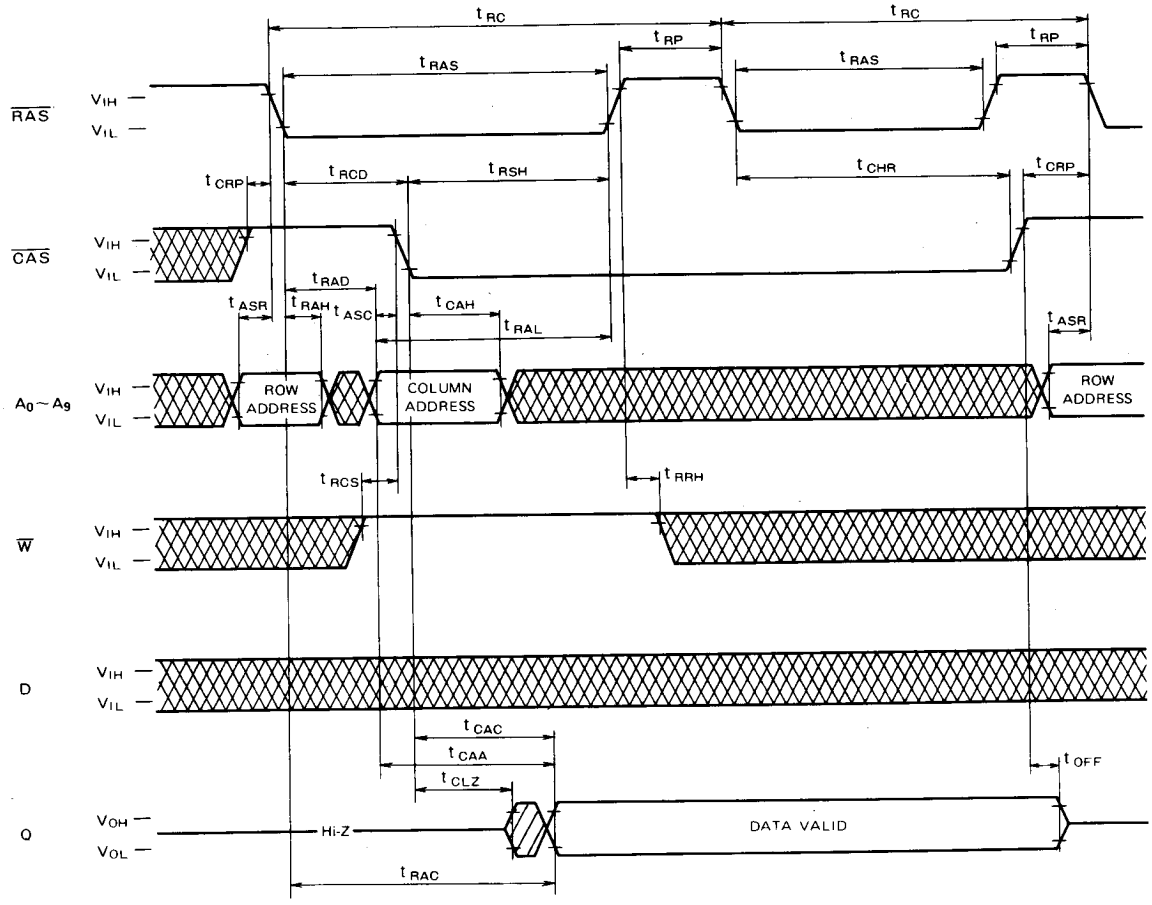
Note 27: $\overline{W}$, D = don't care, A_9 may be V_{IH} or V_{IL}

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)



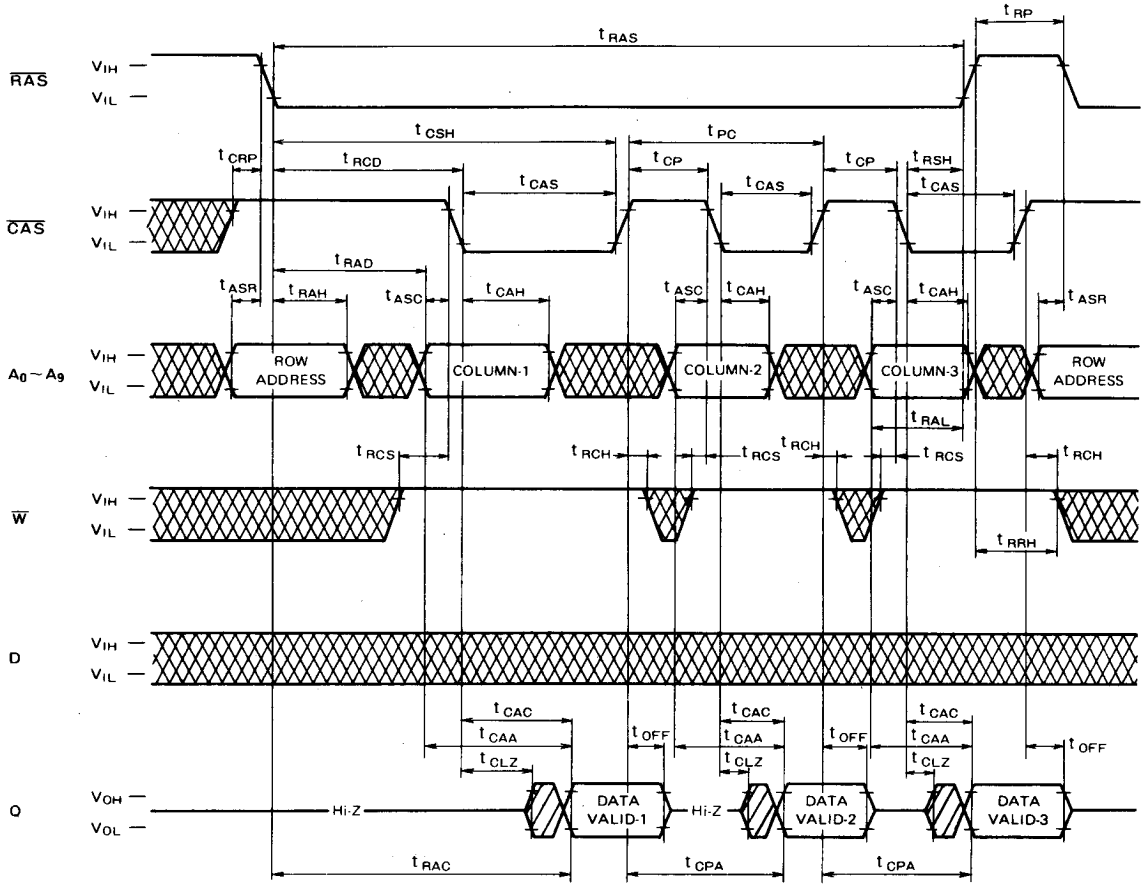
Note 28: $\overline{W}$, D = don't care

Hidden Refresh Cycle (Read) (Note 29)



Note 29: Early write, delayed write, read-write or read-modify-write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown before.

Fast-Page-Mode Read Cycle



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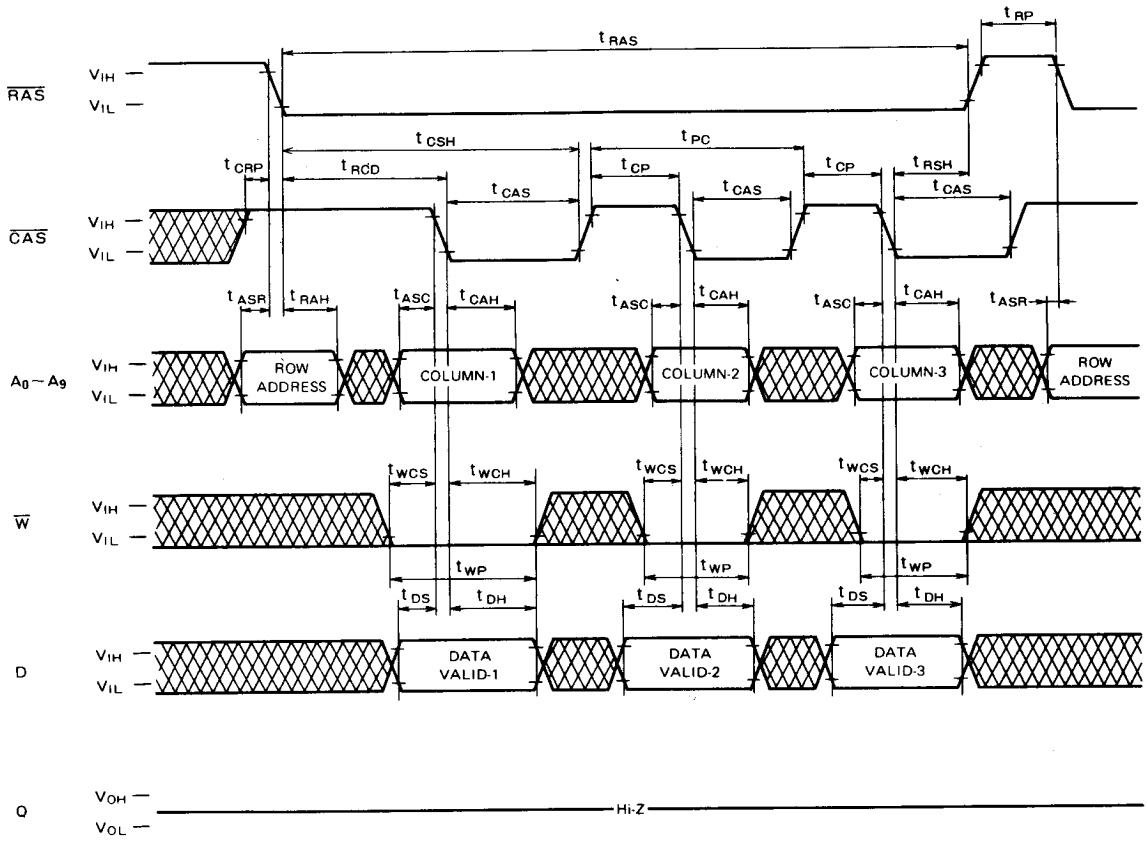
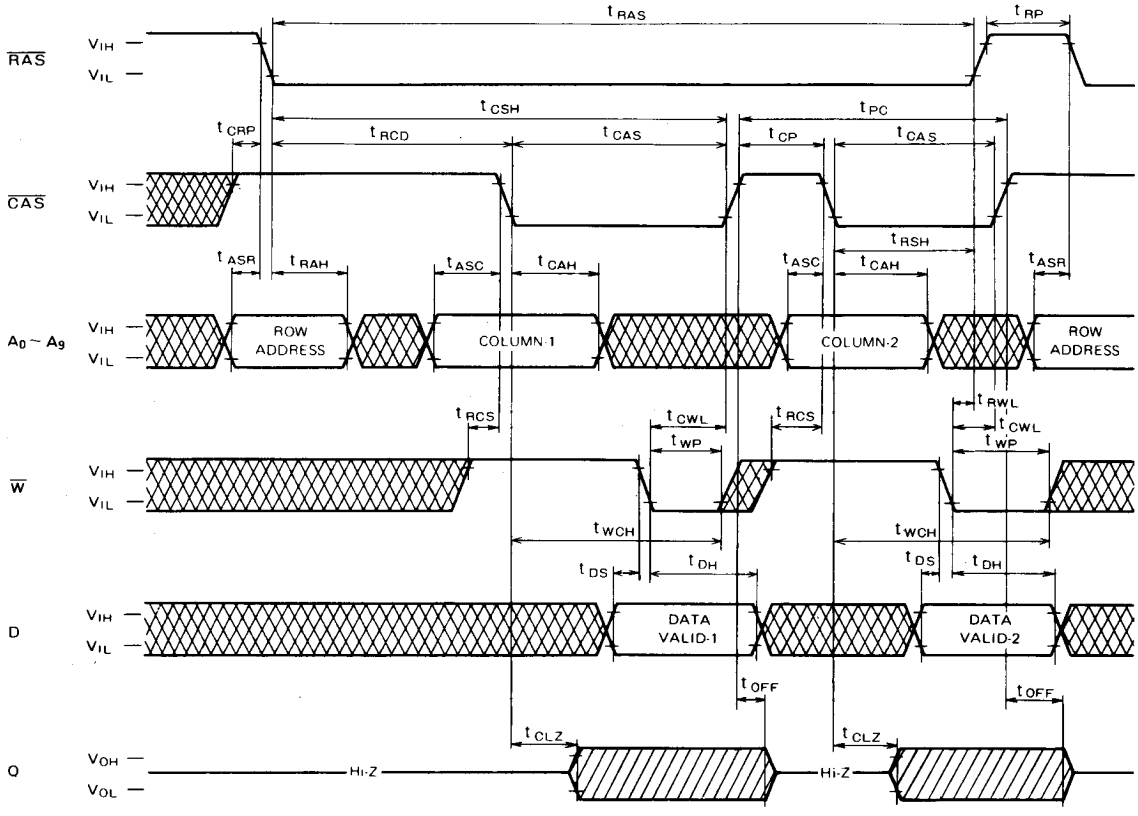
Fast-Page-Mode Early Write Cycle



Fast-Page-Mode Delayed Write Cycle



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Fast-Page-Mode Read-Write, Read-Modify-Write Cycle