ZiLOG

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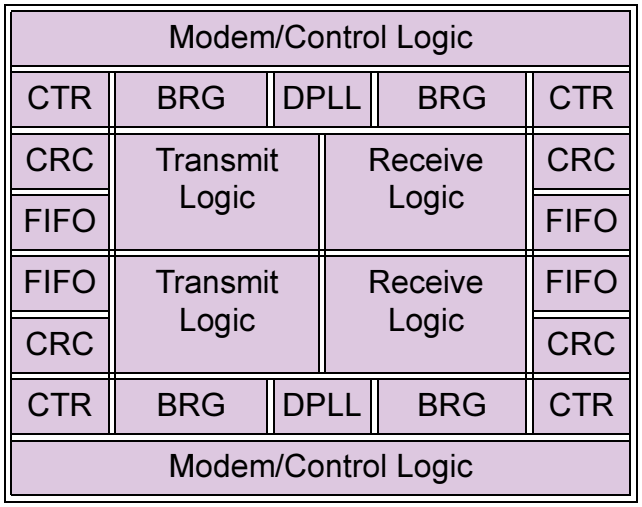
PB000301-0601

Z16C30

USC® Universal Serial Controller

Product Block Diagram



Features

- Two independent, 0 to 10 mbps, full-duplex channels, each with two baud-rate generators (BRGS) and one digital phase-locked loop (DPLL) for clock recovery
- 32-Byte Data FIFO's for each receiver and transmitter
- ASYNC mode with:
  - 1–8 bits/character; 1/16 to two stop bits/character in 1/16 bit increments
  - Programmable clock factor
  - Break detect and generation
  - Odd, Even, Mark, Space, or no parity and framing error detection
- Byte-oriented Synchronous mode with
  - 1–8 bits/character
  - 2- to 16-bit programmable SYNC character
  - 16- or 32-Bit cyclic redundancy check (CRC) and transmit-to-receive slaving (for X.21)
- HDLC/SDLC mode with:
  - 8-bit address compare
  - Extended address field option
  - 16- or 32-bit CRC
  - Programmable idle line condition
  - Optional preamble transmission and loop mode
- External character synchronous mode for receive
- DMA interface with separate request and acknowledge for each receiver and transmitter

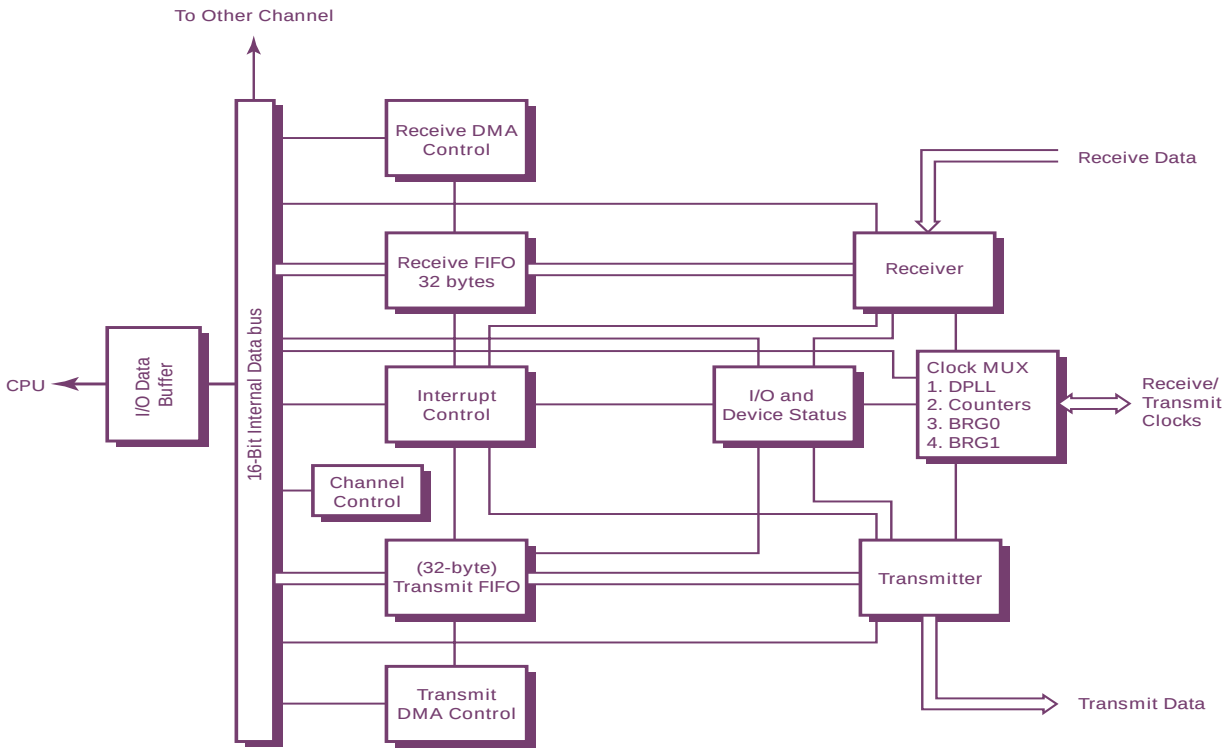
General Description

The Z16C30 USC, Universal Serial Controller is a dual-channel multi-protocol data communications peripheral. Designed for use with any conventional multiplexed or non-multiplexed bus, the USC functions as a serial-to-parallel, parallel-to-serial converter/controller, and may be software configured to satisfy a wide variety of serial communications applications. The device contains a variety of sophisticated internal functions, including two baud rate generators per channel, one digital phase-locked loop per channel, character counters for both receive and transmit in each channel, and 32-byte data FIFO's for each receiver and transmitter.

The CPU bus accesses have been shortened from 160 ns per access to 110 ns per access. The USC has a transmit and receive clock range of up to 10 MHz (20 MHz when using the DPLL, BRG, or CTR to divide the clock by 2 or more), and data transfer rates as high as 10 Mbps (full duplex).

The USC handles asynchronous formats, synchronous byte-oriented formats such as BISYNC, and synchronous bit-oriented formats such as HDLC.

The device generates and checks CRC in any synchronous mode and can be programmed to check data integrity in various modes. The USC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls may be used for general-purpose I/O. The same holds true for most of the other pins in each channel.



Interrupts are supported with a daisy-chain hierarchy, with the two channels having completely separate interrupt structures.

High-speed data transfers through DMA are supported by a Request/Acknowledge signal pair for each receiver and transmitter. The device supports automatic status transfer through DMA and device initialization under DMA control.

Applications and Support Tools

The following development tools are available for the programming and debug of this device:

- Z16C3001ZCO ISA Bus Evaluation Board
- Z8018600ZCO Evaluation Board

Related Products

Similar communication controllers available from ZiLOG's SCC family include:

Z8030 Z8530	NMOS SCC (Serial Communication Controller)
Z80C30 Z85C30	CMOS SCC (Serial Communication Controller)
Z16C35	ISCC Single Channel SCC with Built-in DMA Controllers
Z80230 Z85230	ESCC (Enhanced Serial Communication Controller)
Z16C32	IUSC Single Channel USC with Built-in DMA Controllers

Ordering Information

PSI	Description
Z16C3010ASC	100-pin VQFP USC Device
Z16C3010VSC	68-pin PLCC USC Device
Z16C3001ZCO	ISA Bus Evaluation Board
Z8018600ZCO	80186 Evaluation Board

To order, contact your nearest ZiLOG sales office or send an email to: csupport@zilog.com.

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