

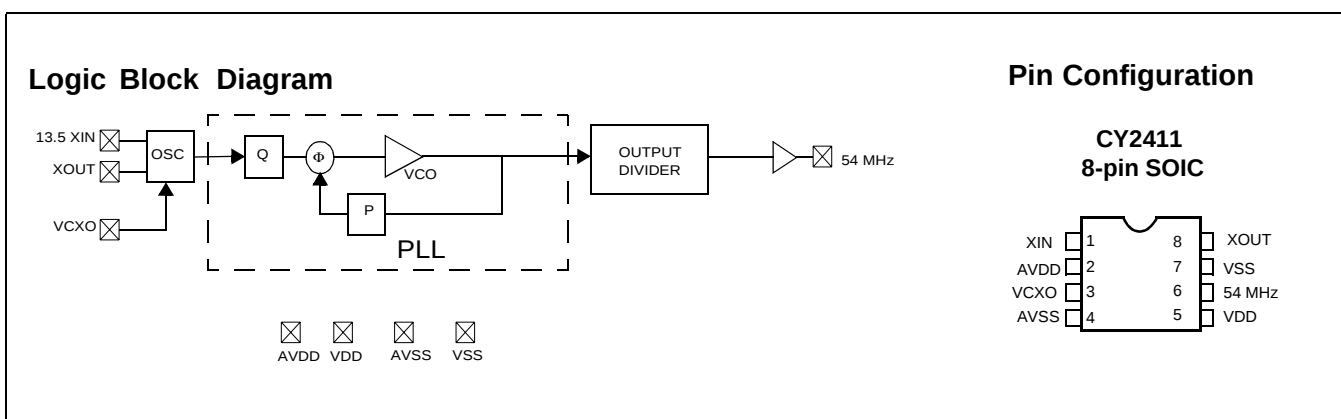


CY2411

MediaClock™ MPEG Clock Generator with VCXO

Features	Benefits
• Integrated phase-locked loop (PLL)	Highest-performance PLL tailored for multimedia applications
• Low-jitter, high-accuracy outputs	Meets critical timing requirements in complex system designs
• VCXO with analog adjust	Large ± 150 ppm range, better linearity
• 3.3V operation	

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY2411-1	1	13.5-MHz Pullable Crystal per Cypress Specification	1 copy of 54 MHz (3.3V)



Pin Summary

Pin Name	Pin Number	Pin Description
A_{VDD}	2	Analog Voltage Supply
V_{DD}	5	Output Voltage Supply
AV_{SS}	4	Analog Ground
V_{SS}	7	Output Ground
X_{IN}	1	Reference Crystal Input
V_{CXO}	3	Analog Control for V_{CXO}
$X_{OUT}^{[1]}$	8	Reference Crystal Output
54 MHz	6	54-MHz clock output

Note:

1. Float X_{OUT} if X_{IN} is externally driven.

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	-0.5	7.0	V
T_S	Storage Temperature ^[2]	-65	125	°C
T_J	Junction Temperature		125	°C
	Digital Inputs	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
	Digital Outputs Referred to V_{DD}	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
	Electro-Static Discharge	2000		V

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.15	3.3	3.45	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Max Load Capacitance			15	pF
f_{REF}	Reference Frequency	13.5	13.5	13.5	MHz

Pullable Crystal Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
CR_{load}	Crystal Load Capacitance		12.4		pF
C0/C1				240	
ESR	Equivalent Series Resistance		35	50	Ω
T_0	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Accuracy			± 20	ppm
TT_S	Stability over Temperature and Aging		± 20	± 50	ppm

DC Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.5$, $V_{DD} = 3.3$ V (source)	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3$ V (sink)	12	24		mA
C_{IN}	Input Capacitance				7	pF
I_{IZ}	Input Leakage Current			5		μ A
$f_{\Delta XO}$	V_{CXO} Pullability Range		-150		+150	ppm
V_{VCXO}	V_{CXO} Input Range		0		AV_{DD}	V
I_{DD}	Supply Current	$V_{DD} = 3.45$ V, $C_{load} = 15$ pF		15	20	mA

AC Electrical Characteristics ($V_{DD} = 3.3$ V)

Parameter ^[3]	Description	Conditions	Min.	Typ.	Max.	Unit
$DC = t_2/t_1$	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> , 50% of V_{DD}	45	50	55	%
ER_0	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} , $C_{load} = 15$ pF (see <i>Figure 2</i>)	0.8	1.4		V/ns
EF_0	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD} , $C_{load} = 15$ pF (see <i>Figure 2</i>)	0.8	1.4		V/ns
t_9	Clock Jitter	Peak to Peak period jitter			200	ps
t_{10}	PLL Lock Time				3	ms

Notes:

2. Rated for 10 years.
3. Not 100% tested.

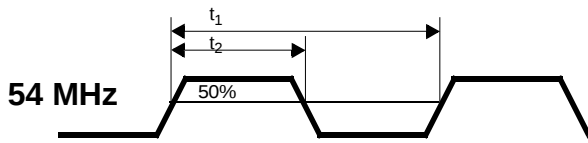


Figure 1. Duty Cycle Definition; $DC = t_2/t_1$

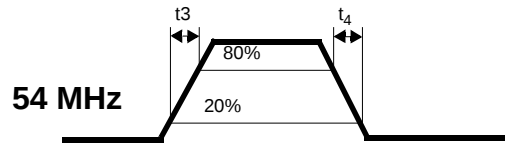
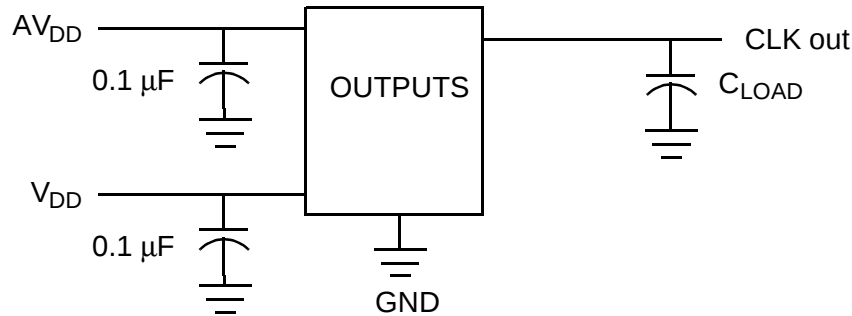


Figure 2. Rise and Fall Time Definitions:
 $ER = 0.6 \times V_{DD}/t_3$, $EF = 0.6 \times V_{DD}/t_4$

Test Circuit

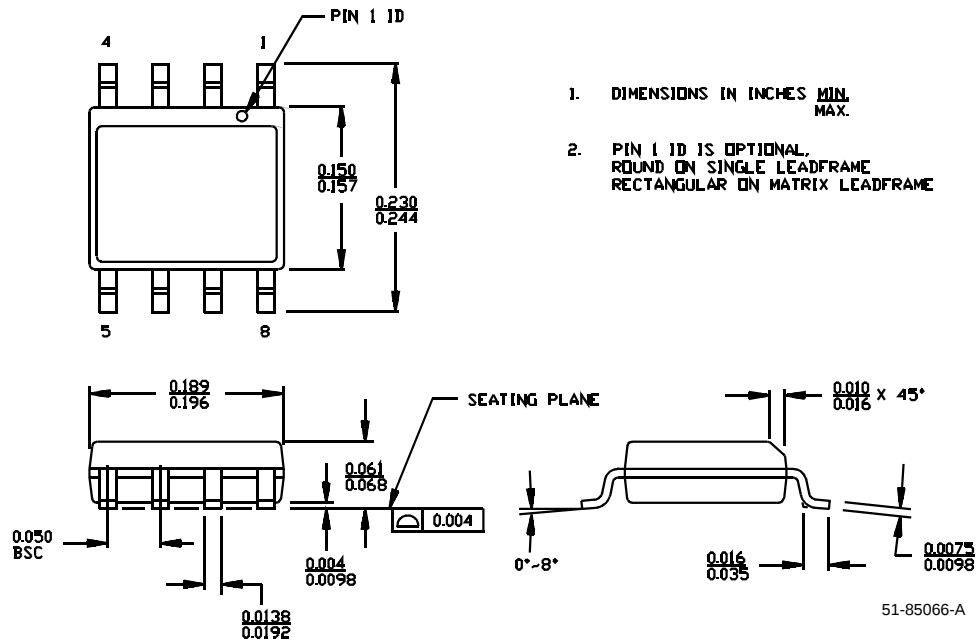


Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY2411SC-1	S8	8-pin SOIC	Commercial	3.3V
CY2411SC-1T	S8	8-pin SOIC—Tape and Reel	Commercial	3.3V

Pin Diagrams

8-lead (150-mil) SOIC S8



MediaClock is a trademark of Cypress Semiconductor. All product and company names mentioned in this document are the trademarks of their respective holders.

Document Title: CY2411 54-MHz MPEG Clock Generator with VCXO Document Number: 38-07193				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110594	11/07/01	DSG	Change from Spec number: 38-00957 to 38-07193
*A	111572	04/30/02	CKN	Changed title to "MPEG Clock Generator with VCXO" Added -1 data on pp. 1 and 3