

LM6118/LM6218 Fast Settling Dual Operational Amplifiers

General Description

The LM6118 series are monolithic fast-settling unity-gain-compensated dual operational amplifiers with ± 20 mA output drive capability. The PNP input stage has a typical bias current of 200 nA, and the operating supply voltage is ± 5 V to ± 20 V.

These dual op amps use slew enhancement with special mirror circuitry to achieve fast response and high gain with low total supply current.

The amplifiers are built on a junction-isolated VIP™ (Vertically Integrated PNP) process which produces fast PNP's that complement the standard NPN's.

Features

- Low offset voltage
- 0.01% settling time
- Slew rate $A_v = -1$
- Slew rate $A_v = +1$
- Gain bandwidth
- Total supply current
- Output drives 50Ω load (± 1 V)

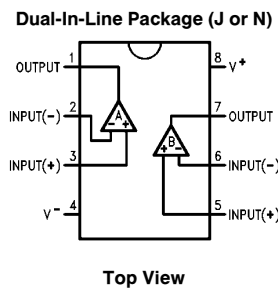
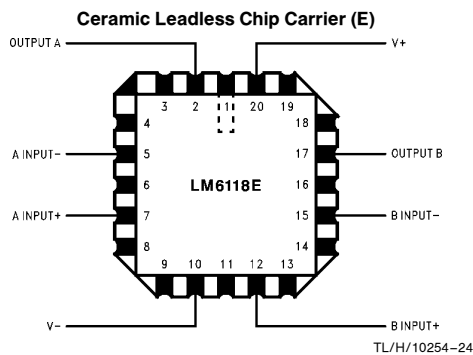
Typical

0.2 mV
400 ns
140 V/ μ s
75 V/ μ s
17 MHz
5.5 mA

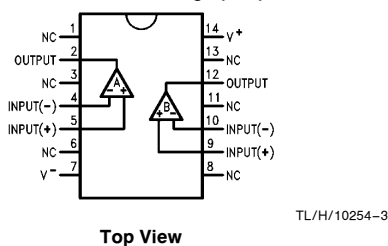
Applications

- D/A converters
- Fast integrators
- Active filters

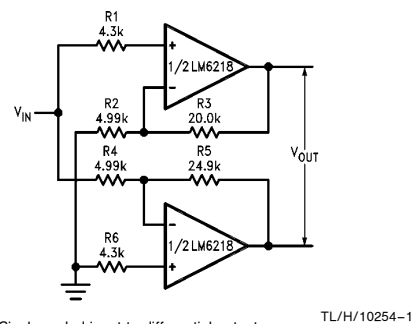
Connection Diagrams and Order Information



Small Outline Package (WM)



Typical Applications



*Available per SMD #5962-9156501

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	42V
Input Voltage	(Note 2)
Differential Input Current (Note 3)	± 10 mA
Output Current (Note 4)	Internally Limited
Power Dissipation (Note 5)	500 mW

ESD Tolerance (C = 100 pF, R = 1.5 kΩ)	± 2 kV
Junction Temperature	150°C
Storage Temperature Range	– 65°C to + 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Temp. Range

LM6118	– 55°C to + 125°C
LM6218A	– 40°C to + 85°C
LM6218	– 40°C to + 85°C

Electrical Characteristics $\pm 5V \leq V_S \leq \pm 20V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, $I_{OUT} = 0A$, unless otherwise specified. Limits with standard type face are for $T_J = 25^\circ C$, and **Bold Face Type** are for **Temperature Extremes**.

Parameter	Conditions	Typ 25°C	LM6118 Limits (Notes 6 & 7)	LM6218A Limits (Note 6)	LM6218 Limits (Note 6)	Units
Input Offset Voltage	$V_S = \pm 15V$	0.2	1 2	1 2	3 4	mV (max)
Input Offset Voltage	$V^- + 3V \leq V_{CM} \leq V^+ - 3.5V$	0.3	1.5 2.5	1.5 2.5	3.5 4.5	mV (max)
Input Offset Current	$V^- + 3V \leq V_{CM} \leq V^+ - 3.5V$	20	50 250	50 100	100 200	nA (max)
Input Bias Current	$V^- + 3V \leq V_{CM} \leq V^+ - 3.5V$	200	350 950	350 950	500 1250	nA (max)
Input Common Mode Rejection Ratio	$V^- + 3V \leq V_{CM} \leq V^+ - 3.5V$ $V_S = \pm 20V$	100	90 85	90 85	80 75	dB (min)
Positive Power Supply Rejection Ratio	$V^- = -15V$ $5V \leq V^+ \leq 20V$	100	90 85	90 85	80 75	dB (min)
Negative Power Supply Rejection Ratio	$V^+ = 15V$ $-20V \leq V^- \leq -5V$	100	90 85	90 85	80 75	dB (min)
Large Signal Voltage Gain	$V_{out} = \pm 15V$ $R_L = 10k$ $V_S = \pm 20V$	500	150 100	150 100	100 70	V/mV (min)
	$V_{out} = \pm 10V$ $R_L = 500$ $V_S = \pm 15V$ (± 20 mA)	200	50 30	50 30	40 25	V/mV (min)
V_O Output Voltage Swing	Supply = $\pm 20V$ $R_L = 10k$	17.3	± 17	± 17	± 17	V (min)
Total Supply Current	$V_S = \pm 15V$	5.5	7 7.5	7 7.5	7 7.5	mA (max)
Output Current Limit	$V_S = \pm 15V$, Pulsed	65	100	100	100	mA (max)
Slew Rate, $A_v = -1$	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF	140	100 50	100 50	100 50	V/μs (min)
Slew Rate, $A_v = +1$	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF	75	50 30	50 30	50 30	V/μs (min)
Gain-Bandwidth Product	$V_S = \pm 15V$, $f_o = 200$ kHz	17	14	14	13	MHz (min)
0.01% Settling Time $A_v = -1$	$\Delta V_{out} = 10V$, $V_S = \pm 15V$, $R_S = R_f = 2k$, $C_f = 10$ pF	400				ns
Input Capacitance	Inverter	5				pF
	Follower	3				pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage range is ($V^+ - 1V$) to (V^-).

Note 3: The inputs are shunted with three series-connected diodes back-to-back for input differential clamping. Therefore differential input voltages greater than about 1.8V will cause excessive current to flow unless limited to less than 10 mA.

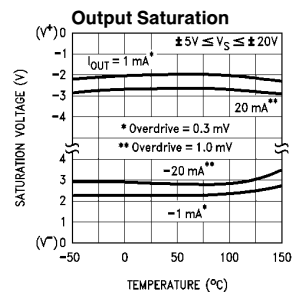
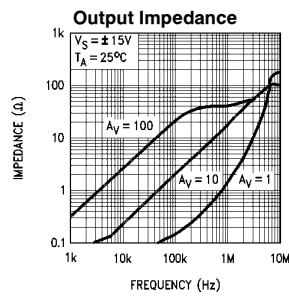
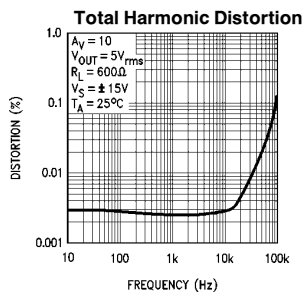
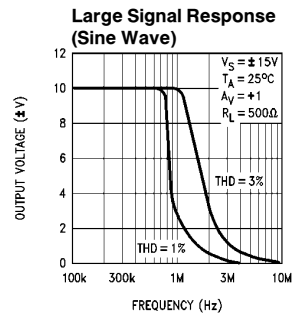
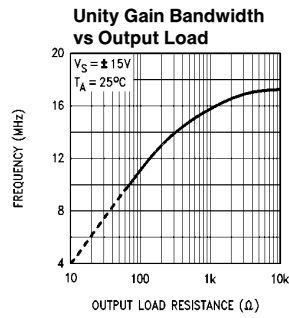
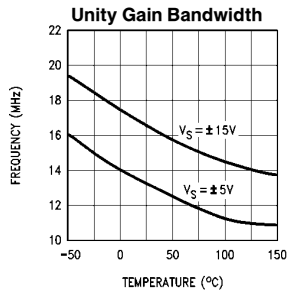
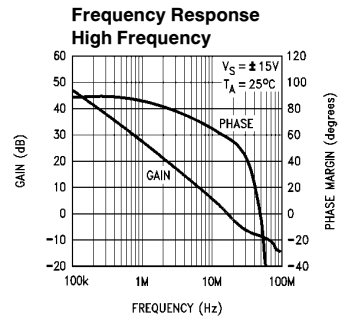
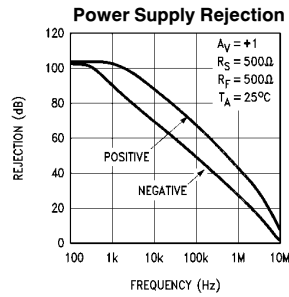
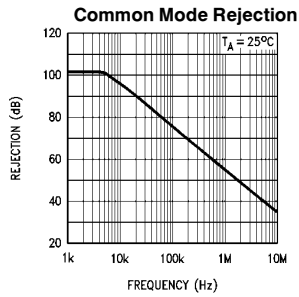
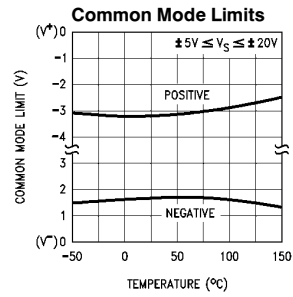
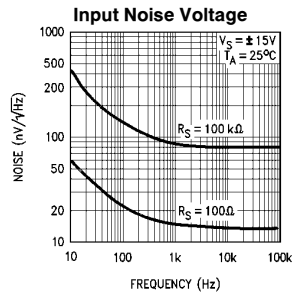
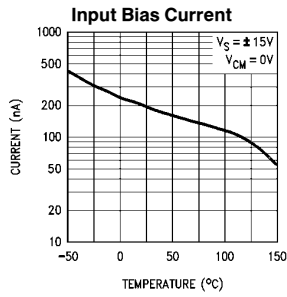
Note 4: Current limiting protects the output from a short to ground or any voltage less than the supplies. With a continuous overload, the package dissipation must be taken into account and heat sinking provided when necessary.

Note 5: Devices must be derated using a thermal resistance of 90°C/W for the N, J and WM packages.

Note 6: Limits are guaranteed by testing or correlation.

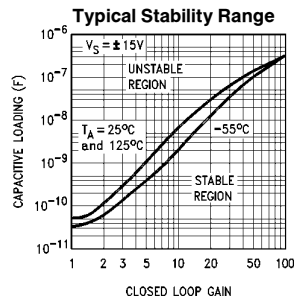
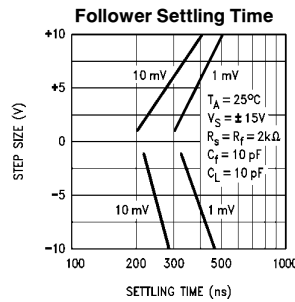
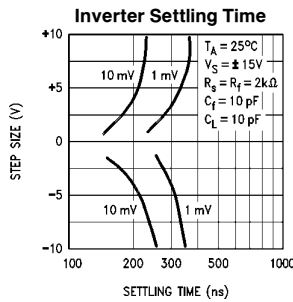
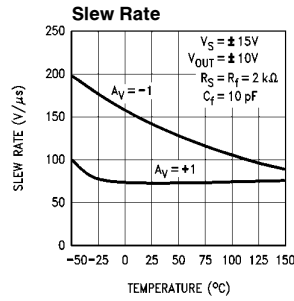
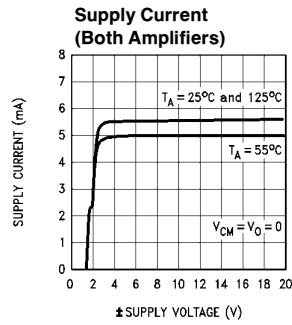
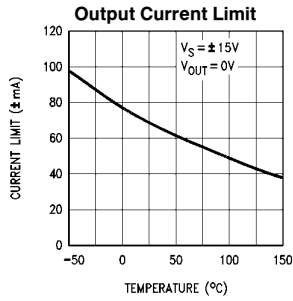
Note 7: A military RETS specification is available on request. At the time of printing, LM6118J/883 and LM6118E/883 RETS spec complied with the **Boldface** limits in this column.

Typical Performance Characteristics

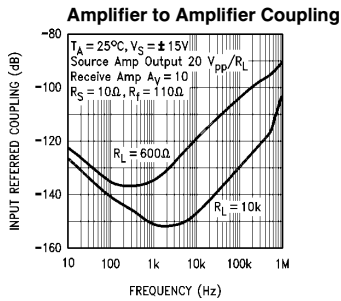


TL/H/10254-5

Typical Performance Characteristics (Continued)

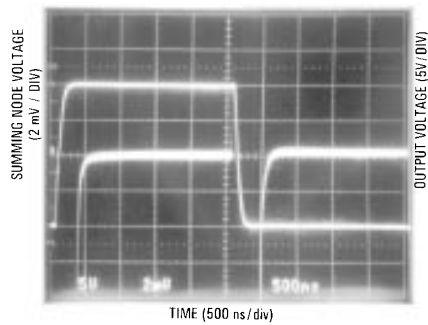


TL/H/10254-6



TL/H/10254-23

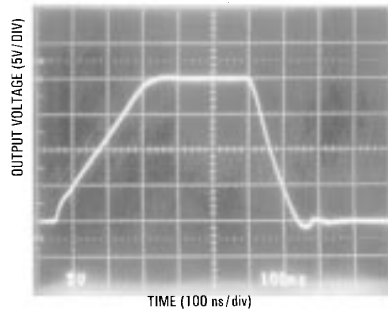
Settling Time, $V_S = \pm 15V$



TL/H/10254-7

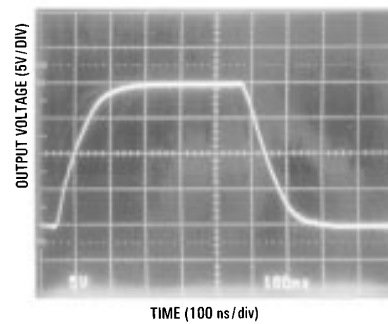
Typical Performance Characteristics (Continued)

Step Response, $A_v = +1$, $V_s = \pm 15V$



TL/H/10254-8

Step Response, $A_v = -1$, $V_s = \pm 15V$



TL/H/10254-9

Application Information

General

The LM6118 series are high-speed, fast-settling dual op-amps. To insure maximum performance, circuit board layout is very important. Minimizing stray capacitance at the inputs and reducing coupling between the amplifier's input and output will minimize problems.

Supply Bypassing

To assure stability, it is recommended that each power supply pin be bypassed with a 0.1 μF low inductance capacitor near the device. If high frequency spikes from digital circuits or switching supplies are present, additional filtering is recommended. To prevent these spikes from appearing at the output, R-C filtering of the supplies near the device may be necessary.

Power Dissipation

These amplifiers are specified to 20 mA output current. If accompanied with high supply voltages, relatively high power dissipation in the device will occur, resulting in high junction temperatures. In these cases the package thermal resistance must be taken into consideration. (See Note 5 under Electrical Characteristics.) For high dissipation, an N package with large areas of copper on the pc board is recommended.

Amplifier Shut Down

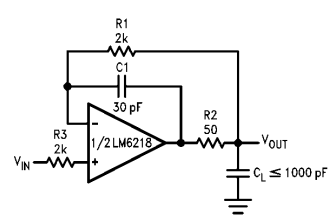
If one of the amplifiers is not used, it can be shut down by connecting both the inverting and non-inverting inputs to the V^- pin. This will reduce the power supply current by approximately 25%.

Capacitive Loading

Maximum capacitive loading is about 50 pF for a closed-loop gain of +1, before the amplifier exhibits excessive ringing and becomes unstable. A curve showing maximum capacitive loads, with different closed-loop gains, is shown in the Typical Performance Characteristics section.

To drive larger capacitive loads at low closed-loop gains, isolate the amplifier output from the capacitive load with 50 Ω . Connect a small capacitor directly from the amplifier output to the inverting input. The feedback loop is closed from the isolated output with a series resistor to the inverting input.

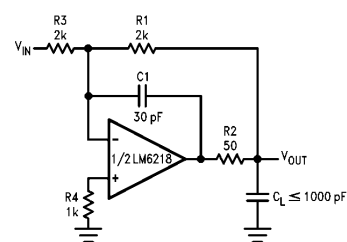
Voltage Follower



TL/H/10254-10

For $C_L = 1000$ pF, Small signal BW = 5 MHz
20 V_{p-p} BW = 500 kHz

Inverter



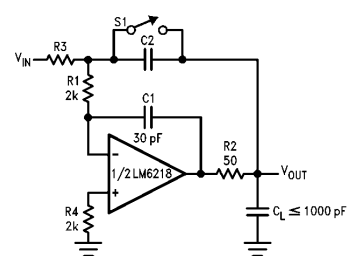
TL/H/10254-11

Settling time to 0.01%, 10V Step

For $C_L = 1000$ pF, settling time ≈ 1500 ns

For $C_L = 300$ pF, settling time ≈ 500 ns

Integrator



TL/H/10254-12

Application Information (Continued)

Examples of unity gain connections for a voltage follower, inverter, and integrator driving capacitive loads up to 1000 pF are shown here. Different R1–C1 time constants and capacitive loads will have an effect on settling times.

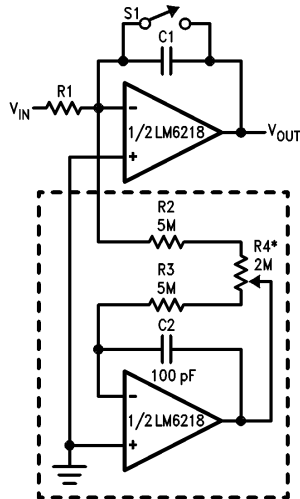
Input Bias Current Compensation

Input bias current of the first op amp can be reduced or balanced out by the second op amp. Both amplifiers are laid out in mirror image fashion and in close proximity to each other, thus both input bias currents will be nearly identical

and will track with temperature. With both op amp inputs at the same potential, a second op amp can be used to convert bias current to voltage, and then back to current feeding the first op amp using large value resistors to reduce the bias current to the level of the offset current.

Examples are shown here for an inverting application, (a) where the inputs are at ground potential, and a second circuit (b) for compensating bias currents for both inputs.

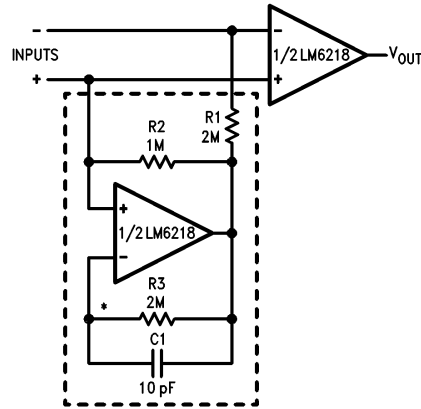
Bias Current Compensation



*adjust for zero integrator drift

TL/H/10254–13

(a) Inverting Input Bias Compensation for Integrator Application

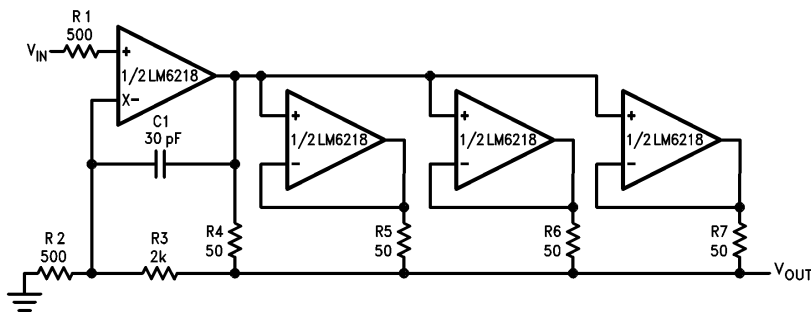


TL/H/10254–14

*mount resistor close to input pin to minimize stray capacitance

(b) Compensation to Both Inputs

Amplifier/Parallel Buffer



TL/H/10254–15

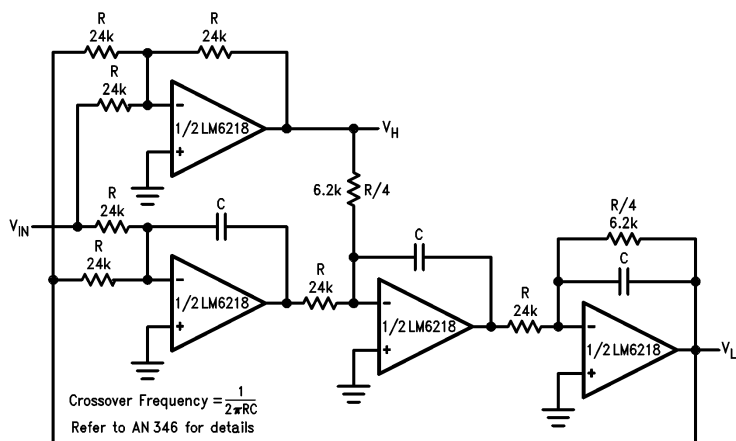
$A_V = +5$, $I_{OUT} \leq 80$ mA

$V_S = \pm 15$ V, $C_L \leq 0.01$ μ F

Large and small signal B.W. = 1.3 MHz (THD = 3%)

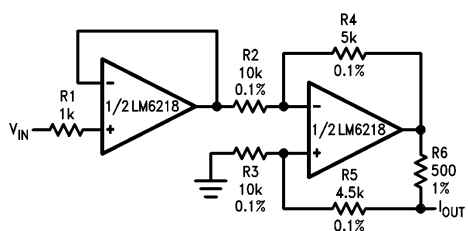
Application Information (Continued)

Constant-Voltage Crossover Network With 12 dB/Octave Slope



TL/H/10254-16

Bilateral Current Source



TL/H/10254-17

$$V_S = \pm 15V, -10 \leq V_{IN} \leq 10V$$

$$\frac{I_{OUT}}{V_{IN}} = \frac{R_4}{R_2 R_6} = \frac{1}{1V} \text{ mA}$$

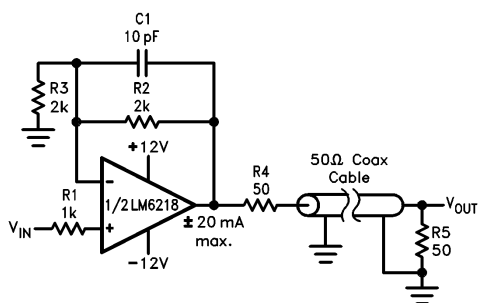
$$\text{Output dynamic range} = 10V - R_6 |I_{OUT}|$$

$$R_L = 500\Omega, \text{ small signal BW} = 6 \text{ MHz}$$

$$\text{Large signal response} = 800 \text{ kHz}$$

$$C_{out \text{ equiv.}} = \frac{R_2 + R_4}{2\pi f_O R_2 R_6} = 32 \text{ pF} (f_O = 15 \text{ MHz})$$

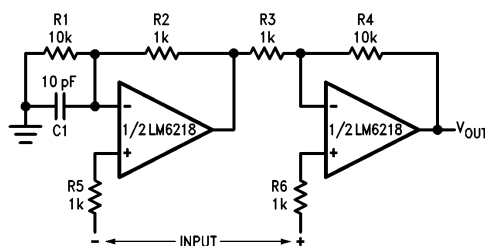
Coaxial Cable Driver



TL/H/10254-19

Small signal (200 mV_{p-p}) BW ≈ 5 MHz

Instrumentation Amplifier

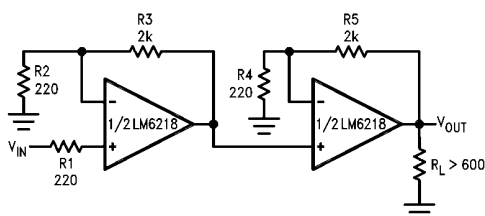


TL/H/10254-18

$$A_V = 10, V_S = \pm 15V, \text{ All resistors } 0.01\%$$

$$\text{Small signal and large signal (20 V}_{p-p}\text{) B.W.} \approx 800 \text{ kHz}$$

150 MHz Gain-Bandwidth Amplifier



TL/H/10254-20

$$A_V = 100, V_S = \pm 15V,$$

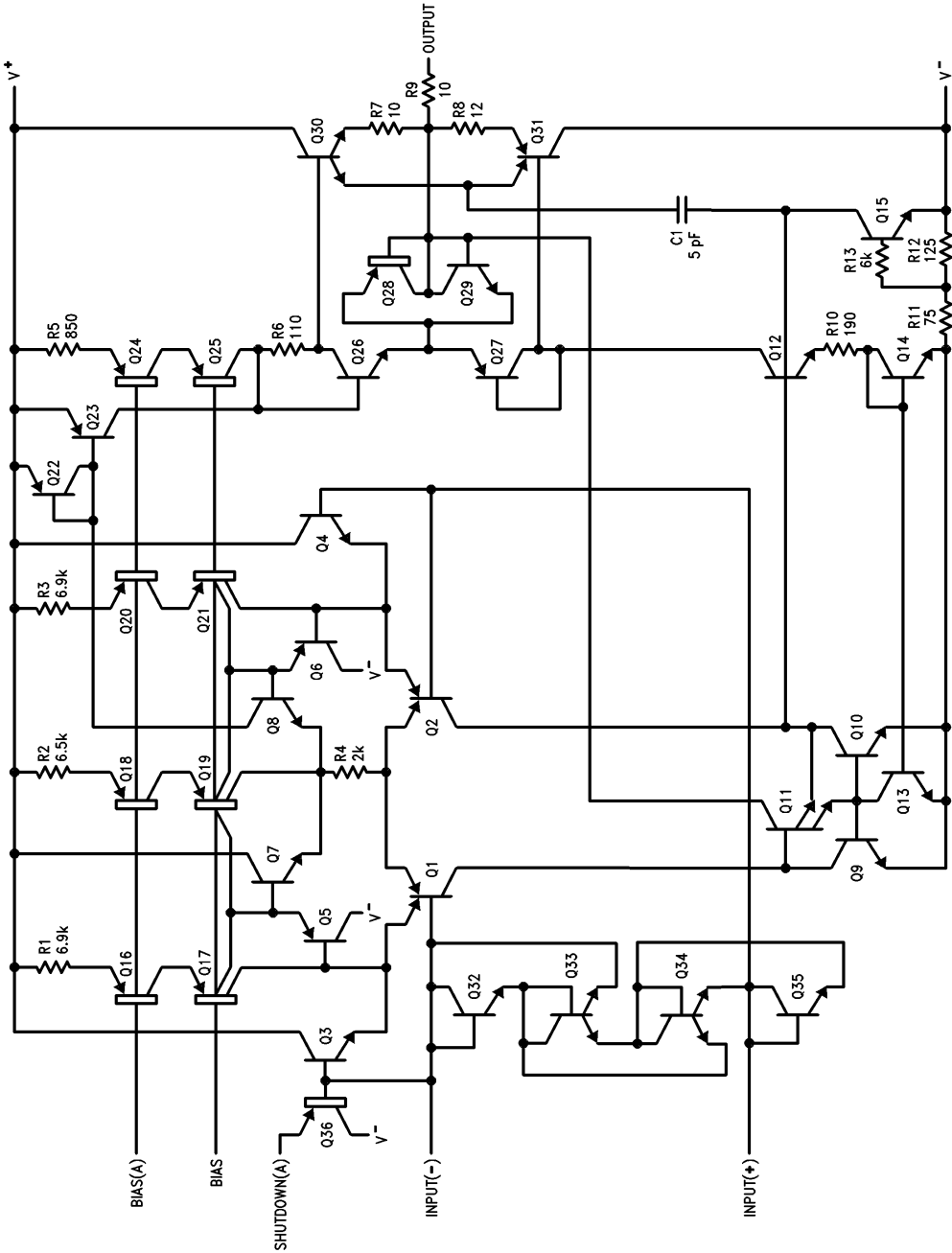
$$\text{Small signal BW} \approx 1.5 \text{ MHz}$$

$$\text{Large signal BW (20 V}_{p-p}\text{) } \approx 800 \text{ kHz}$$

Schematic Diagram

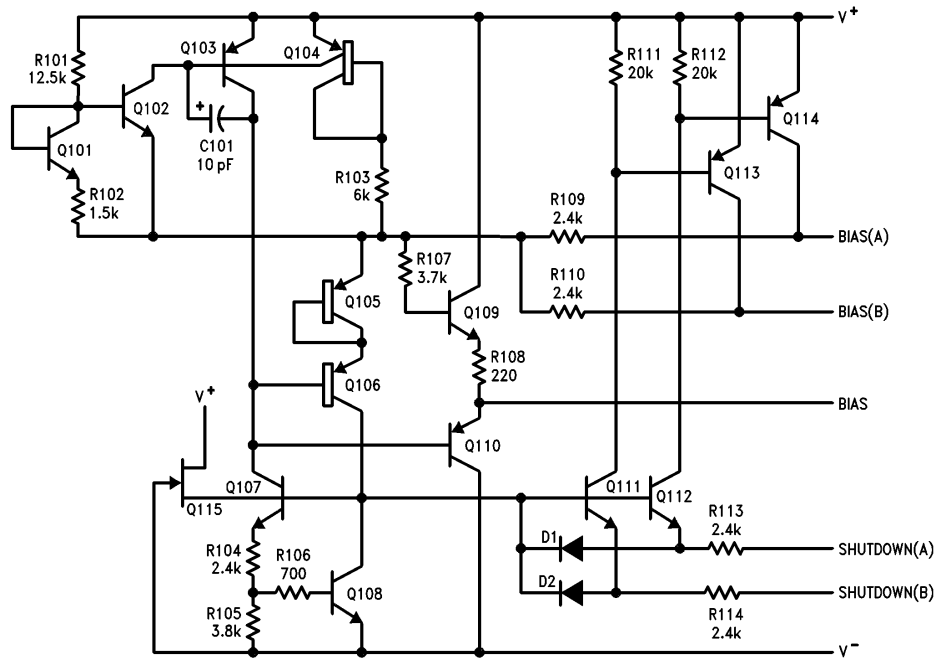
1/2 LM6118 (Op Amp A)

TL/H/10254-21



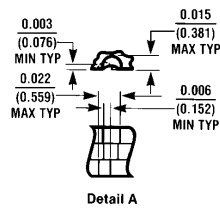
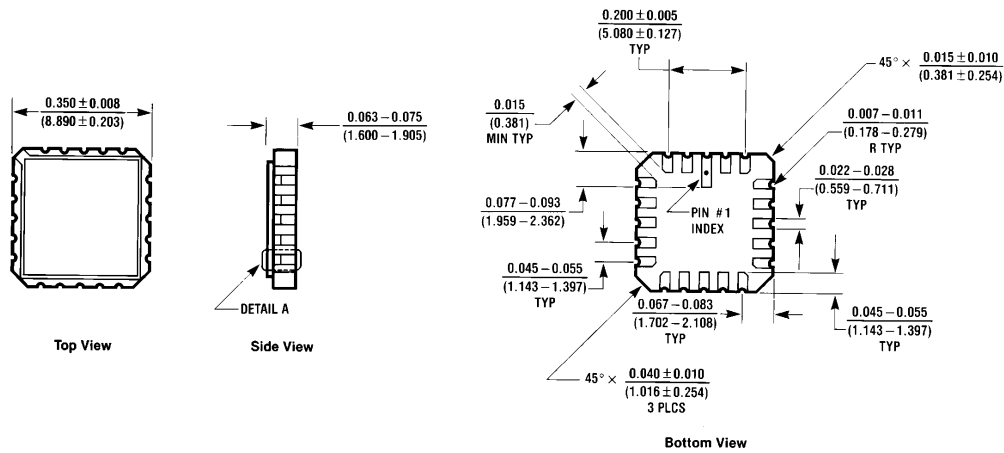
Schematic Diagram (Continued)

Bias Circuit



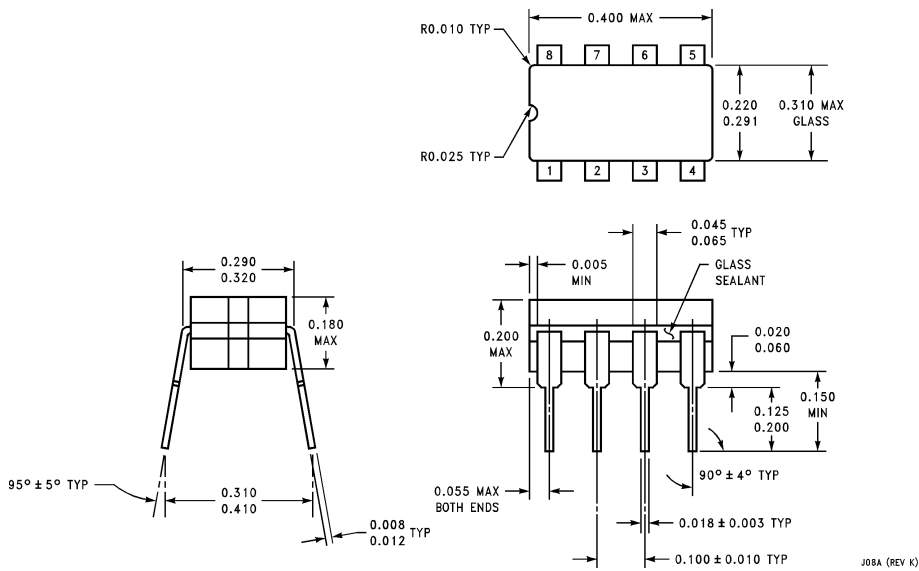
TL/H/10254-22

Physical Dimensions inches (millimeters)



E20A (REV D)

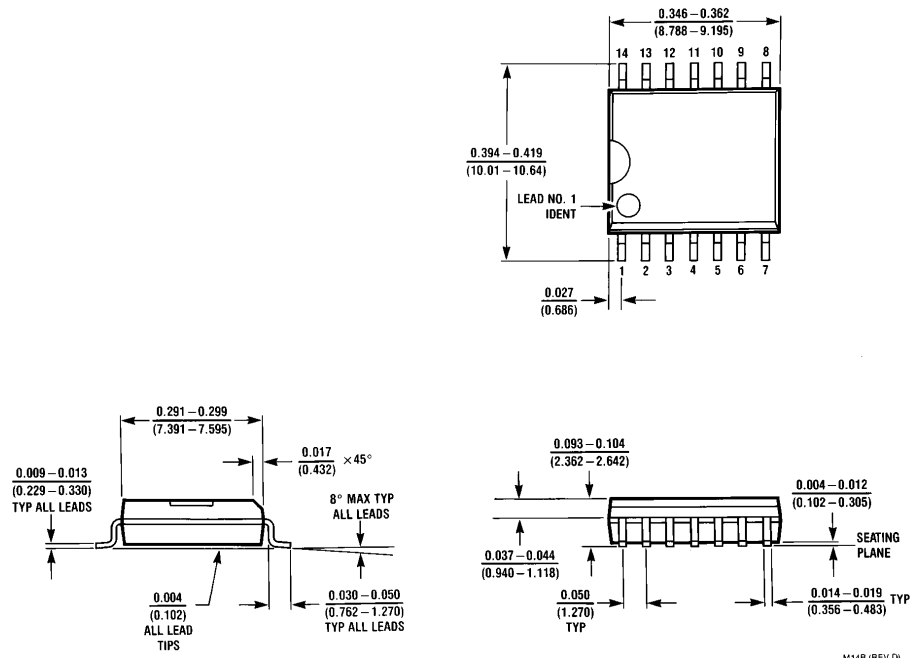
20-Pin Leadless Chip Carrier
Order Number LM6118E/883
NS Package Number E20A



J08A (REV K)

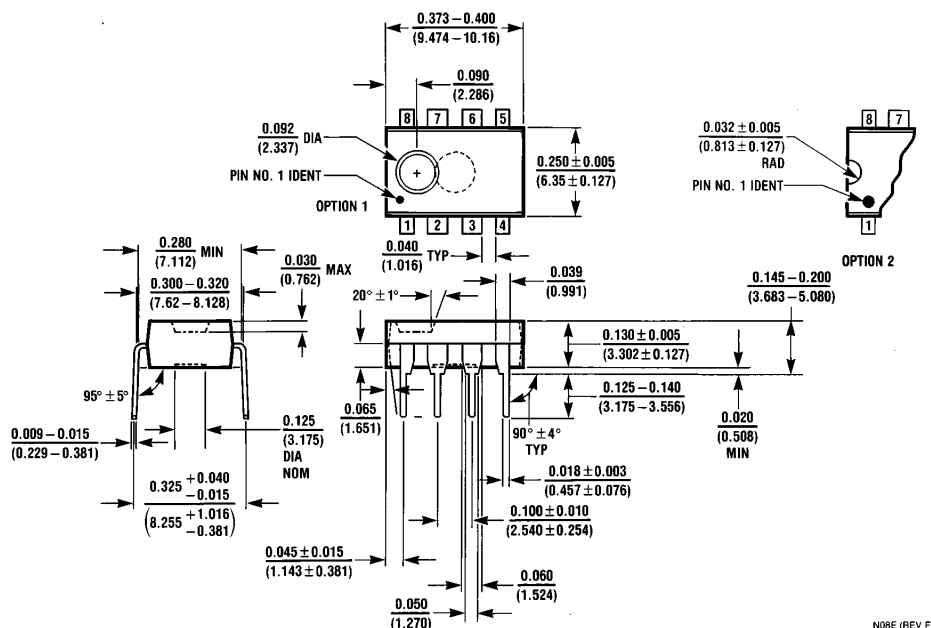
8-Lead Ceramic Dual-In-Line Package (J)
Order Number LM6118J/883
NS Package Number J08A

Physical Dimensions inches (millimeters)



M14B (REV D)

8-Lead Molded Small Outline Package (M)
Order Number LM6218AWM or LM6218WM
NS Package Number M14B

Physical Dimensions inches (millimeters) (Continued)

8-Lead Molded Dual-In-Line Package (N)
Order Number LM6118N, LM6218AN or LM6218N
NS Package Number N08E

N08E (REV F)

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