TM4100GAD8
4 194 304 BY 8-BIT DYNAMIC RAM MODULE

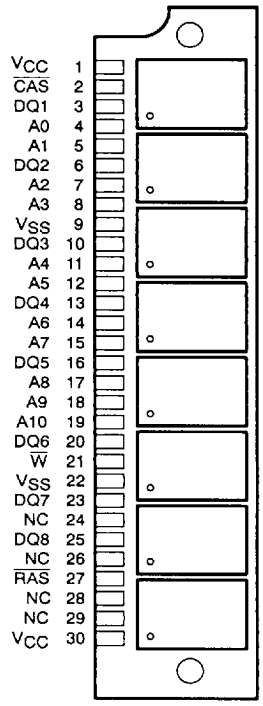
SMMS508A–MARCH 1992–REVISED JANUARY 1993

- **Organization . . . 4 194 304 × 8**
- **Single 5-V Power Supply (±10% Tolerance)**
- **30-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Eight 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'4100GAD8-60	60 ns	30 ns	15 ns	110 ns
'4100GAD8-70	70 ns	35 ns	18 ns	130 ns
'4100GAD8-80	80 ns	40 ns	20 ns	150 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**

SINGLE IN-LINE MODULE†
(TOP VIEW)



† The package shown is for pinout reference only.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
NC	No Internal Connection
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4100GAD8 is a dynamic random-access memory module organized as 4 194 304 × 8-bits in a 30-pin leadless single in-line memory module (SIMM).

The SIMM is composed of eight TMS44100DJ, 4 194 304 × 1-bit dynamic RAMs in 20/26-lead plastic small-outline J-lead packages (SOJ), mounted on a substrate with decoupling capacitors.

The TM4100GAD8 is available in the AD single-sided, leadless module for use with sockets.

The TM4100GAD8 is characterized for operation from 0°C to 70°C.

operation

The TM4100GAD8 operates as eight TMS44100DJs connected as shown in the functional block diagram. Refer to the TMS44100 data sheet for details of its operation. The common I/O feature of the TM4100GAD8 dictates the use of early write cycles to prevent contention on D and Q.

single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

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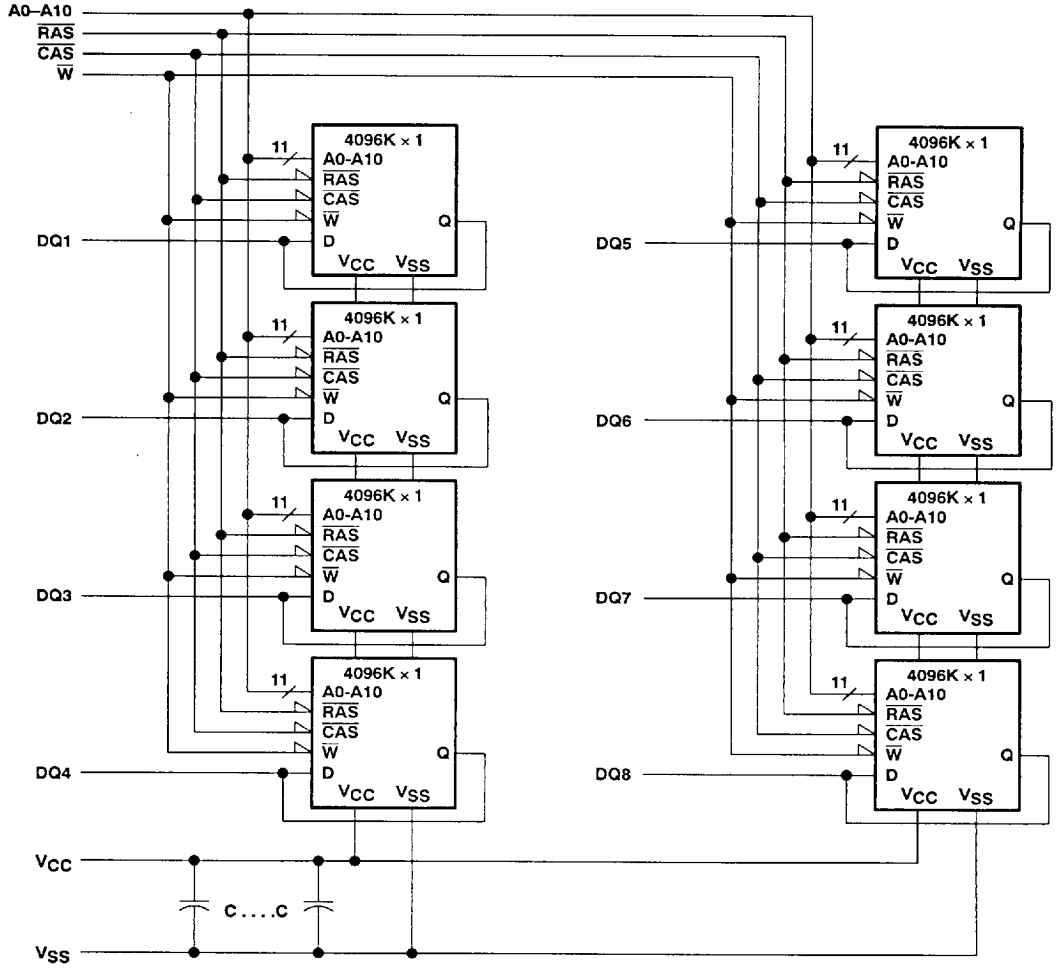
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Supply voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 8 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4100GAD8-60		'4100GAD8-70		'4100GAD8-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		840		720		640	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high,		16		16		16	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		8		8		8	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high		840		720		640	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, $t_{c(P)}$ = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		720		640		560	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		40	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		56	pF
$C_{i(W)}$	Input capacitance, write-enable input		56	pF
C_o	Output capacitance (pins DQ1–DQ8)		12	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on the pin under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4100GAD8-60		'4100GAD8-70		'4100GAD8-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'4100GAD8-60		'4100GAD8-70		'4100GAD8-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	$\overline{W}$ low setup time (test mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{DH}	Data hold time	10		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 10)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 10)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 9)	50		55		60		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTH}	$\overline{W}$ low hold time (test mode only)	10		10		10		ns

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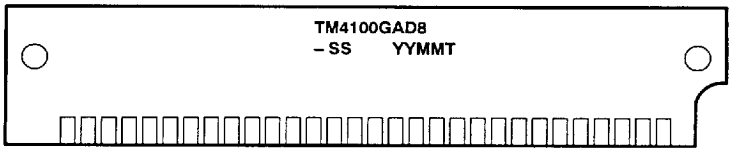
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		'4100GAD8-60		'4100GAD8-70		'4100GAD8-80		UINT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 11)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 11)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTE 11: The maximum value is specified only to assure access time.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed

NOTE: The location of symbolization may vary.

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