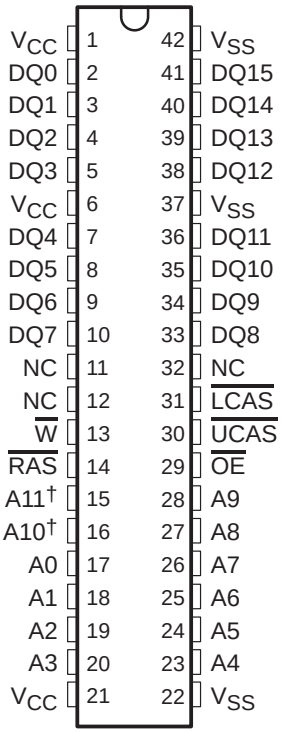
- **Organization . . . 1048576 Words by 16 Bits**
- **Single 5-V Power Supply**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR EDO CYCLE MIN
'41x169/P-60	60 ns	15 ns	30 ns	25 ns
'41x169/P-70	70 ns	18 ns	35 ns	30 ns
'41x169/P-80	80 ns	20 ns	40 ns	35 ns

- **Extended-Data-Out (EDO) Operation**
- **$\overline{\text{xCAS}}$-Before-$\overline{\text{RAS}}$ ($\overline{\text{x}}$CBR) Refresh**
- **$\overline{\text{RAS}}$-Only Refresh**
  - **1024-Cycle Refresh in 16 ms (TMS418169)**
  - **4096-Cycle Refresh in 64 ms (TMS416169)**
- **3-State Unlatched Output**
- **High-Reliability Plastic 42-Lead (DZ Suffix) 400-Mil-Wide Surface-Mount (SOJ) Package**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments Enhanced Performance Implanted CMOS (EPIC™) Process**

DZ PACKAGE
(TOP VIEW)



description

The TMS418169 and the TMS416169 are high-speed, 16777216-bit dynamic random-access memories (DRAMs) organized as 1048576 words of 16 bits each. Both devices employ state-of-the-art EPIC technology for high performance, reliability, and low power at low cost.

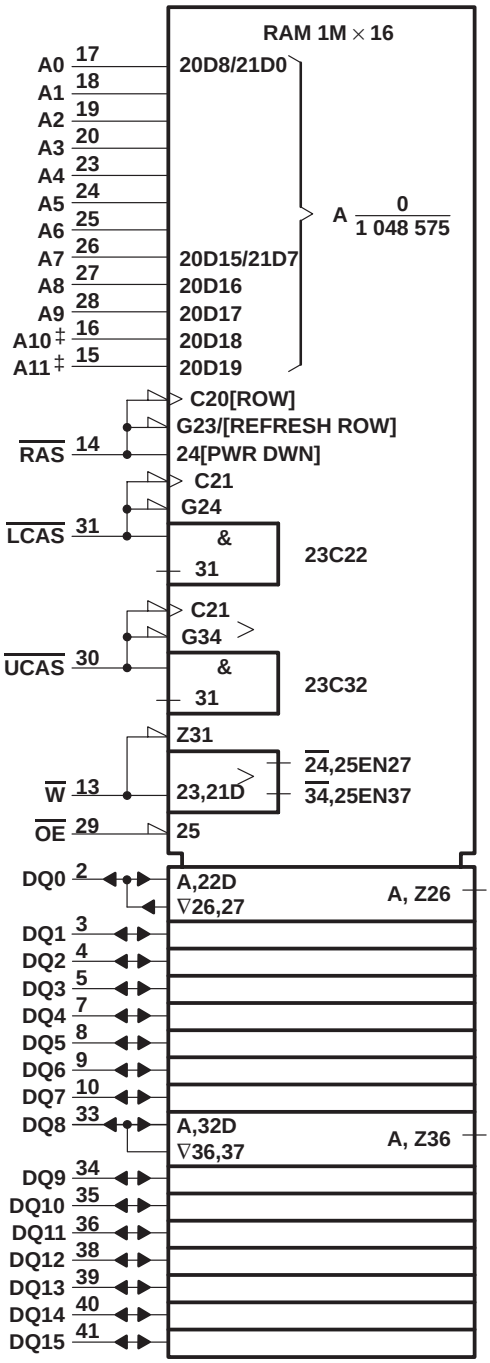
These devices feature maximum $\overline{\text{RAS}}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

† A10 and A11 are NC for TMS418169.

PIN NOMENCLATURE	
A0–A11	Address Inputs
DQ0–DQ15	Data In/Data Out
$\overline{\text{LCAS}}$	Lower Column-Address Strobe
$\overline{\text{UCAS}}$	Upper Column-Address Strobe
NC	No Internal Connection
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

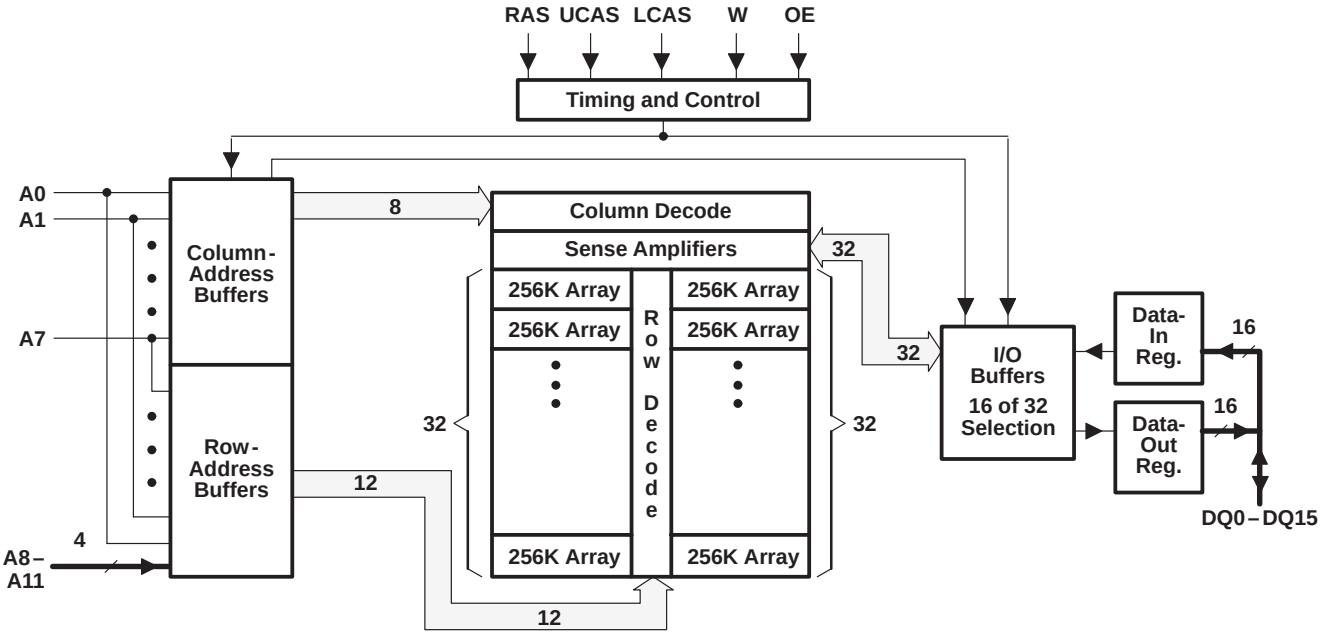
The TMS416169 and TMS418169 are offered in a 42-lead plastic surface-mount SOJ (DZ suffix) package. The package is characterized for operation from 0°C to 70°C.

logic symbol†

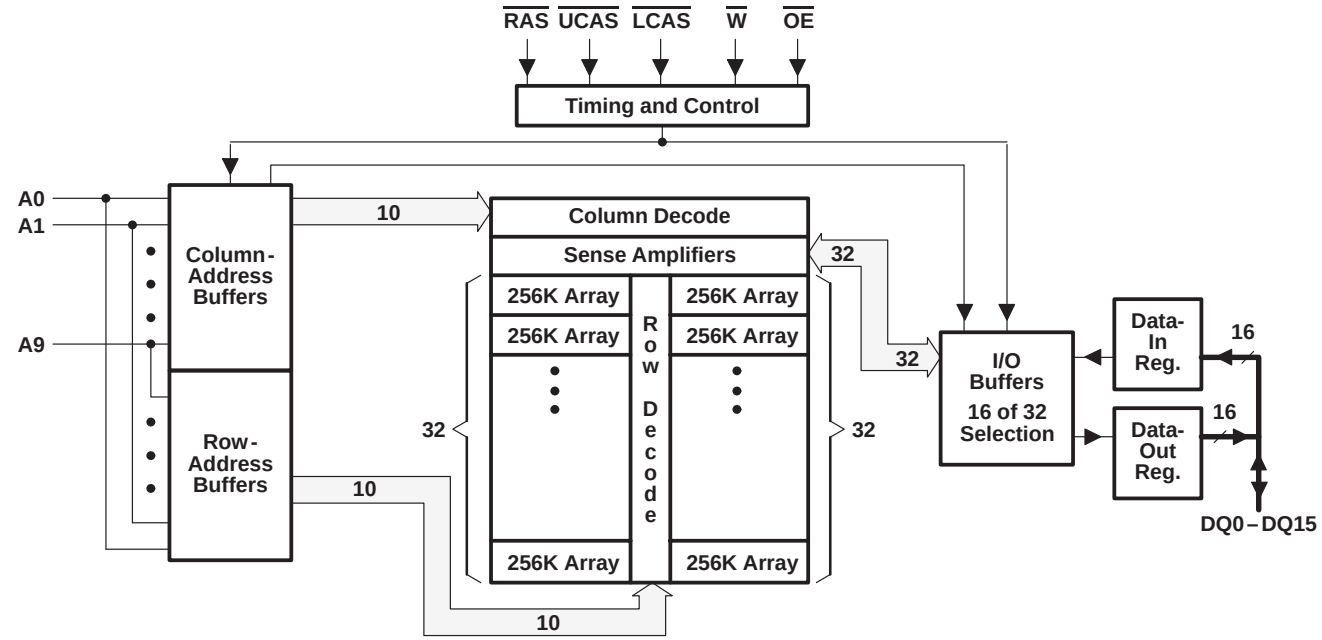


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.
‡ A10 and A11 are NC for TMS418169.

functional block diagram (TMS416169)



functional block diagram (TMS418169)



operation

dual $\overline{\text{CAS}}$

Two $\overline{\text{CAS}}$ pins ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$) are provided to give independent control of the 16 data-I/O pins (DQ0–DQ15), with $\overline{\text{LCAS}}$ corresponding to DQ0–DQ7 and $\overline{\text{UCAS}}$ corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first $\overline{\text{xCAS}}$ falling edge. Each $\overline{\text{xCAS}}$ going low enables its corresponding DQx pin with data associated with the column address latched on the first falling $\overline{\text{xCAS}}$ edge. All address setup and hold parameters are referenced to the first falling $\overline{\text{xCAS}}$ edge.The delay time from $\overline{\text{xCAS}}$ low to valid data out (see parameter t_{CAC}) is measured from each individual $\overline{\text{xCAS}}$ to its corresponding DQx pin.

In order to latch in a new column address, both $\overline{\text{xCAS}}$ pins must be brought high. The column-precharge time (see parameter t_{CP}) is measured from the last $\overline{\text{xCAS}}$ rising edge to the first $\overline{\text{xCAS}}$ falling edge of the new cycle. Keeping a column address valid while toggling $\overline{\text{xCAS}}$ requires a minimum setup time, t_{CLCH}. During t_{CLCH}, at least one $\overline{\text{xCAS}}$ must be brought low before the other $\overline{\text{xCAS}}$ is taken high.

For early-write cycles, the data is latched on the first $\overline{\text{xCAS}}$ falling edge. Data is written only into the DQs that have the corresponding $\overline{\text{xCAS}}$ low. Each $\overline{\text{xCAS}}$ must meet t_{CAS} minimum in order to ensure writing into the storage cell. To latch a new address and new data, all $\overline{\text{xCAS}}$ pins must be high and meet t_{CP}.

extended data out

Extended data out (EDO) allows for data-output rates of up to 40 MHz for 60-ns devices. When keeping the same row address while selecting random column addresses, the time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{\text{RAS}}$ low time (t_{RASP}).

EDO does not enter the DQs into the high-impedance state with the rising edge of $\overline{\text{xCAS}}$. The output remains valid for the system to latch the data. After $\overline{\text{xCAS}}$ goes high, the DRAM is decoding the next address. $\overline{\text{OE}}$ and $\overline{\text{W}}$ can be used to control the output impedance. Descriptions of $\overline{\text{OE}}$ and $\overline{\text{W}}$ further explain EDO operation benefit.

address: A0 – A11 (TMS416169) and A0 – A9 (TMS418169)

Twenty address bits are required to decode one of the 1048576 storage cell locations. For the TMS416169, 12 row-address bits are set up on A0 through A11 and latched onto the chip by $\overline{\text{RAS}}$. Eight column-address bits are set up on A0 through A7 and latched on the chip by the first $\overline{\text{xCAS}}$. For the TMS418169, 10 row-address bits are set up on A0–A9 and latched on the chip by $\overline{\text{RAS}}$. Ten column-address bits are set up on A0–A9 and latched on the chip by the first $\overline{\text{xCAS}}$. All addresses must be stable on or before the falling edge of $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$. $\overline{\text{RAS}}$ is similar to a chip-enable in that it activates the sense amplifiers as well as the row decoder. $\overline{\text{xCAS}}$ is used as a chip-select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

write enable ($\overline{\text{W}}$)

The read or write mode is selected through $\overline{\text{W}}$. A logic high on $\overline{\text{W}}$ selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. When $\overline{\text{W}}$ goes low prior to $\overline{\text{xCAS}}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation independent of the state of $\overline{\text{OE}}$. This permits early-write operation to be completed with $\overline{\text{OE}}$ grounded. If $\overline{\text{W}}$ goes low in an extended-data-out read cycle, the DQs go into the high-impedance state as long as $\overline{\text{xCAS}}$ is high.

data in (DQ0 – DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{\text{xCAS}}$ or $\overline{\text{W}}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{\text{W}}$ is brought low prior to $\overline{\text{xCAS}}$ and the data is strobed in by the first occurring $\overline{\text{xCAS}}$ with setup and hold times referenced to this signal. In a

data in (DQ0 – DQ15) (continued)

delayed-write or read-modify-write cycle, $\overline{xCAS}$ is already low and the data is strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ0 – DQ15)

Data out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{xCAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{xCAS}$) as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. While $\overline{xCAS}$ and $\overline{RAS}$ are low and $\overline{W}$ is high, $\overline{OE}$ can be brought low or high and the DQs switch from valid data to high impedance. There are two methods for placing the DQs into the high-impedance state and keeping them in that state during $\overline{xCAS}$ high time using $\overline{OE}$. The first method is to switch $\overline{OE}$ high before $\overline{xCAS}$ goes high and keep $\overline{OE}$ high for t_{CHO} past the $\overline{CAS}$ transition. This disables the DQs and they remain in the high-impedance state, regardless of $\overline{OE}$, until $\overline{xCAS}$ falls again. The second method is to have $\overline{OE}$ low as $\overline{xCAS}$ transitions high. Then $\overline{OE}$ can pulse high for a minimum of t_{OEP} anytime during $\overline{CAS}$ high time disabling the DQs regardless of further transitions on $\overline{OE}$ until $\overline{CAS}$ falls again.

$\overline{RAS}$-only refresh

TMS416169

A refresh operation must be performed at least once every 64 ms to retain data. This is achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

TMS418169

A refresh operation must be performed at least once every 16 ms to retain data. This is achieved by strobing each of the 1024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding both $\overline{xCAS}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pins. This is accomplished by holding $\overline{xCAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored and the refresh address is generated internally.

$\overline{xCAS}$-before-$\overline{RAS}$ (xCBR) refresh

xCBR refresh is achieved by bringing at least one $\overline{xCAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive xCBR refresh cycles, $\overline{xCAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

power-up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after power-up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or xCBR) cycle.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 1 V to 7 V
Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		’41x169			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

TMS416169

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'416169-60		'416169-70		'416169-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other inputs = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 5.5 V, V_O = 0 V to V_{CC}, xCAS high		± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		90		80		70	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, RAS and xCAS high		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, RAS and xCAS high		1		1		1	mA
I_{CC3}§	Average refresh current (RAS-only refresh or CBR)	$\overline{V_{CC}}$ = 5.5 V, Minimum cycle, RAS cycling, xCAS high (RAS only), RAS low after xCAS low (CBR)		90		80		70	mA
I_{CC4}‡¶	Average EDO current	$\overline{V_{CC}}$ = 5.5 V, t_{HPC} = MIN, RAS low, xCAS cycling		100		90		80	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while xCAS = V_{IH}

TMS418169

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†	'418169-60		'418169-70		'418169-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other inputs = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 5.5 V, V_O = 0 V to V_{CC}, $\overline{xCAS}$ high		± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		190		180		170	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{xCAS}$ high		1		1		1	mA
I_{CC3}§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	$\overline{V_{CC}}$ = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{xCAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{xCAS}$ low (CBR)		190		180		170	mA
I_{CC4}‡¶	Average EDO current	$\overline{V_{CC}}$ = 5.5 V, t_{HPC} = MIN, $\overline{RAS}$ low, $\overline{xCAS}$ cycling		100		90		80	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{xCAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11†		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{xCAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_O	Output capacitance		7	pF

† A10 and A11 are NC for TMS418169.

NOTE 3: V_{CC} = 5 V ± 0.5 V or 3.3 V ± 0.3 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

PARAMETER		'41x169-60		'41x169-70		'41x169-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$		15		18		20	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$		15		18		20	ns
t_{CLZ}	Delay time, $\overline{CAS}$ to output in the low-impedance state	0		0		0		ns
t_{OEZ}	Output buffer turn off delay from $\overline{OE}$ (see Note 5)	3	15	3	18	3	20	ns
t_{REZ}	Output buffer turn off delay from $\overline{RAS}$ (see Note 5)	3	15	3	18	3	20	ns
t_{CEZ}	Output buffer turn off delay from $\overline{CAS}$ (see Note 5)	3	15	3	18	3	20	ns
t_{WEZ}	Output buffer turn off delay from $\overline{W}$ (see Note 5)	3	15	3	18	3	20	ns

NOTES: 4. With ac parameters, it is assumed t_T = 5 ns.

5. Maximum t_{REZ}, t_{CEZ}, t_{WEZ}, and t_{OEZ} are specified when the output is no longer driven.

EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

		'41x169-60		'41x169-70		'41x169-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page-mode read or write	25		30		35		ns
t_{PRWC}	Cycle time, EDO read-write	80		90		100		ns
t_{CSH}	Delay time, $\overline{RAS}$ active to $\overline{CAS}$ precharge	50		55		60		ns
t_{CHO}	Hold time, $\overline{OE}$ from $\overline{CAS}$	10		10		10		ns
t_{DOH}	Hold time, output from $\overline{CAS}$ active	3		3		3		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ active	10	10000	12	10000	15	10000	ns
t_{WPE}	Pulse duration, $\overline{W}$ (output disable only)	5		5		5		ns
t_{OCH}	Setup time, $\overline{OE}$ before $\overline{CAS}$	10		10		10		ns
t_{CP}	Pulse duration, $\overline{CAS}$ precharge	5		5		5		ns
t_{OEP}	Precharge time, $\overline{OE}$ (output disable only)	5		5		5		ns

NOTE 4: With ac parameters, it is assumed t_T = 5 ns.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

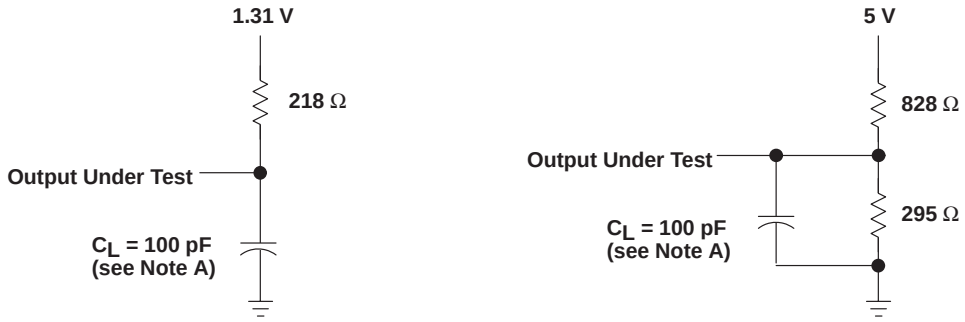
		’41x169-60		’41x169-70		’41x169-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read	110		130		150		ns
t_{WC}	Cycle time, write	110		130		150		ns
t_{RWC}	Cycle time, read-write	150		175		200		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ active, page mode (see Note 6)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ active, nonpage mode (see Note 6)	60	10 000	70	10 000	80	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ precharge	40		50		60		ns
t_{WP}	Pulse duration, write command	10		10		10		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data in (see Note 7)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{CAS}$ precharge	10		12		15		ns
t_{RWL}	Setup time, write command before $\overline{RAS}$ precharge	10		12		15		ns
t_{WCS}	Setup time, write command before $\overline{CAS}$ active (early-write only)	0		0		0		ns
t_{CSR}	Setup time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)	5		5		5		ns
t_{CAH}	Hold time, column address	10		12		15		ns
t_{DH}	Hold time, data in (see Note 7)	10		12		15		ns
t_{RAH}	Hold time, row address	10		10		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{CAS}$ (see Note 8)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{RAS}$ (see Note 8)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{CAS}$ active (early-write only)	10		12		15		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	5		5		5		ns
t_{RHCP}	Hold time, $\overline{RAS}$ active from $\overline{CAS}$ precharge	35		40		45		ns
t_{OEH}	Hold time, $\overline{OE}$ command	15		18		20		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{CHR}	Hold time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)	10		10		10		ns
t_{AWD}	Delay time, column address to write command (read-write only)	55		63		70		ns
t_{CRP}	Delay time, $\overline{CAS}$ precharge to $\overline{RAS}$	5		5		5		ns
t_{CWD}	Delay time, $\overline{CAS}$ to write command (read-write only)	40		46		50		ns
t_{OED}	Delay time, $\overline{OE}$ to data in	15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ to column address (see Note 9)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ precharge	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ precharge	20		25		30		ns
t_{RCD}	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (see Note 9)	20	45	20	52	20	60	ns

NOTES: 4. With ac parameters, it is assumed t_T = 5 ns.
6. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
7. Referenced to the later of $\overline{xCAS}$ or $\overline{W}$ in write operations
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. The maximum value is specified only to ensure access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			’41x169-60		’41x169-70		’41x169-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{RPC}	Delay time, $\overline{RAS}$ precharge to $\overline{CAS}$		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ active to $\overline{RAS}$ precharge		10		12		15		ns
t_{RWD}	Delay time, $\overline{RAS}$ to write command (read-write only)		85		98		110		ns
t_{CPW}	Delay time, $\overline{CAS}$ precharge to write command (read-write only)		60		68		75		ns
t_{REF}	Refresh time interval	’416169		64		64		64	ms
		’418169		16		16		16	ms
t_T	Transition time		2	30	2	30	2	30	ns

PARAMETER MEASUREMENT INFORMATION

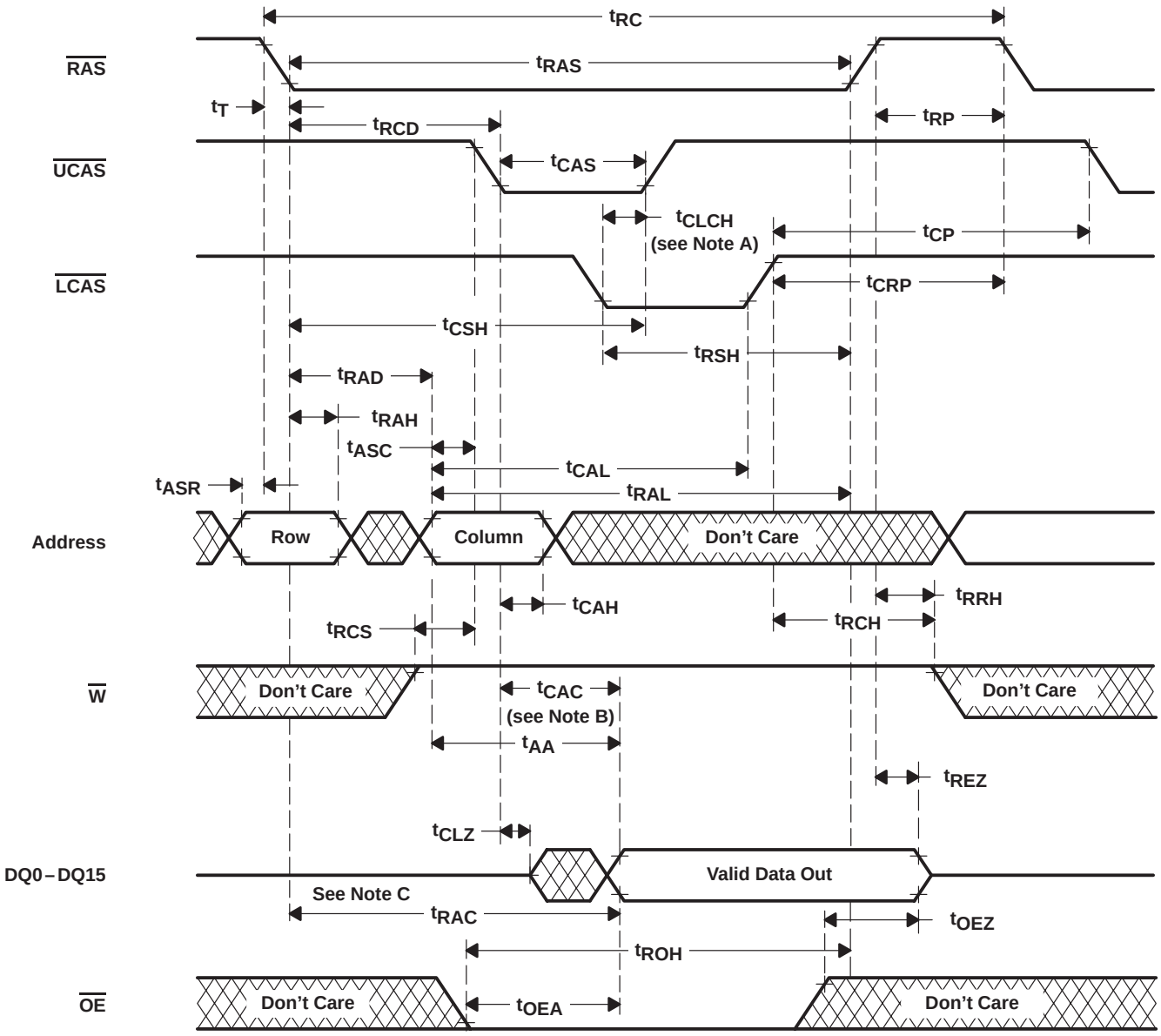


(a) LOAD CIRCUIT **(b) ALTERNATE LOAD CIRCUIT**

NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

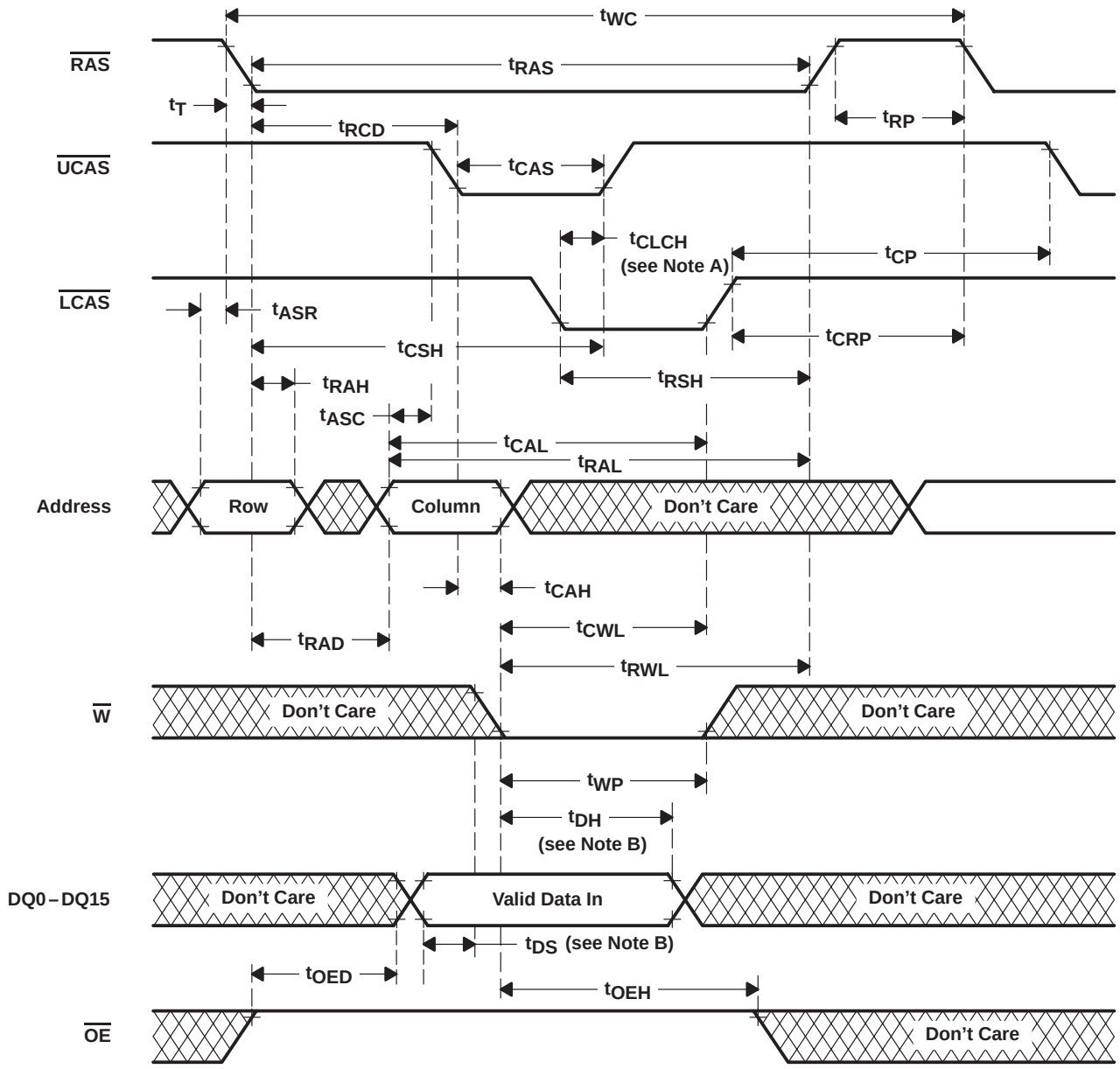
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 2. Read-Cycle Timing

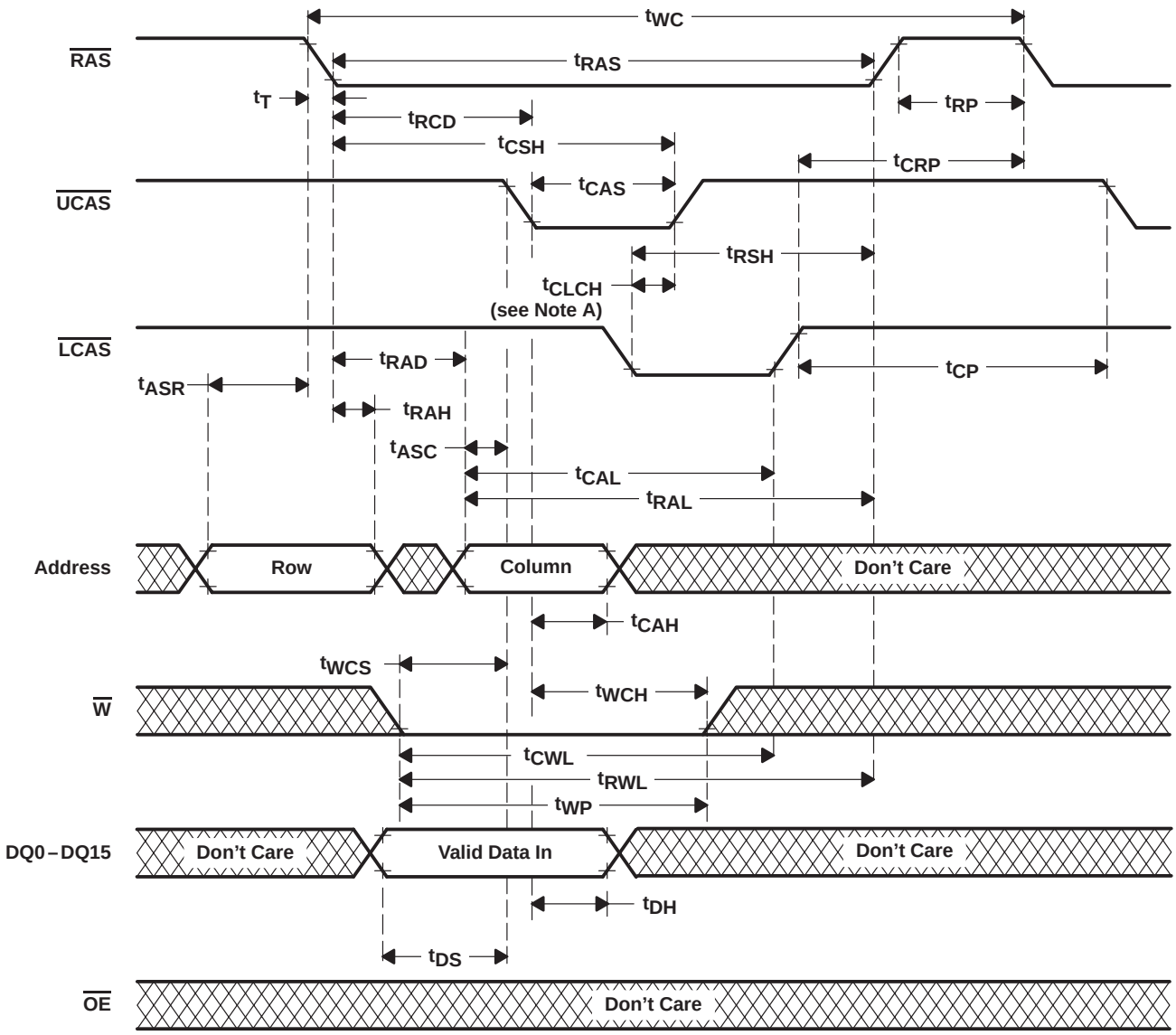
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Referenced to the first $\overline{\text{xCAS}}$ or $\overline{\text{W}}$, whichever occurs last
C. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 3. Write-Cycle Timing

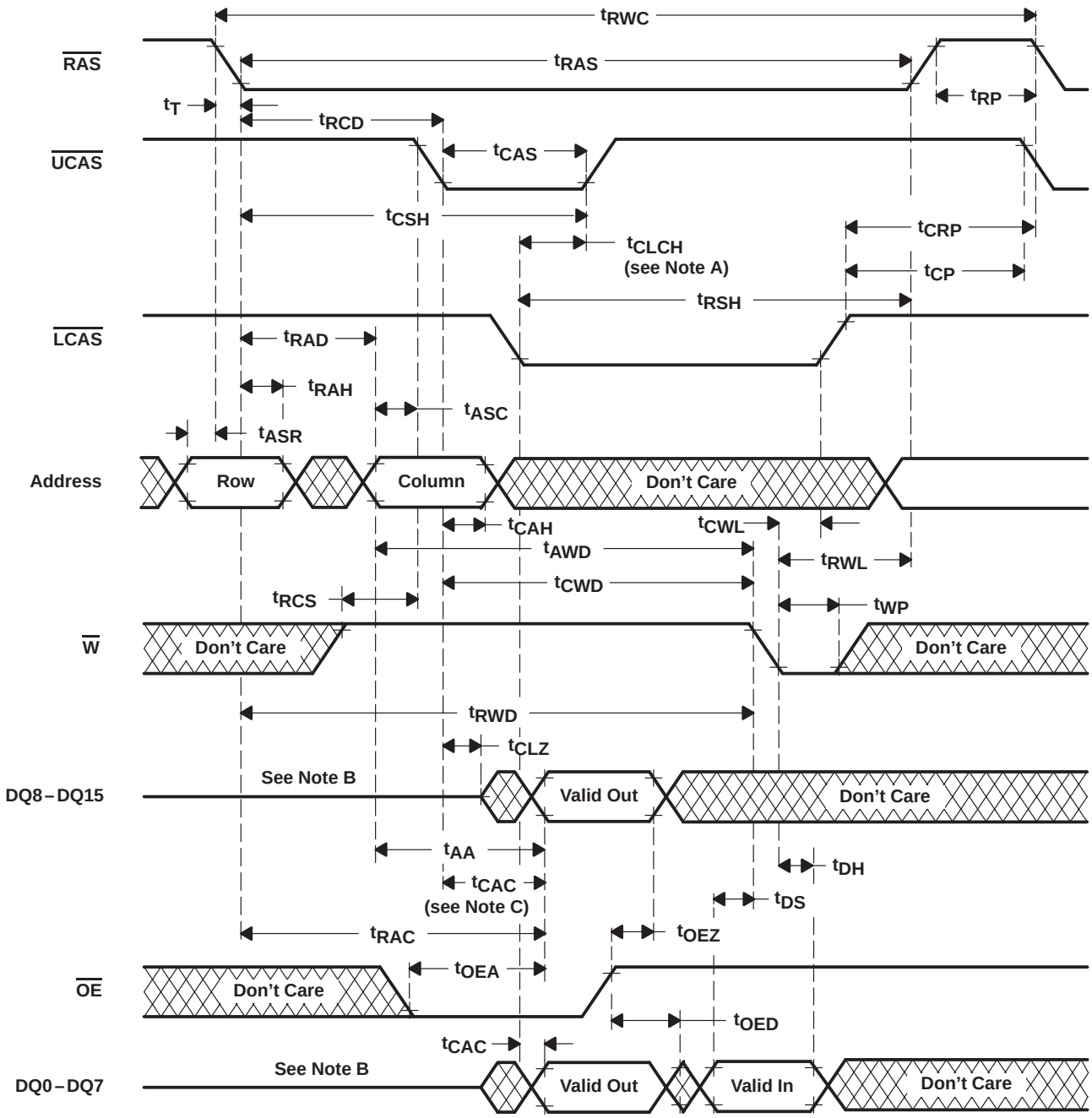
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
B. xCAS order is arbitrary.

Figure 4. Early-Write-Cycle Timing

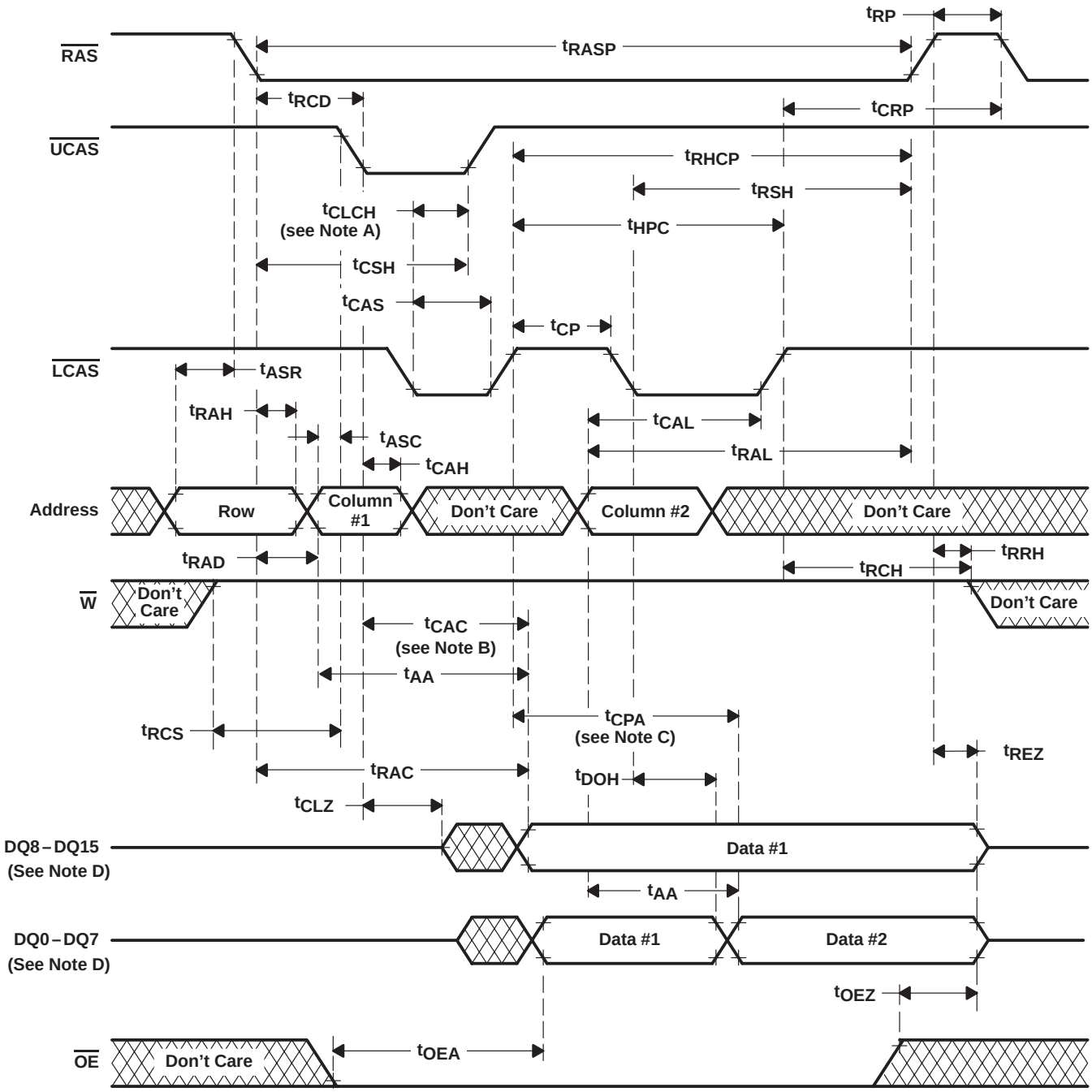
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first xCAS going low, the parameter t_{CLCH} must be met.
B. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
C. t_{CAC} is measured from xCAS to its corresponding DQx.
D. xCAS order is arbitrary.

Figure 5. Read-Modify-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.
C. Access time is t_{CPA} or t_{AA} dependent.
D. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
E. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write- and read-modify-write-timing specifications are not violated.
F. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 6. Extended-Data-Out Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

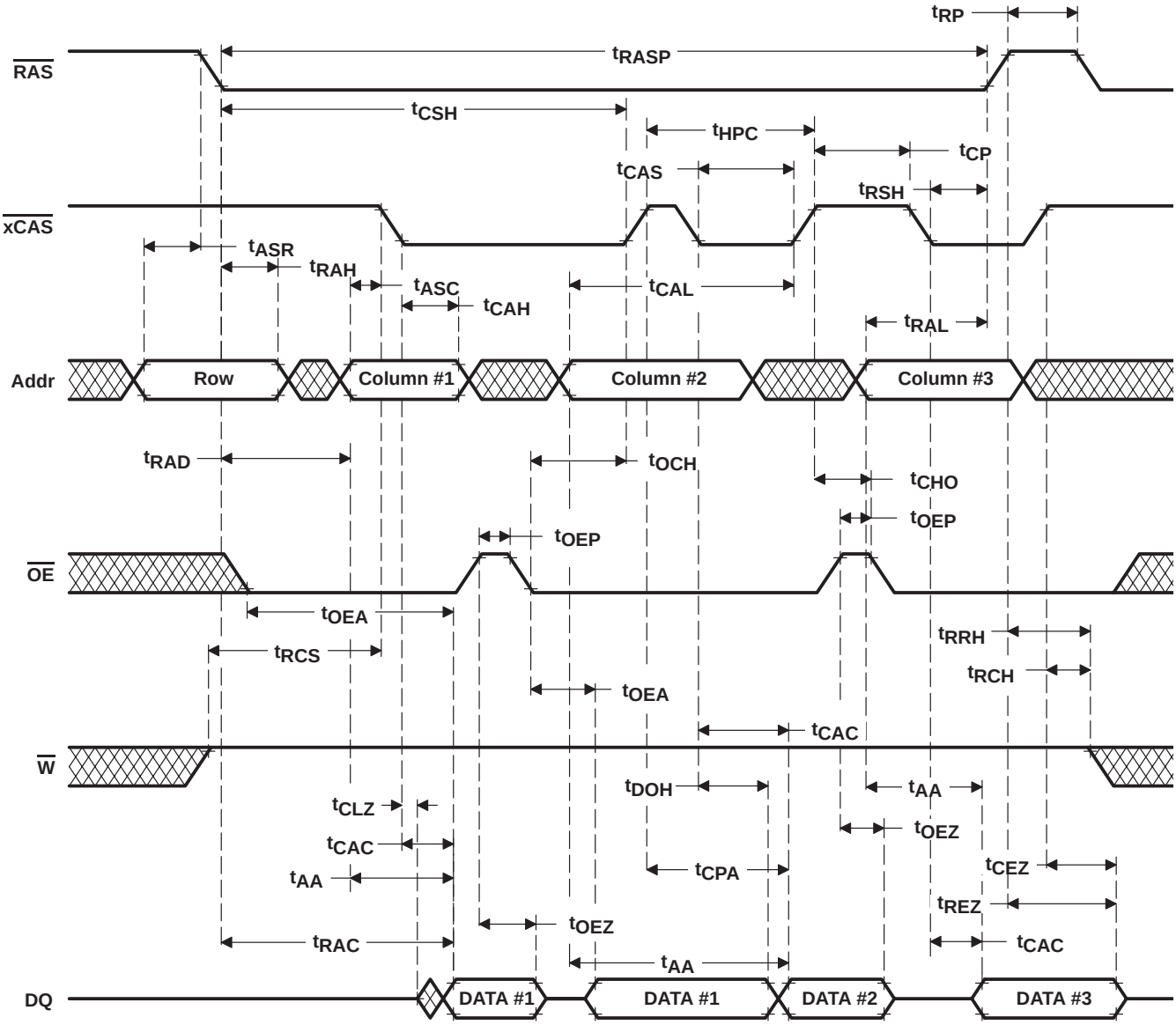


Figure 7. Extended-Data-Out Read-Cycle Timing With $\overline{OE}$ Control

PARAMETER MEASUREMENT INFORMATION

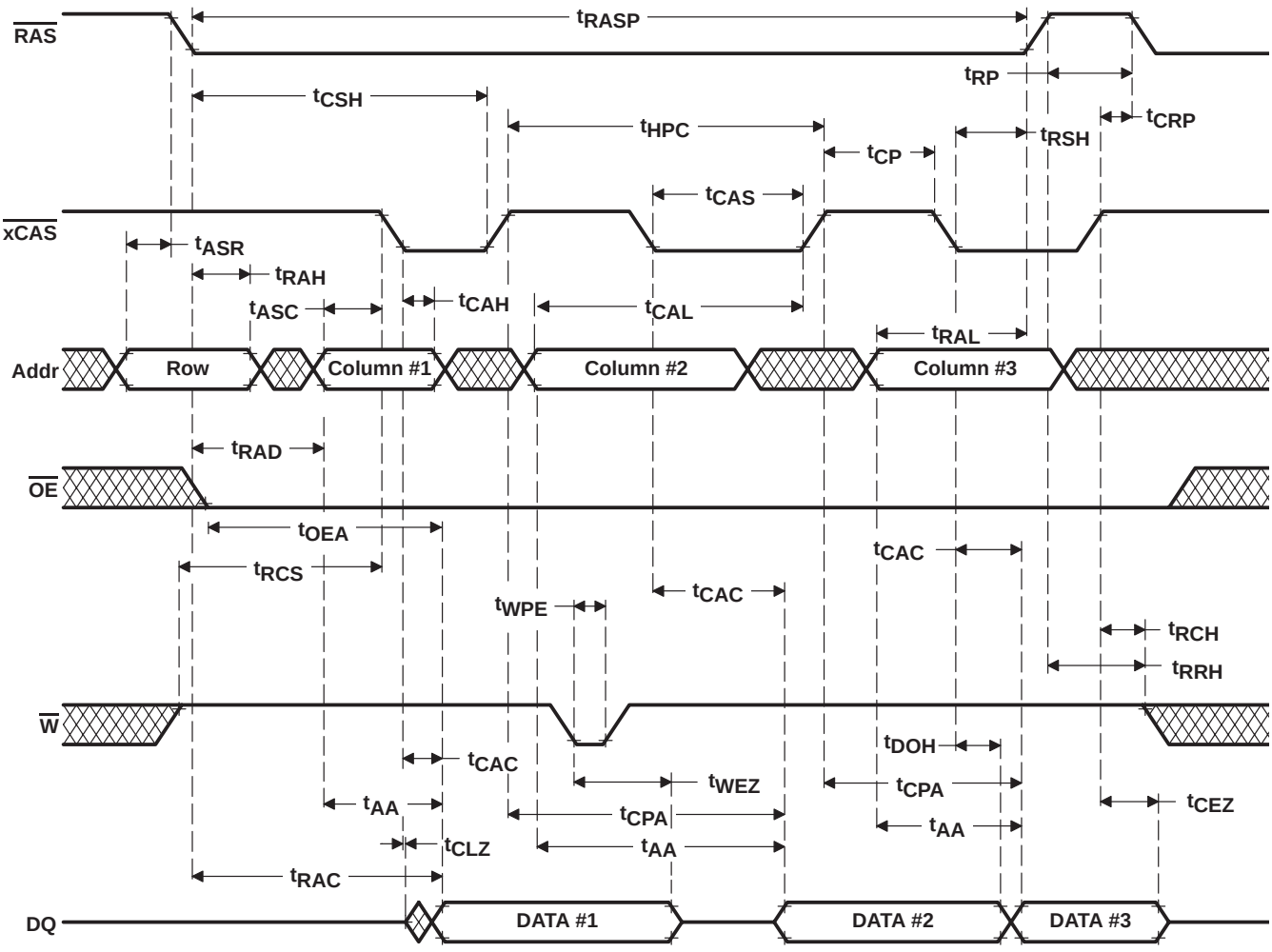
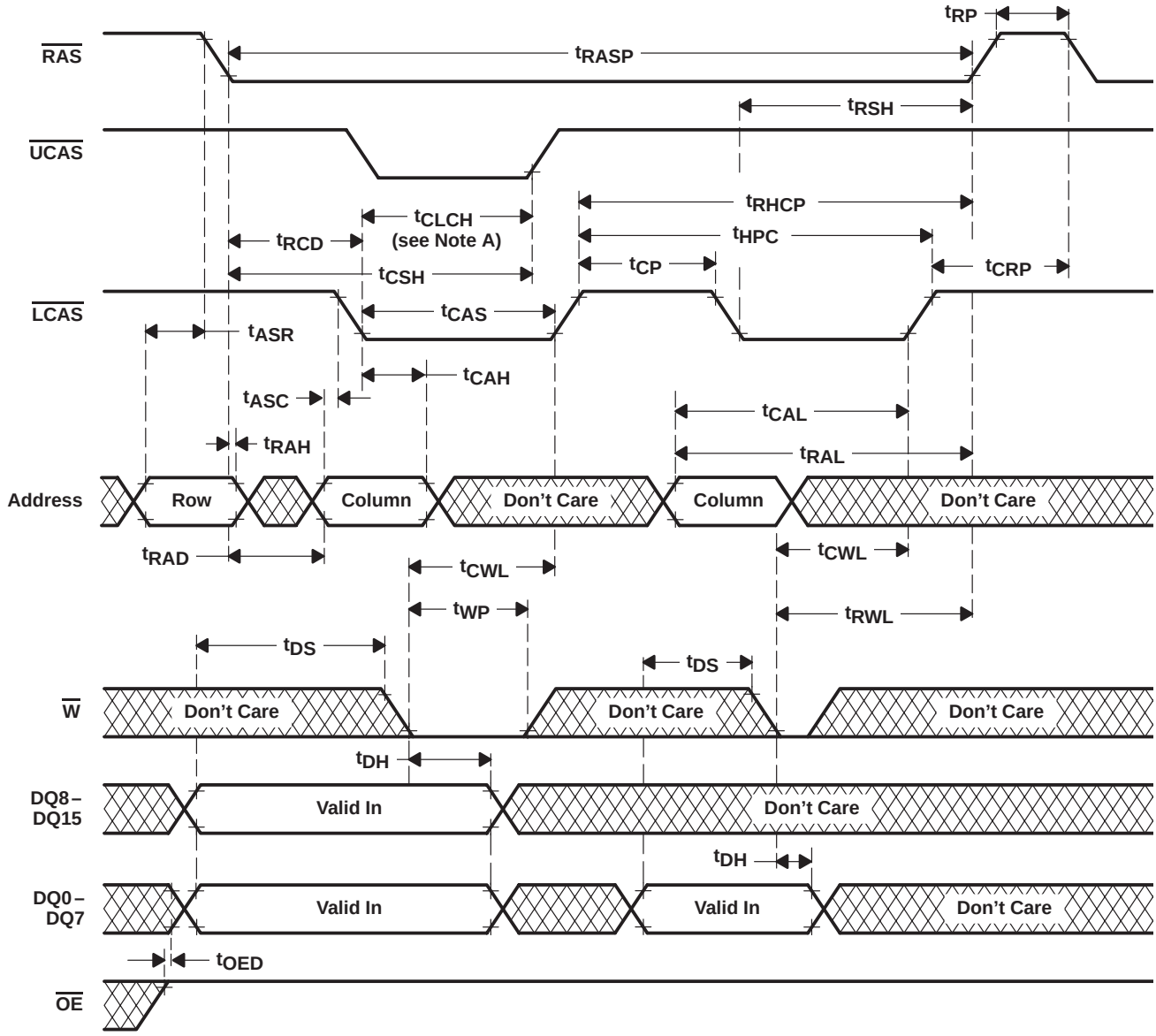


Figure 8. Extended-Data-Out Read-Cycle Timing With $\overline{W}$ Control

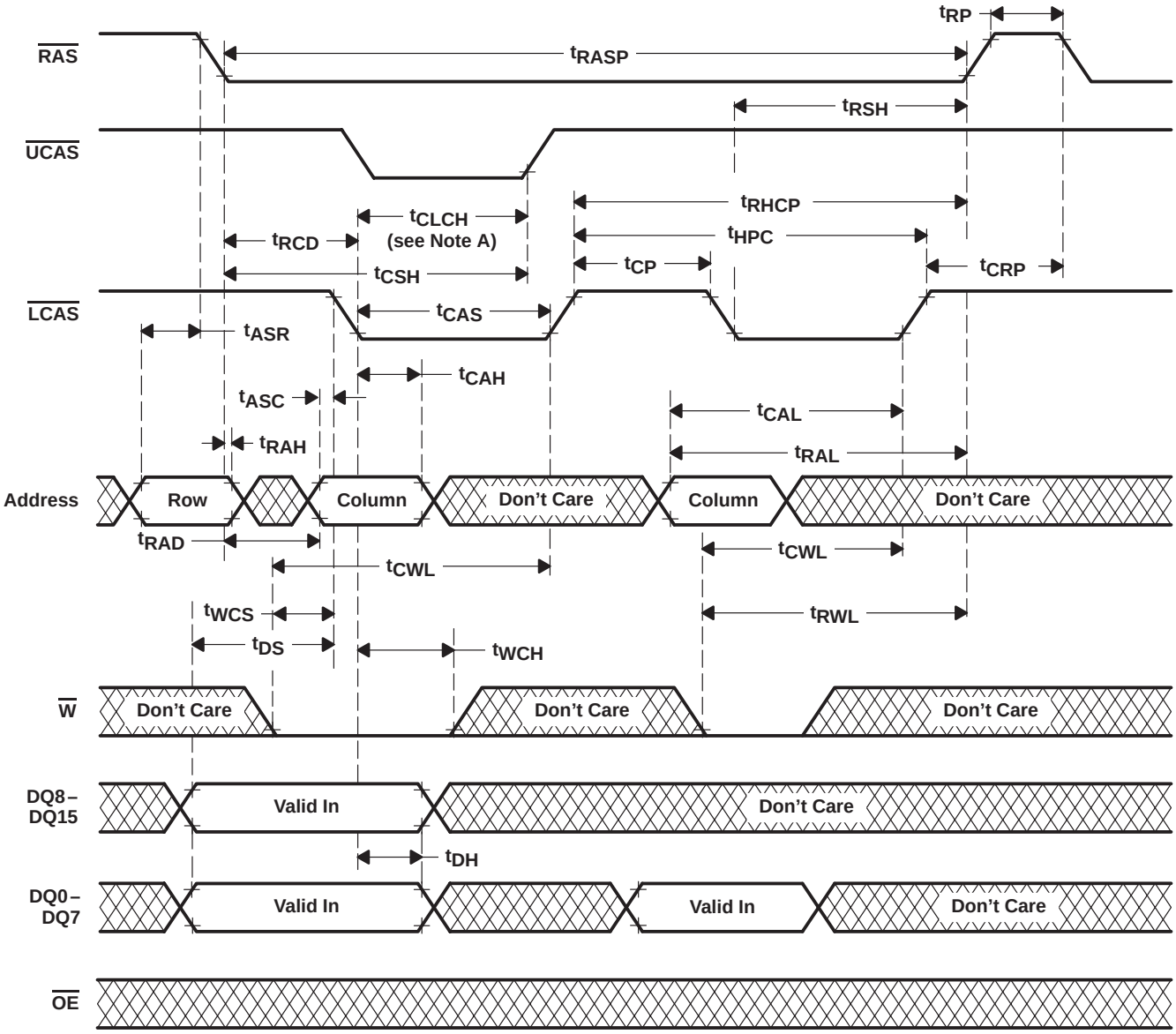
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write-timing specifications are not violated.
C. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 9. Extended-Data-Out Write-Cycle Timing

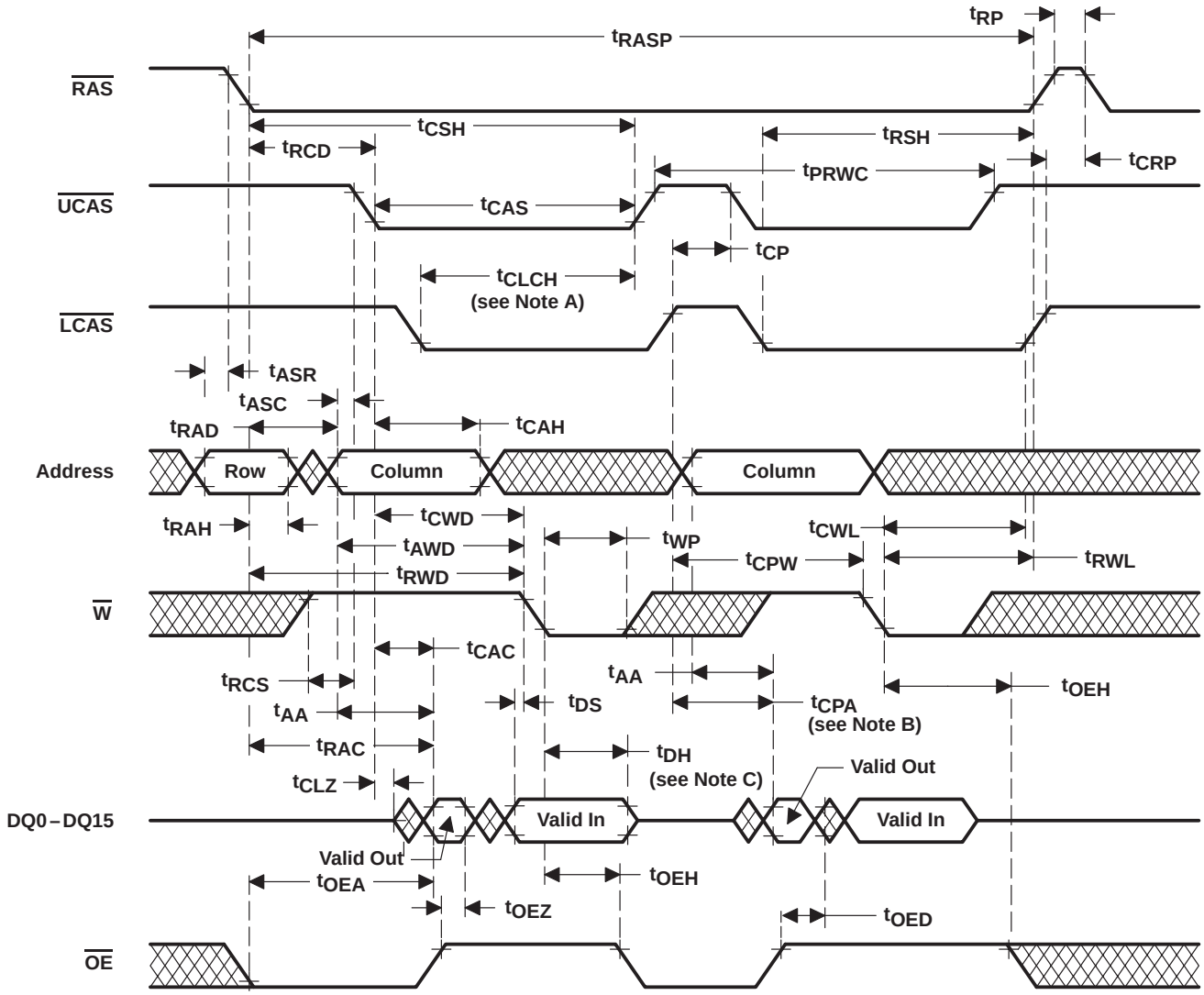
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read- and read-modify-write-timing specifications are not violated.
C. $\overline{\text{xCAS}}$ order is arbitrary.

Figure 10. Extended-Data-Out Early Write-Cycle Timing

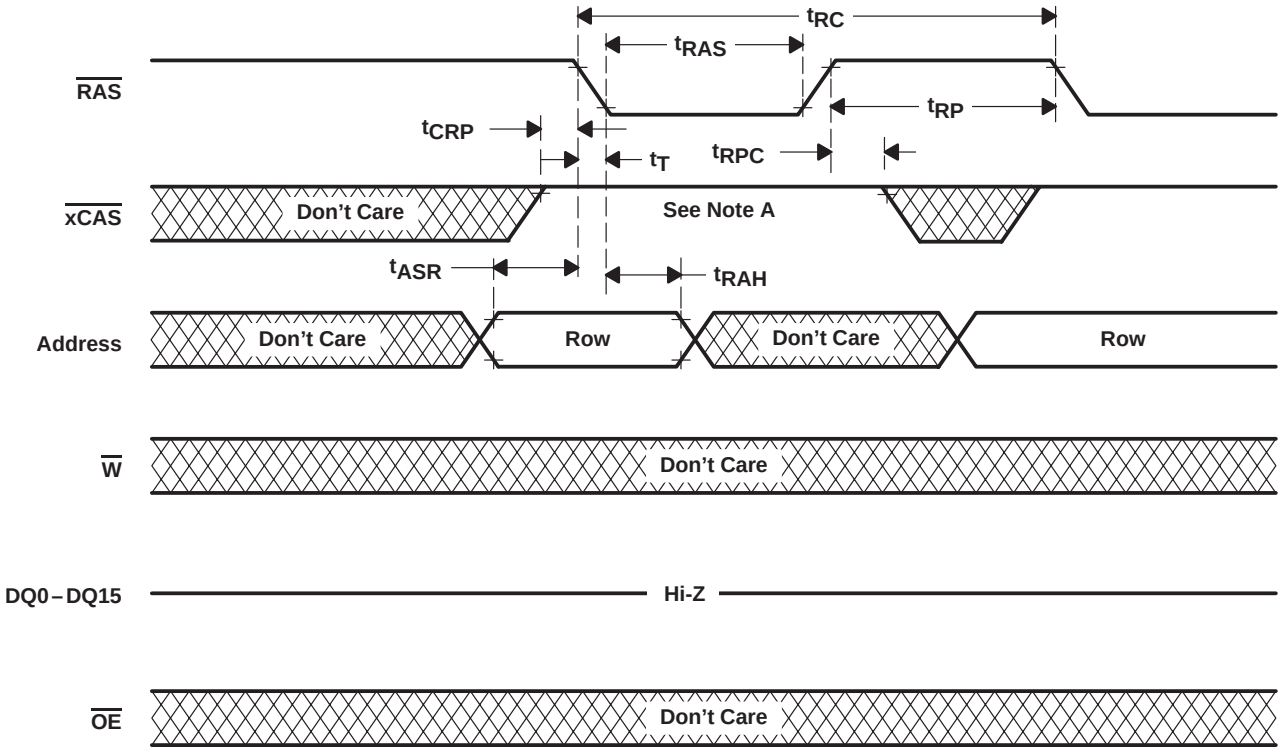
PARAMETER MEASUREMENT INFORMATION



NOTES: A. To hold the address latched by the first $\overline{\text{xCAS}}$ going low, the parameter t_{CLCH} must be met.
B. Access time is t_{CPA}- or t_{AA}-dependent.
C. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
D. xCAS order is arbitrary.
E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read- and write-cycle timing specifications are not violated.
F. t_{CAC} is measured from $\overline{\text{xCAS}}$ to its corresponding DQx.

Figure 11. Extended-Data-Out Read-Modify-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE G: All xCAS must be high.

Figure 12. RAS-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

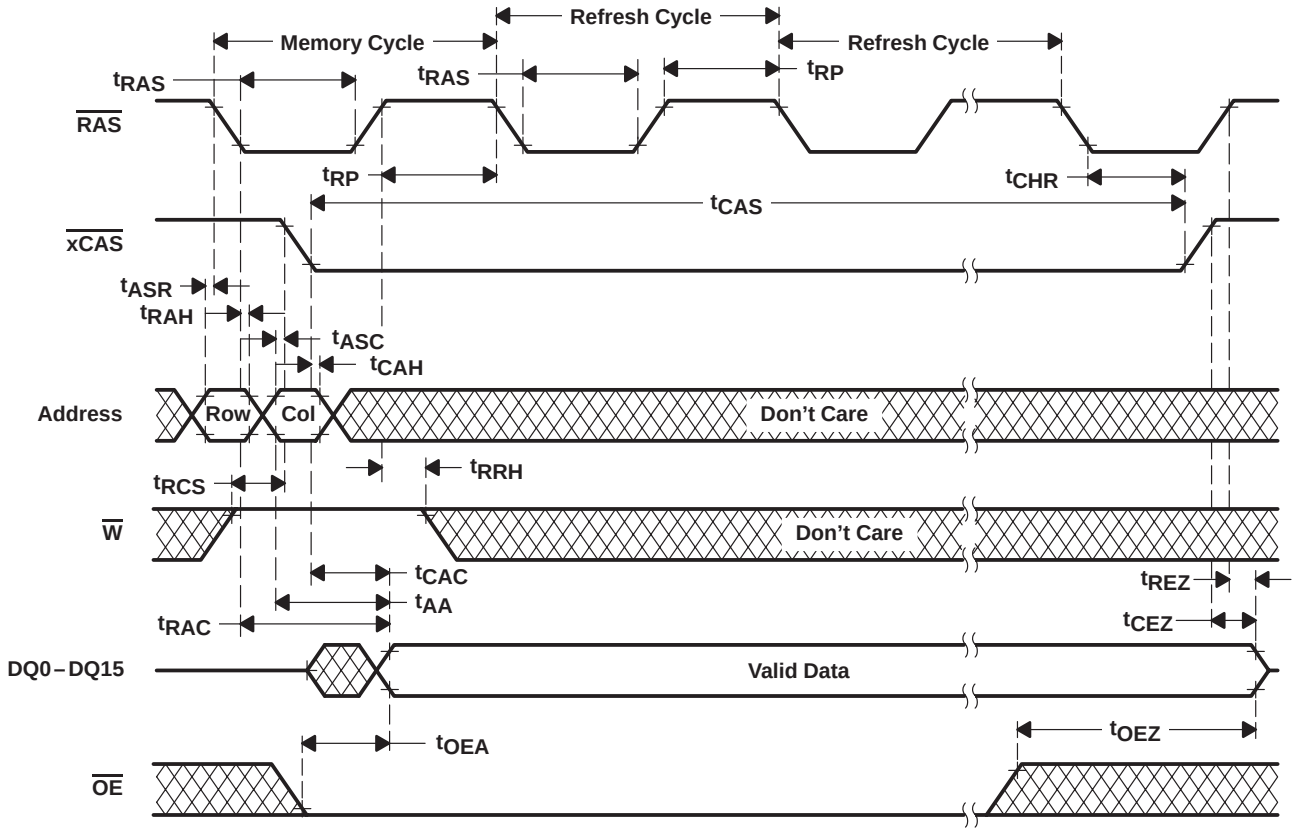
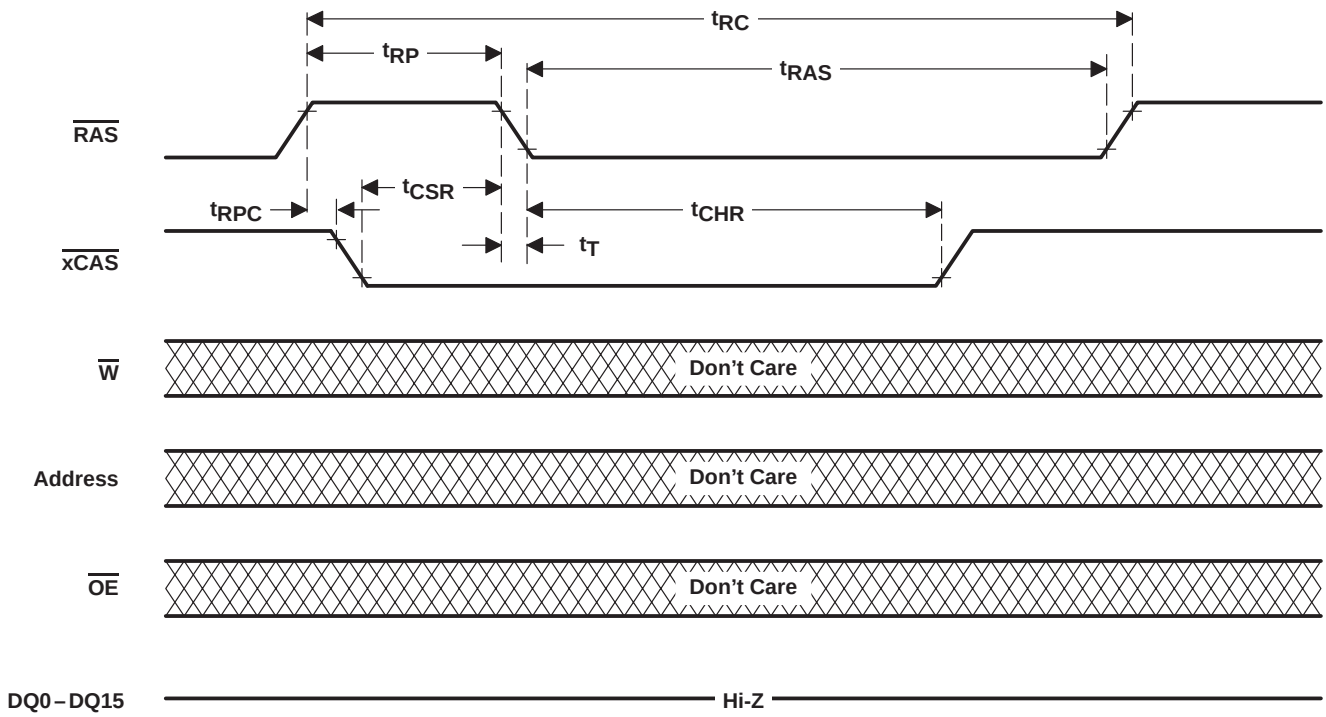


Figure 13. Hidden-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

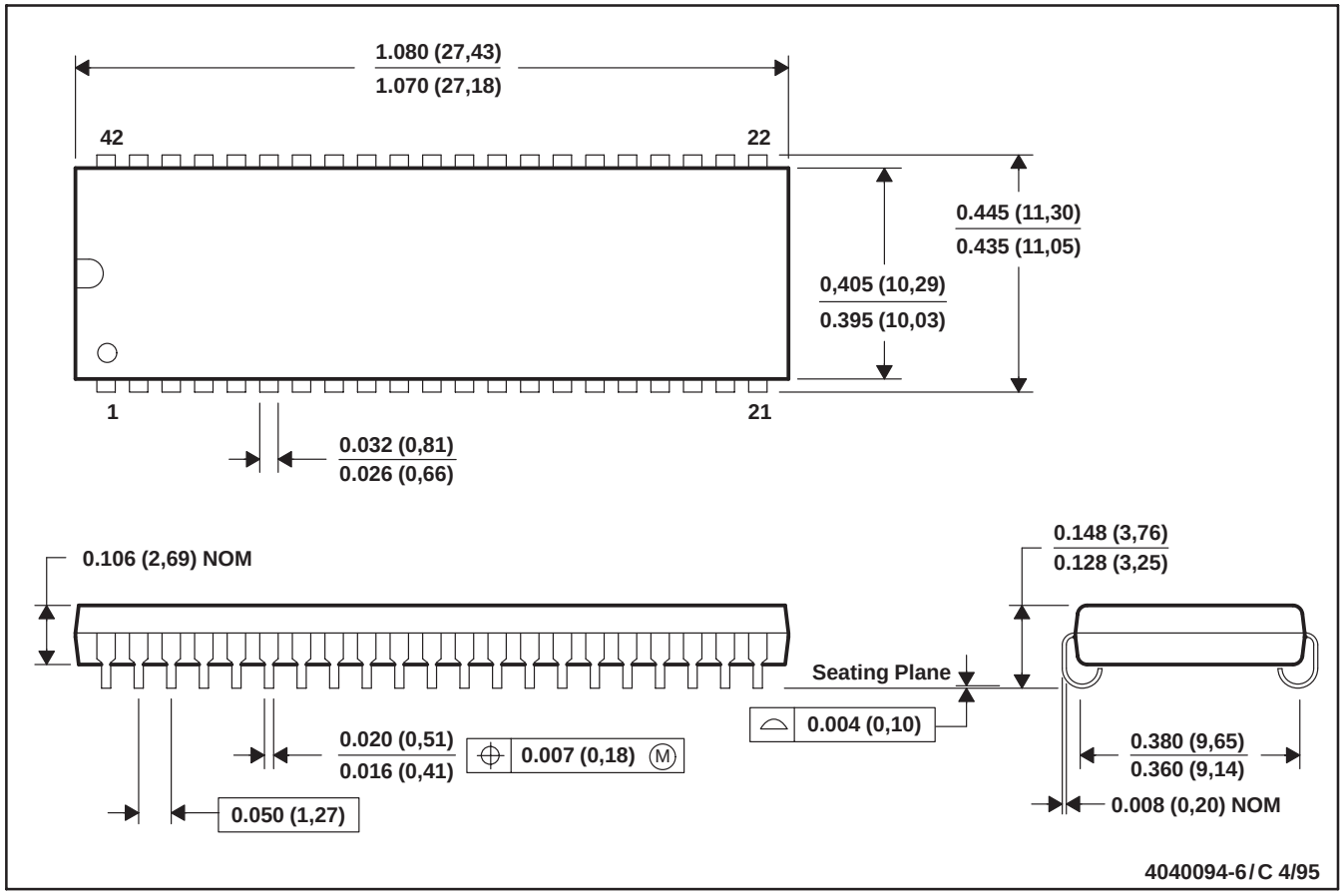


NOTE A: Any $\overline{\text{xCAS}}$ can be used.

Figure 14. Automatic (xCBR) Refresh-Cycle Timing

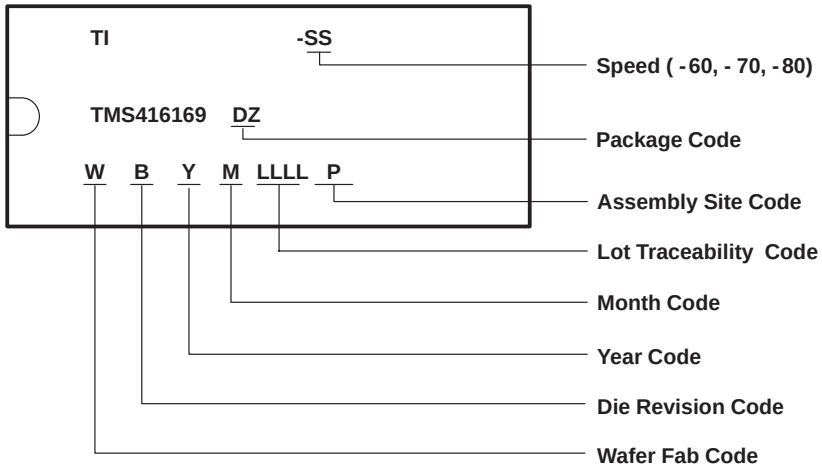
MECHANICAL DATA

DZ (R-PDSO-J42) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE**



NOTES: B. All linear dimensions are in inches (millimeters).
C. This drawing is subject to change without notice.
D. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

device symbolization (TMS416169 illustrated)



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