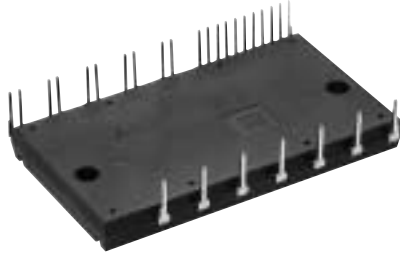


## PS22056



### INTEGRATED POWER FUNCTIONS

1200V/25A low-loss 4<sup>th</sup> generation IGBT inverter bridge  
for 3 phase DC-to-AC power conversion

### INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

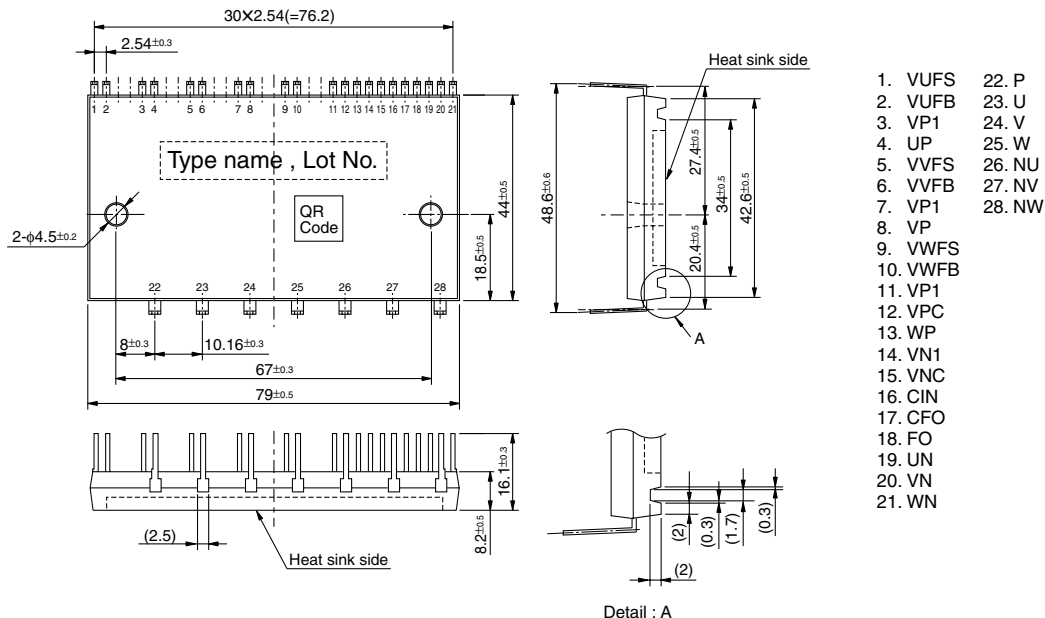
- For upper-leg IGBTs : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-side IGBT) or a UV fault (Lower-side supply).
- Input interface : 5V line CMOS/TTL compatible (High active logic).

## APPLICATION

AC400V 0.2kW~3.7kW inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES

Dimensions in mm



All external terminals are treated with lead free solder (ingredient : Sn-Cu) plating.

Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

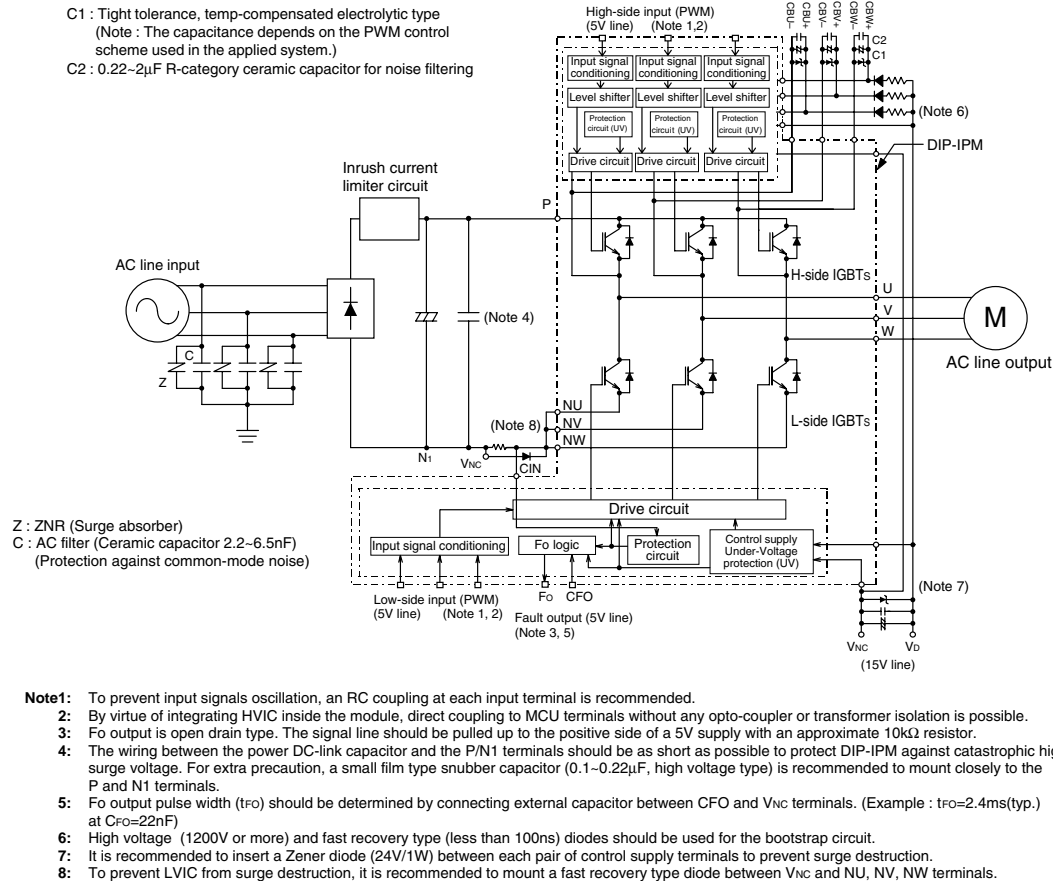
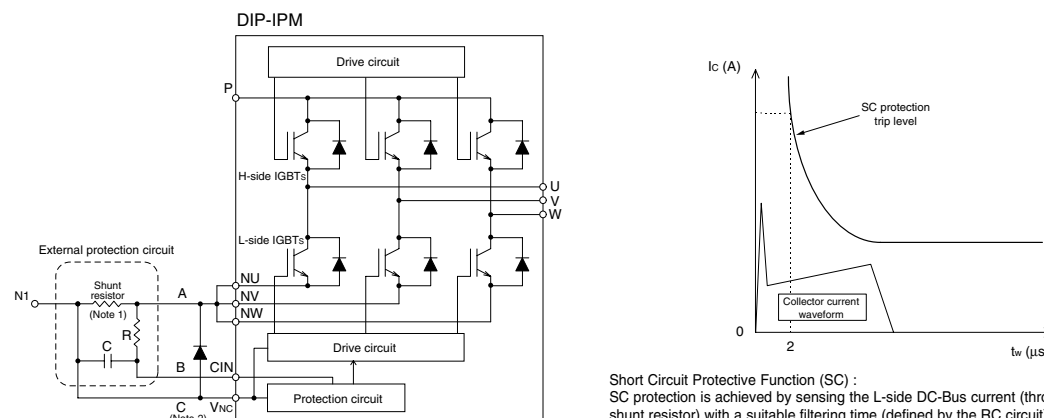


Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT



Short Circuit Protective Function (SC) :  
SC protection is achieved by sensing the L-side DC-Bus current (through the external shunt resistor) with a suitable filtering time (defined by the RC circuit).  
When the sensed shunt voltage exceeds the SC trip-level, all the L-side IGBTs are turned OFF and a fault signal (Fo) is output.  
Since the SC fault may be repetitive, it is recommended to stop the system and check the fault, when the Fo signal is received.

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TRANSFER-MOLD TYPE  
INSULATED TYPE

**MAXIMUM RATINGS** ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)

## INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V <sub>CC</sub>	Supply voltage	Applied between P-NU, NV, NW	900	V
V <sub>CC(surge)</sub>	Supply voltage (surge)	Applied between P-NU, NV, NW	1000	V
V <sub>CES</sub>	Collector-emitter voltage		1200	V
±I <sub>C</sub>	Each IGBT collector current	T <sub>c</sub> = 25°C	25	A
±I <sub>CP</sub>	Each IGBT collector current (peak)	T <sub>c</sub> = 25°C, less than 1ms	50	A
P <sub>C</sub>	Collector dissipation	T <sub>c</sub> = 25°C, per 1 chip	78.1	W
T <sub>j</sub>	Junction temperature	(Note 1)	-20~+125	°C

**Note 1** : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ T<sub>c</sub> ≤ 100°C) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to T<sub>j(ave)</sub> ≤ 125°C (@ T<sub>c</sub> ≤ 100°C).

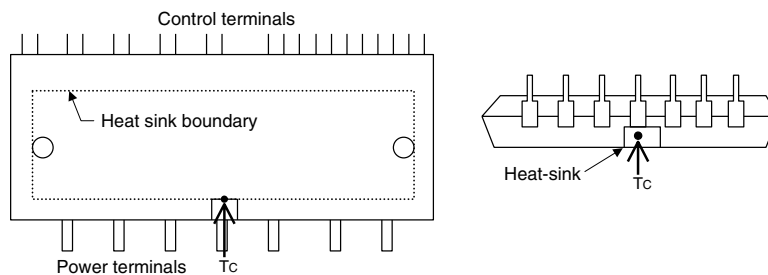
## CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V <sub>D</sub>	Control supply voltage	Applied between VP1-VPC, VN1-VNC	20	V
V <sub>DB</sub>	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
V <sub>IN</sub>	Input voltage	Applied between UP, VP, WP-VPC, UN, VN, WN-VNC	-0.5~V <sub>D</sub> +0.5	V
V <sub>FO</sub>	Fault output supply voltage	Applied between FO-VNC	-0.5~V <sub>D</sub> +0.5	V
I <sub>FO</sub>	Fault output current	Sink current at FO terminal	1	mA
V <sub>SC</sub>	Current sensing input voltage	Applied between CIN-VNC	-0.5~V <sub>D</sub> +0.5	V

## TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V <sub>CC(PROT)</sub>	Self protection supply voltage limit (short circuit protection capability)	V <sub>D</sub> = 13.5~16.5V, Inverter part T <sub>j</sub> = 125°C, non-repetitive, less than 2 μs	800	V
T <sub>C</sub>	Module case operation temperature	(Note 2)	-20~+100	°C
T <sub>stg</sub>	Storage temperature		-40~+125	°C
V <sub>iso</sub>	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	2500	V <sub>rms</sub>

**Note 2 : T<sub>C</sub> MEASUREMENT POINT**



## THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R <sub>th(j-c)Q</sub>	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	1.28	°C/W
R <sub>th(j-c)F</sub>		Inverter FWDi part (per 1/6 module)	—	—	1.70	°C/W
R <sub>th(c-f)</sub>	Contact thermal resistance	Case to fin, (per 1 module) thermal grease applied	—	—	0.047	°C/W

**Note 3:** Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIP-IPM and heat-sink.

ELECTRICAL CHARACTERISTICS (T<sub>j</sub> = 25°C, unless otherwise noted)

## INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V <sub>CE(sat)</sub>	Collector-emitter saturation voltage	V <sub>D</sub> = V <sub>DB</sub> = 15V V <sub>IN</sub> = 5V, I <sub>C</sub> = 25A	—	2.7	3.4	V
V <sub>EC</sub>	FWDi forward voltage	—I <sub>C</sub> = 25A, V <sub>IN</sub> = 0V	—	2.5	3.0	V
t <sub>on</sub>	Switching times	V <sub>CC</sub> = 600V, V <sub>D</sub> = V <sub>DB</sub> = 15V I <sub>C</sub> = 25A, T <sub>j</sub> = 125°C, V <sub>IN</sub> = 0 ↔ 5V Inductive load (upper-lower arm)	0.8	1.5	2.2	μs
t <sub>rr</sub>			—	0.3	—	μs
t <sub>c(on)</sub>			—	0.6	0.9	μs
t <sub>off</sub>			—	2.8	3.8	μs
t <sub>c(off)</sub>			—	0.6	0.9	μs
I <sub>CES</sub>	Collector-emitter cut-off current	V <sub>CE</sub> = V <sub>CES</sub>	—	—	1	mA
		T <sub>j</sub> = 125°C	—	—	10	

## CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
ID	Circuit current	VD = VDB = 15V VIN = 5V	Total of VP1-VPC, VN1-VNC	—	—	3.70	mA
			VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	—	—	1.30	mA
		VD = VDB = 15V VIN = 0V	Total of VP1-VPC, VN1-VNC	—	—	3.50	mA
			VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	—	—	1.30	mA
VFOH	Fault output voltage	VSC = 0V, FO circuit pull-up to 5V with 10kΩ		4.9	—	—	V
VFOL		VSC = 1V, IFO = 1mA		—	—	1.10	V
VSC(ref)	Short circuit trip level	TJ = 25°C, VD = 15V (Note 4)		0.43	0.48	0.53	V
IIN	Input current	VIN = 5V		0.7	1.5	2.0	mA
UVDBt	Supply circuit under-voltage protection	TJ ≤ 125°C	Trip level	10.0	—	12.0	V
UVDBr			Reset level	10.5	—	12.5	V
UVDt			Trip level	10.3	—	12.5	V
UVDr			Reset level	10.8	—	13.0	V
tFO	Fault output pulse width	CFO = 22nF (Note 5)		1.6	2.4	—	ms
Vth(on)	ON threshold voltage	Applied between UP, VP, WP-VPC, UN, VN, WN-VNC		2.0	3.0	4.2	V
Vth(off)	OFF threshold voltage			0.8	1.4	2.0	V

**Note 4 :** Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 1.7 times device current rating.

**5 :** Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width t<sub>FO</sub> depends on the capacitance value of C<sub>FO</sub> according to the following approximate equation : C<sub>FO</sub> = 9.3 × 10<sup>-6</sup> × t<sub>FO</sub> [F].

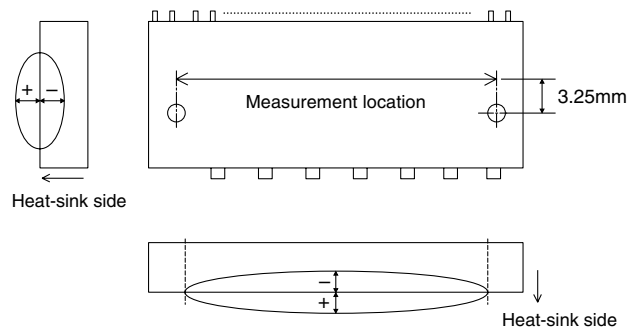
# PS22056

TRANSFER-MOLD TYPE  
INSULATED TYPE

## MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Limits			Unit
		Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4      Recommended 1.18 N·m	0.98	—	1.47	N·m
Weight		—	77	—	g
Heat-sink flatness	(Note 6)	-50	—	100	μm

### Note 6: Measurement point of heat-sink flatness



## RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
VCC	Supply voltage	Applied between P-NU, NV, NW		350	600	800	V
VD	Control supply voltage	Applied between VP1-VPC, VN1-VNC		13.5	15.0	16.5	V
VDB	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS		13.5	15.0	16.5	V
ΔVD, ΔVDB	Control supply variation			−1	—	1	V/μs
tdead	Arm shoot-through blocking time	For each input signal, Tc ≤ 100°C		3.3	—	—	μs
fPWM	PWM input frequency	Tc ≤ 100°C, Tj ≤ 125°C		—	—	15	kHz
Io	Allowable r.m.s. current	VCC = 600V, VD = 15V, fc = 15kHz P.F = 0.8, sinusoidal PWM Tj ≤ 125°C, Tc ≤ 100°C		—	—	9.2	Arms
PWIN(on)	Minimum input pulse width	(Note 8)		1.5	—	—	μs
PWIN(off)		350 ≤ VCC ≤ 800V, 13.5 ≤ VD ≤ 16.5V, 13.5 ≤ VDB ≤ 16.5V, −20°C ≤ Tc ≤ 100°C, N line wiring inductance less than 10nH	Ic ≤ 25A	2.1	—	—	
		(Note 9)	25 < Ic ≤ 42.5A	2.3	—	—	
VNC	VNC variation	Between VNC-NU, NV, NW (including surge)		−5.0	—	5.0	V

**Note 7 :** The output r.m.s. current value depends on the actual application conditions.

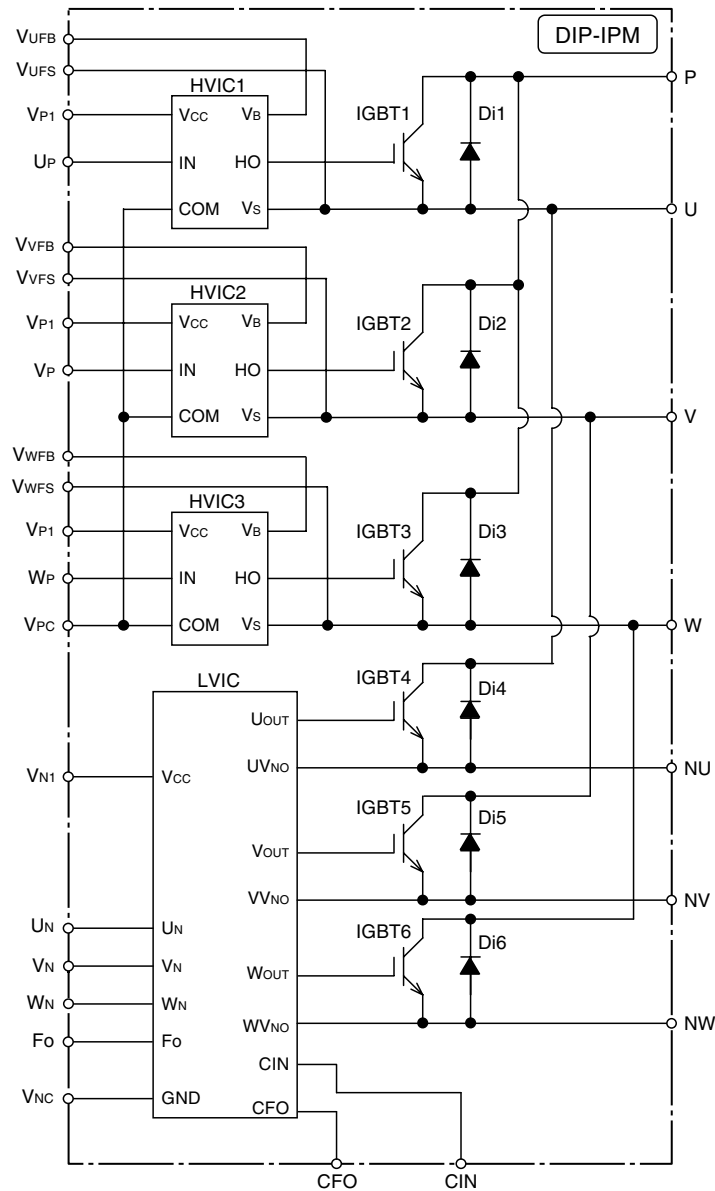
**8 :** DIP-IPM might not make response to the input on signal with pulse width less than PWIN (on).

**9 :** DIP-IPM might not make response or work properly if the input off signal pulse width is less than PWIN (off).

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TRANSFER-MOLD TYPE  
INSULATED TYPE

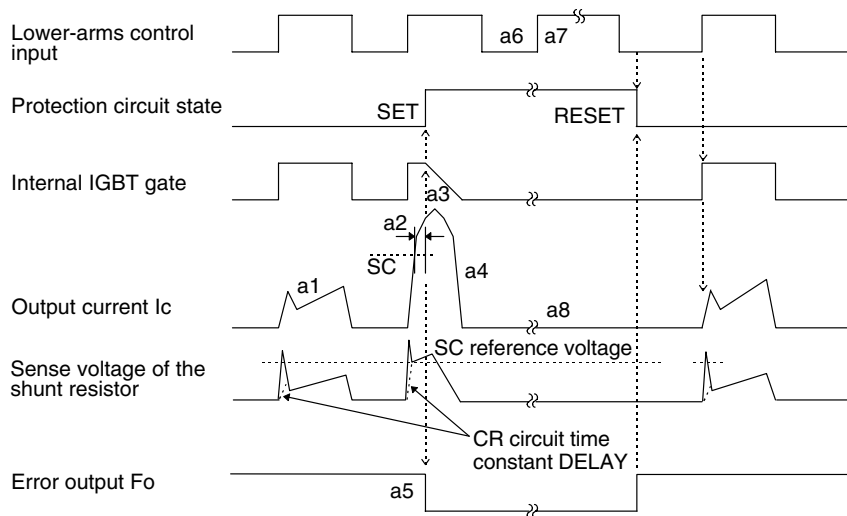
Fig. 4 THE DIP-IPM INTERNAL CIRCUIT



**Fig. 5 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS**

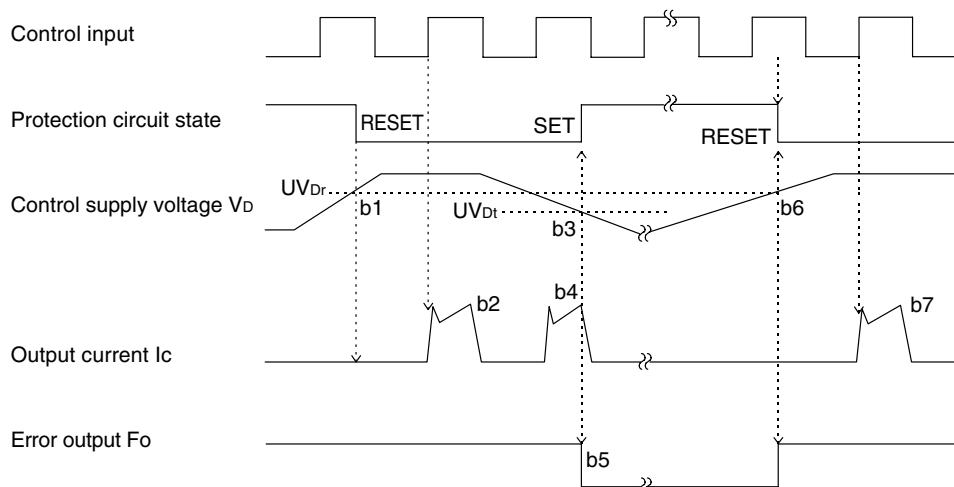
**[A] Short-Circuit Protection (Lower-arms only with the external shunt resistor and CR filter)**

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
- a3. IGBT gate hard interruption.
- a4. IGBT turns OFF.
- a5. Fo output with a fixed pulse width determined by the external capacitor C<sub>FO</sub>.
- a6. Input = "L" : IGBT OFF
- a7. Input = "H" :
- a8. IGBT OFF state in spite of input "H".



**[B] Under-Voltage Protection (Lower-arm, UVd)**

- b1. Control supply voltage rising : After the voltage level reaches UV<sub>Dr</sub>, the circuits start to operate when next input is applied.
- b2. Normal operation : IGBT ON and carrying current.
- b3. Under voltage trip (UV<sub>Dt</sub>).
- b4. IGBT OFF in spite of control input condition.
- b5. Fo keeps output during the UV period, however, Fo pulse is not less than the fixed width for very short UV interval.
- b6. Under voltage reset (UV<sub>Dr</sub>).
- b7. Normal operation : IGBT ON and carrying current.



### [C] Under-Voltage Protection (Upper-side, UVDB)

- c1. Control supply voltage rises : After the voltage reaches UVDBr, the circuits start to operate when next input is applied.
- c2. Normal operation : IGBT ON and carrying current.
- c3. Under voltage trip (UVDBt).
- c4. IGBT OFF in spite of control input signal level, but there is no Fo signal output.
- c5. Under voltage reset (UVDBr).
- c6. Normal operation : IGBT ON and carrying current.

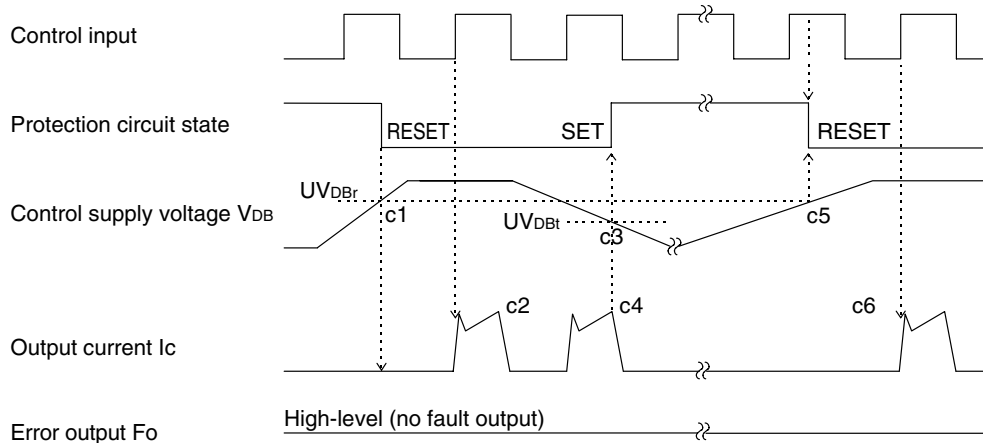
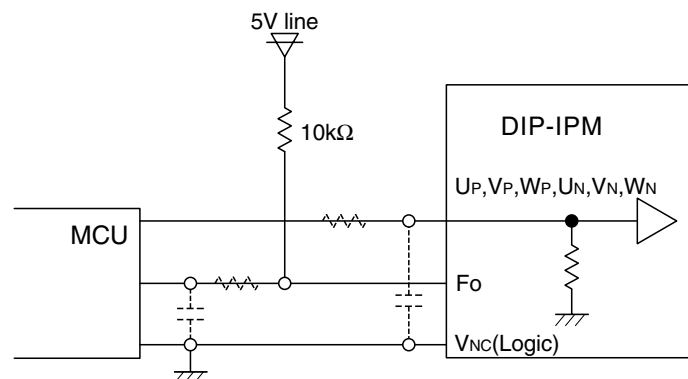
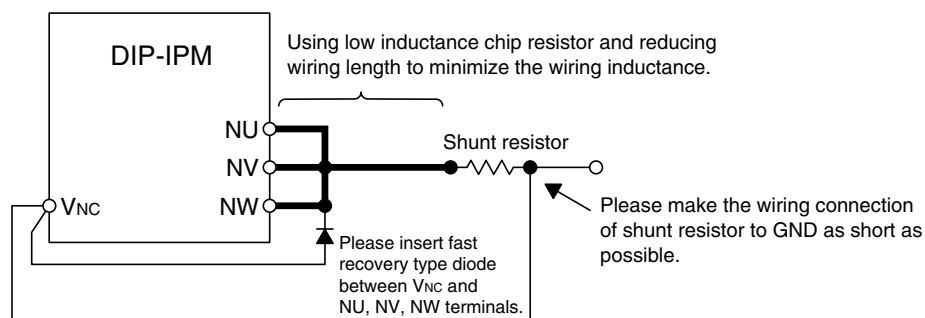


Fig. 6 MCU I/O INTERFACE CIRCUIT



**Note :** RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board.  
The DIP-IPM input signal section integrates a 2.5kΩ(min) pull-down resistor. Therefore, when using a external filtering resistor, pay attention to the turn-on threshold voltage requirement.

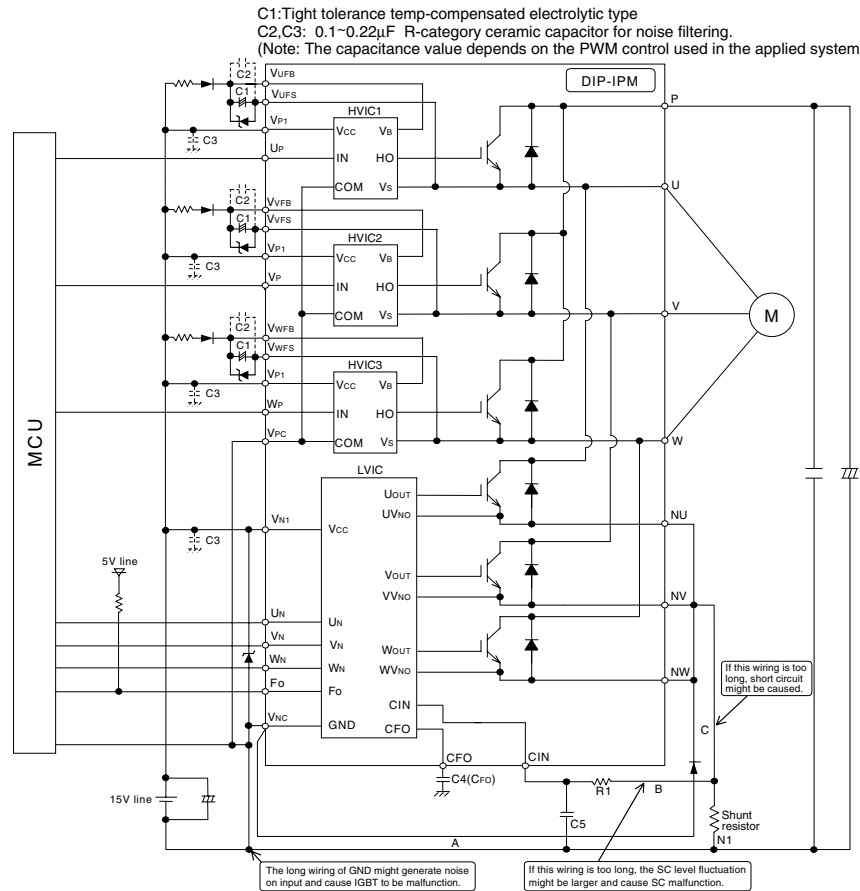
Fig. 7 WIRING CONNECTION WITH 1 SHUNT RESISTOR



For 3 shunt resistors connection, please refer to Fig.9.



Fig. 8 AN EXAMPLE OF TYPICAL DIP-IPM APPLICATION CIRCUIT WITH 1 SHUNT RESISTOR



- Note 1:** To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)
- 2:** By virtue of integrating HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible.
- 3:** Fo output is open drain type. The signal line should be pulled up to the positive side of a 5V supply with an approximate 10k $\Omega$  resistor.
- 4:** Fo output pulse width (tFO) should be determined by connecting external capacitor C4 between CFO and Vnc terminals. (Example : tFO=2.4ms(typ.) at CFO=22nF)
- 5:** Input signal is High-Active type. There is a 2.5k $\Omega$  (Min.) resistor inside IC to pull down each input signal line to GND. When employing RC coupling circuits at each input, set up RC couple such that input signal agree with turn-off/turn-on threshold voltage.
- 6:** To prevent errors of the protection function, the wiring of A, B, C should be as short as possible.
- 7:** The time constant R5C1 of the protection circuit should be selected in the range of 1.5~2 $\mu$ s. SC interrupting time might vary with the wiring pattern.
- 8:** All capacitors should be mounted as close to the terminals of the DIP-IPM as possible.
- 9:** To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 terminals should be as short as possible. Generally a 0.1~0.22 $\mu$ F snubber between the P&N1 terminals is recommended.
- 10:** It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
- 11:** To prevent LVIC from surge destruction, it is recommended to mount a fast recovery type diode between Vnc and NU, NV, NW terminals.

Fig. 9 EXAMPLE OF EXTERNAL PROTECTION CIRCUIT WITH 3 SHUNT RESISTORS

