

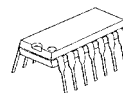


## Headphone Amplifier with Electronic Volume

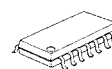
### ■ GENERAL DESCRIPTION

**NJW1109** is a headphone amplifier with electronic volume. It includes widely gain adjustable volume, +20 to -80 dB, and mute function. These are controlled by I<sup>2</sup>C bus. The **NJW1109** is suitable for headphone output on TV set.

### ■ PACKAGE OUTLINE



NJW1109D



NJW1109M

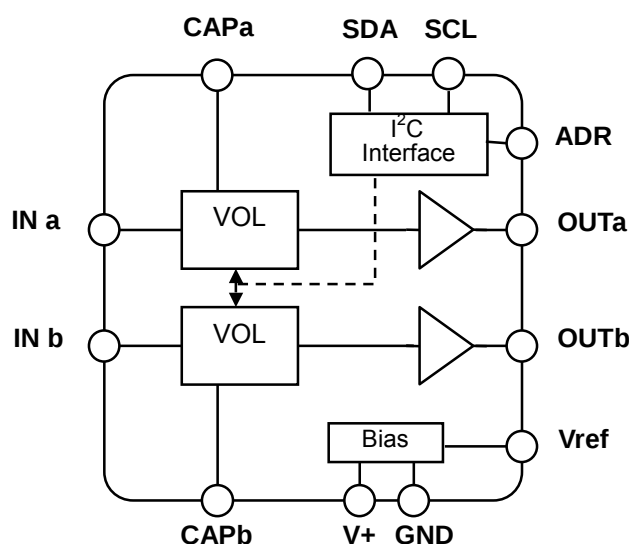


NJW1109V

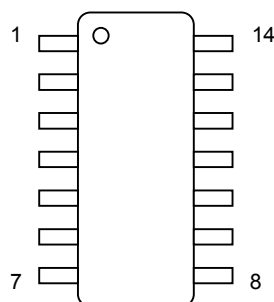
### ■ FEATURES

- Operating Voltage 7.5 to 10 V
- Electronic Volume +20dB to -80dB / 0.5dB step, Mute
- I<sup>2</sup>C Bus Interface
- Bi-CMOS Technology
- Package Outline DIP14, DMP14, SSOP14

### ■ BLOCK DIAGRAM



### ■ PIN FUNCTION



| No. | SYMBOL | FUNCTION                                                         | No. | SYMBOL | FUNCTION                                                        |
|-----|--------|------------------------------------------------------------------|-----|--------|-----------------------------------------------------------------|
| 1   | V+     | Power Supply                                                     | 8   | SCL    | I <sup>2</sup> C Bus Clock Input                                |
| 2   | OUTb   | Bch Output                                                       | 9   | Vref   | Reference voltage stabilized capacitor connect terminal         |
| 3   | N.C.   | No Connect                                                       | 10  | INa    | Ach Input                                                       |
| 4   | CAPb   | Balance control click noise absorbing capacitor connect terminal | 11  | CAPa   | Volume control click noise absorbing capacitor connect terminal |
| 5   | INb    | Bch Input                                                        | 12  | N.C.   | No Connect                                                      |
| 6   | ADR    | I <sup>2</sup> C Bus Slave Address Select                        | 13  | OUTa   | Ach Output                                                      |
| 7   | SDA    | I <sup>2</sup> C Bus Data Input                                  | 14  | GND    | Ground                                                          |

## ■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

| PARAMETER                   | SYMBOL         | RATING                                       | UNIT |
|-----------------------------|----------------|----------------------------------------------|------|
| Supply Voltage              | V <sup>+</sup> | 12                                           | V    |
| Power Dissipation           | P <sub>D</sub> | DIP14 : 500<br>DMP14 : 500*<br>SSOP14 : 440* | mW   |
| Operating Temperature Range | Topr           | -20 to +75                                   | °C   |
| Storage Temperature Range   | Tstg           | -40 to +125                                  | °C   |

\*(Note) EIA/JEDEC STANDARD Test board(76.2 x 114.3 x 1.6mm, 2layers, FR-4)mounting

## ■ ELECTRICAL CHARACTERISTICS

(V<sup>+</sup>=9V, V<sub>IN</sub>=-20dBV, f=1kHz, R<sub>L</sub>=100Ω, VOL = 0dB, Ta=25°C)

### ●POWER SUPPLY

| PARAMETER         | SYMBOL           | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-------------------|------------------|----------------|------|------|------|------|
| Operating Voltage | V <sup>+</sup>   |                | 7.5  | 9    | 10   | V    |
| Operating Current | I <sub>CC</sub>  | No Signal      | -    | 5    | 8    | mA   |
| Reference Voltage | V <sub>REF</sub> |                | 4.0  | 4.5  | 5.0  | V    |

### ●AMPLIFIER

| PARAMETER                     | SYMBOL            | TEST CONDITION                  | MIN.         | TYP.          | MAX.        | UNIT           |
|-------------------------------|-------------------|---------------------------------|--------------|---------------|-------------|----------------|
| Volume Maximum Gain           | G <sub>VMAX</sub> | VOL = +20dB setting             | 18           | 20            | 22          | dB             |
| Volume Minimum Gain           | G <sub>VMIN</sub> | VOL = -80dB setting             |              | -80           |             |                |
| Voltage Gain Channel Balance  | ΔGv               | VOL = 0dB setting               | -1.5         | 0             | 1.5         | dB             |
| Maximum Input Voltage         | V <sub>IM</sub>   | VOL = -10dB setting<br>THD=3%   | 8.9<br>(2.8) | 9.5<br>(3.0)  | -           | dBV<br>(Vrms)  |
| Output Power                  | P <sub>O</sub>    | VOL = 10dB, THD=10%             | 70           | 100           | -           | mW             |
| Total Harmonic Distortion     | THD               | VOL = 0dB setting               | -            | 0.1           | 1           | %              |
| Channel Separation            | CS                | Rg=600Ω, Vin = 0dBV             | 70           | 80            | -           | dB             |
| Mute Level                    | Mute              | VOL = Mute, Vin = 0dBV          | -            | -100          | -90         | dB             |
| Output Noise Voltage 1        | V <sub>NO1</sub>  | Rg=0Ω, A-Weighted               | -            | -95<br>(18)   | -85<br>(56) | dBV<br>(μVrms) |
| Output Noise Voltage 2        | V <sub>NO2</sub>  | VOL = Mute<br>Rg=0Ω, A-Weighted | -            | -105<br>(5.6) | -95<br>(18) | dBV<br>(μVrms) |
| Power Supply Ripple Rejection | PSRR              | Vripple=-20dBV, Rg=0Ω           | -            | 70            | -           | dB             |

### ●CONTROL

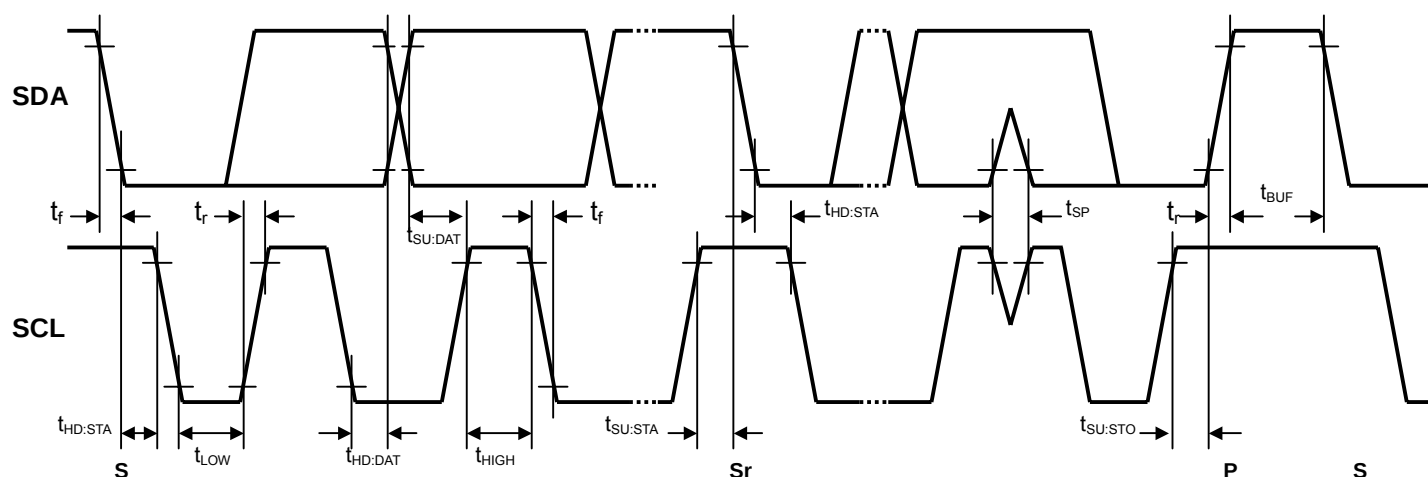
| PARAMETER                | SYMBOL            | TEST CONDITION           | MIN.              | TYP. | MAX. | UNIT |
|--------------------------|-------------------|--------------------------|-------------------|------|------|------|
| High Level Input Voltage | V <sub>ADRH</sub> | High : Slave Address 84H | V <sup>+</sup> /2 | -    | -    | V    |
| Low Level Input Voltage  | V <sub>ADRL</sub> | Low : Slave Address 80H  | -                 | -    | 1.0  | V    |

## ■ I<sup>2</sup>C BUS CHARACTERISTICS (SDA, SCL)

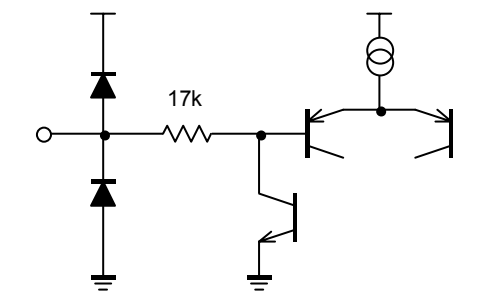
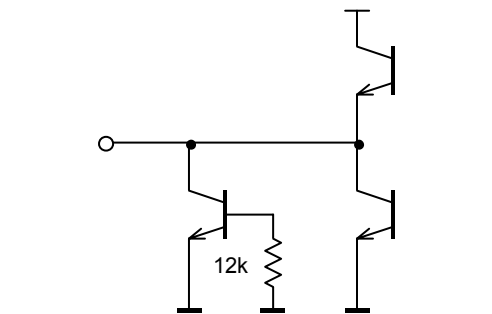
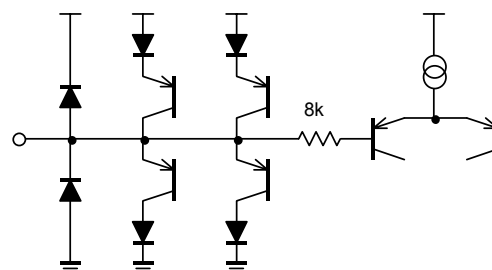
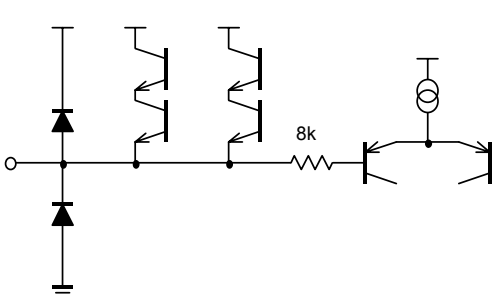
I<sup>2</sup>C BUS Load Conditions: Pull up resistance 4k $\Omega$  (Connected to +5V), Load capacitance 200pF (Connected to GND)

| PARAMETER                                                                                             | SYMBOL       | MIN.        | TYP. | MAX. | UNIT    |
|-------------------------------------------------------------------------------------------------------|--------------|-------------|------|------|---------|
| Low Level Input Voltage                                                                               | $V_{IL}$     | 0.0         | -    | 1.5  | V       |
| High Level Input Voltage                                                                              | $V_{IH}$     | 2.5         | -    | 5.0  | V       |
| Hysteresis of Schmitt trigger inputs                                                                  | $V_{hys}$    | 0.25        | -    | -    | V       |
| LOW level output voltage (3mA at SDA pin)                                                             | $V_{OL}$     | 0           | -    | 0.4  | V       |
| Output fall time from $V_{IHmin}$ to $V_{ILmax}$ with a bus capacitance from 10pF to 400pF            | $t_{of}$     | $20+0.1C_b$ | -    | 250  | ns      |
| Pulse width of spikes which must be suppressed by the input filter                                    | $t_{SP}$     | 0           | -    | 50   | ns      |
| Input current each I/O pin with an input voltage between 0.1V <sub>DD</sub> and 0.9V <sub>DDmax</sub> | $I_i$        | -10         | -    | 10   | $\mu$ A |
| Capacitance for each I/O pin                                                                          | $C_i$        | -           | -    | 10   | pF      |
| SCL clock frequency                                                                                   | $f_{SCL}$    | -           | -    | 400  | kHz     |
| Hold time (repeated) START condition.                                                                 | $t_{HD:STA}$ | 0.6         | -    | -    | $\mu$ s |
| LOW period of the SCL clock                                                                           | $t_{LOW}$    | 1.3         | -    | -    | $\mu$ s |
| HIGH period of the SCL clock                                                                          | $t_{HIGH}$   | 0.6         | -    | -    | $\mu$ s |
| Set-up time for a repeated START condition                                                            | $t_{SU:STA}$ | 0.6         | -    | -    | $\mu$ s |
| Data hold time                                                                                        | $t_{HD:DAT}$ | -           | -    | 0.9  | $\mu$ s |
| Data set-up time                                                                                      | $t_{SU:DAT}$ | 100         | -    | -    | ns      |
| Rise time of both SDA and SCL signals                                                                 | $t_r$        | -           | -    | 300  | ns      |
| Fall time of both SDA and SCL signals                                                                 | $t_f$        | -           | -    | 300  | ns      |
| Set-up time for STOP condition                                                                        | $t_{SU:STO}$ | 0.6         | -    | -    | $\mu$ s |
| Bus free time between a STOP and START condition                                                      | $t_{BUF}$    | 1.3         | -    | -    | $\mu$ s |
| Capacitive load for each bus line                                                                     | $C_b$        | -           | -    | 400  | pF      |
| Noise margin at the LOW level                                                                         | $V_{nL}$     | 0.5         | -    | -    | V       |
| Noise margin at the HIGH level                                                                        | $V_{nH}$     | 1           | -    | -    | V       |

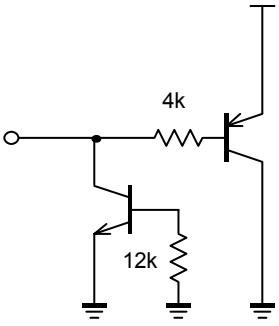
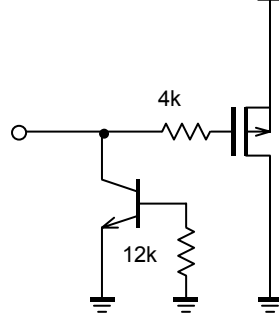
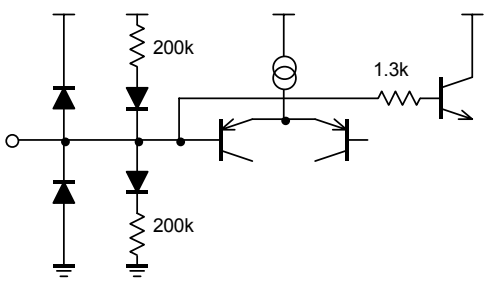
$C_b$  ; total capacitance of one bus line in pF.



■TERMINAL DESCRIPTION

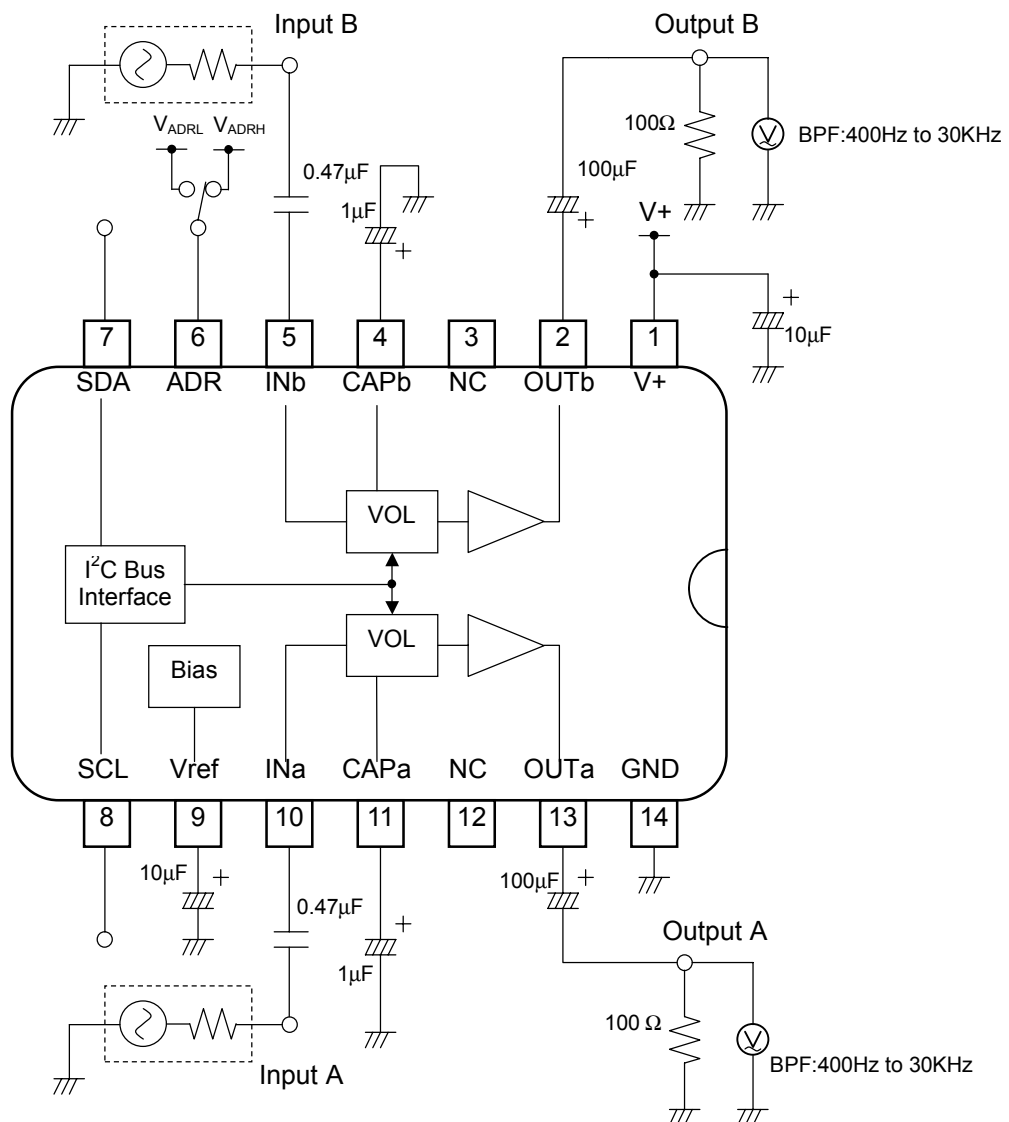
| No.     | SYMBOL       | FUNCTION                                                         | EQUIVALENT CIRCUIT                                                                   | VOLTAGE |
|---------|--------------|------------------------------------------------------------------|--------------------------------------------------------------------------------------|---------|
| 5<br>10 | INb<br>INa   | Bch Input<br>Ach Input                                           |    | V+/2    |
| 2<br>13 | OUTb<br>OUTa | Bch Output<br>Ach Output                                         |   | V+/2    |
| 4       | CAPb         | Balance control click noise absorbing capacitor connect terminal |  | 3.1V    |
| 11      | CAPa         | Volume control click noise absorbing capacitor connect terminal  |  | 3.8V    |

## ■ TERMINAL DESCRIPTION

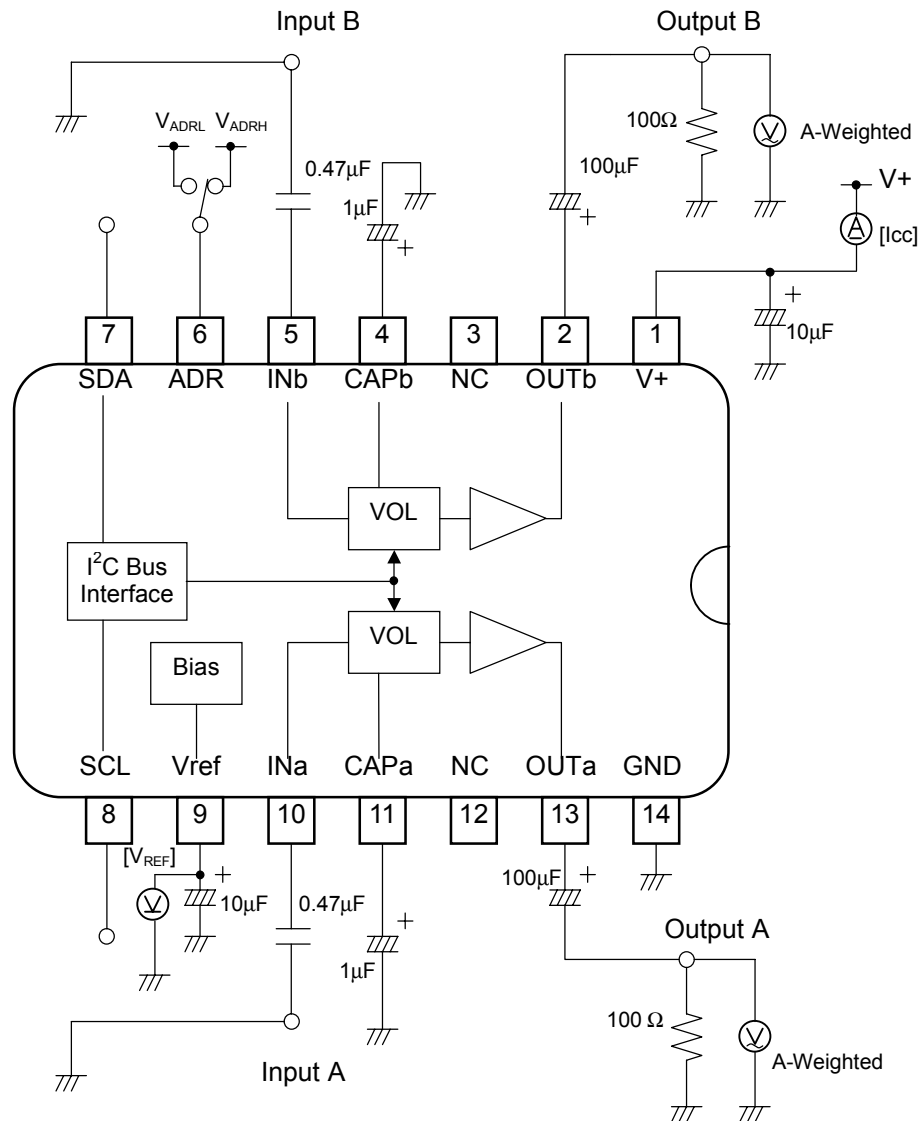
| No.    | SYMBOL     | FUNCTION                                                            | EQUIVALENT CIRCUIT                                                                   | VOLTAGE |
|--------|------------|---------------------------------------------------------------------|--------------------------------------------------------------------------------------|---------|
| 6      | ADR        | I <sup>2</sup> C Bus Slave Address Select                           |    | -       |
| 7<br>8 | SDA<br>SCL | I <sup>2</sup> C Bus Data Input<br>I <sup>2</sup> C Bus Clock Input |   | -       |
| 9      | Vref       | Reference voltage stabilized capacitor connect terminal             |  | V+/2    |
| 1      | V+         | Power Supply                                                        | -                                                                                    | -       |
| 14     | GND        | Ground                                                              | -                                                                                    | -       |

## ■ TEST CIRCUIT

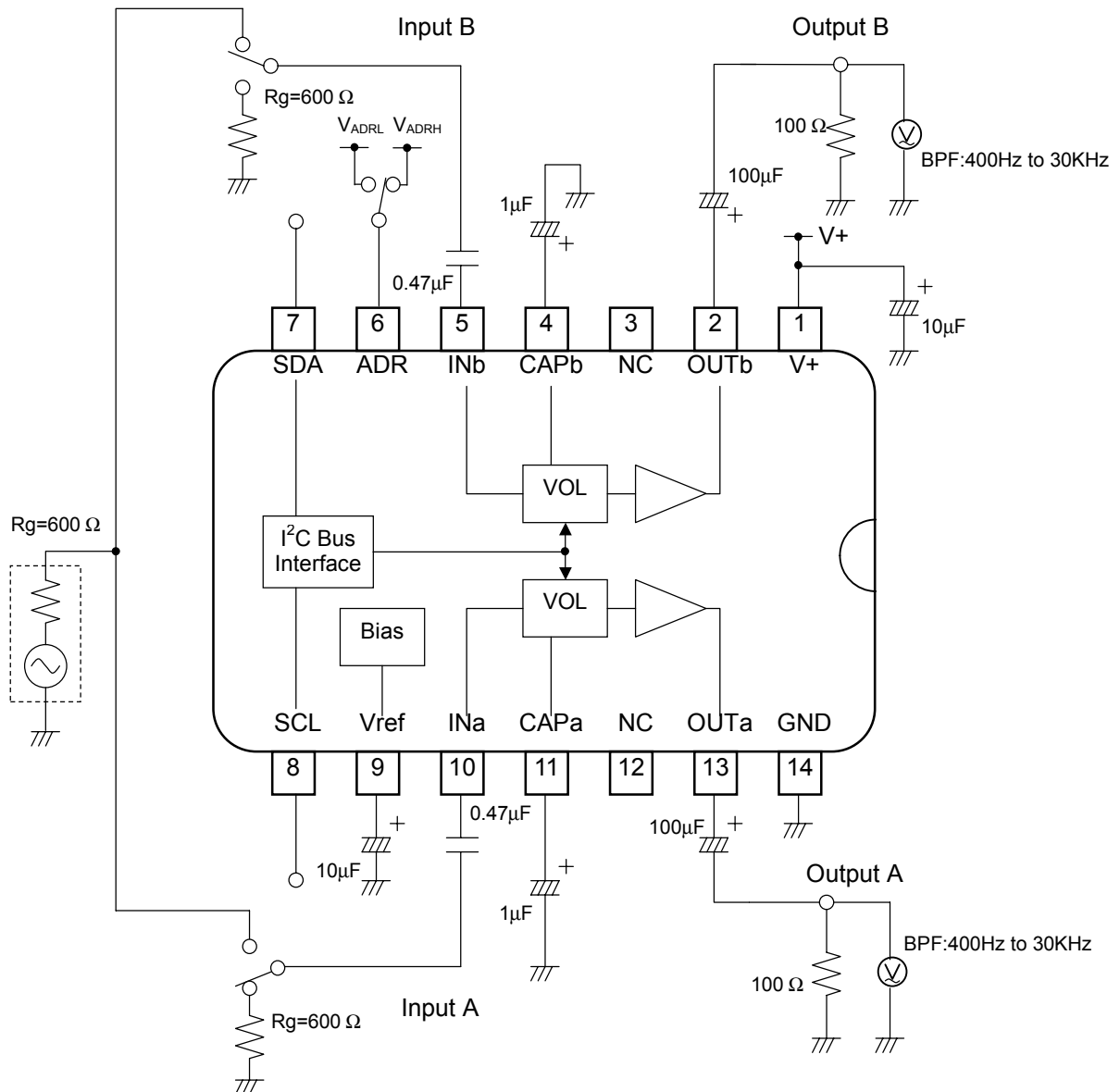
### TEST CIRCUIT 1 ( $G_{VMAX}$ , $G_{VMIN}$ , $\Delta G_V$ , $V_{IM}$ , $P_O$ , THD, Mute)



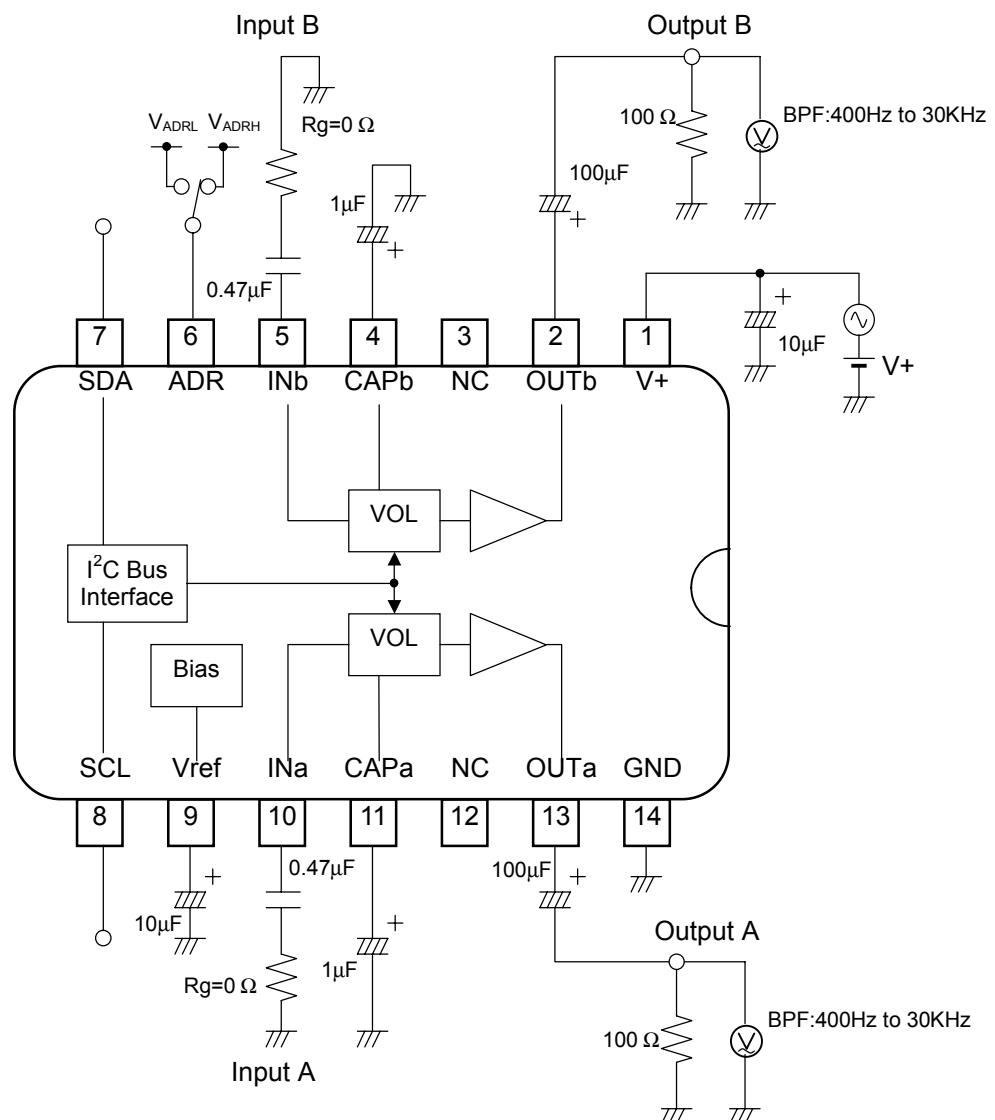
TEST CIRCUIT 2 ( $I_{CC}$ ,  $V_{REF}$ ,  $V_{NO1}$ ,  $V_{NO2}$ )



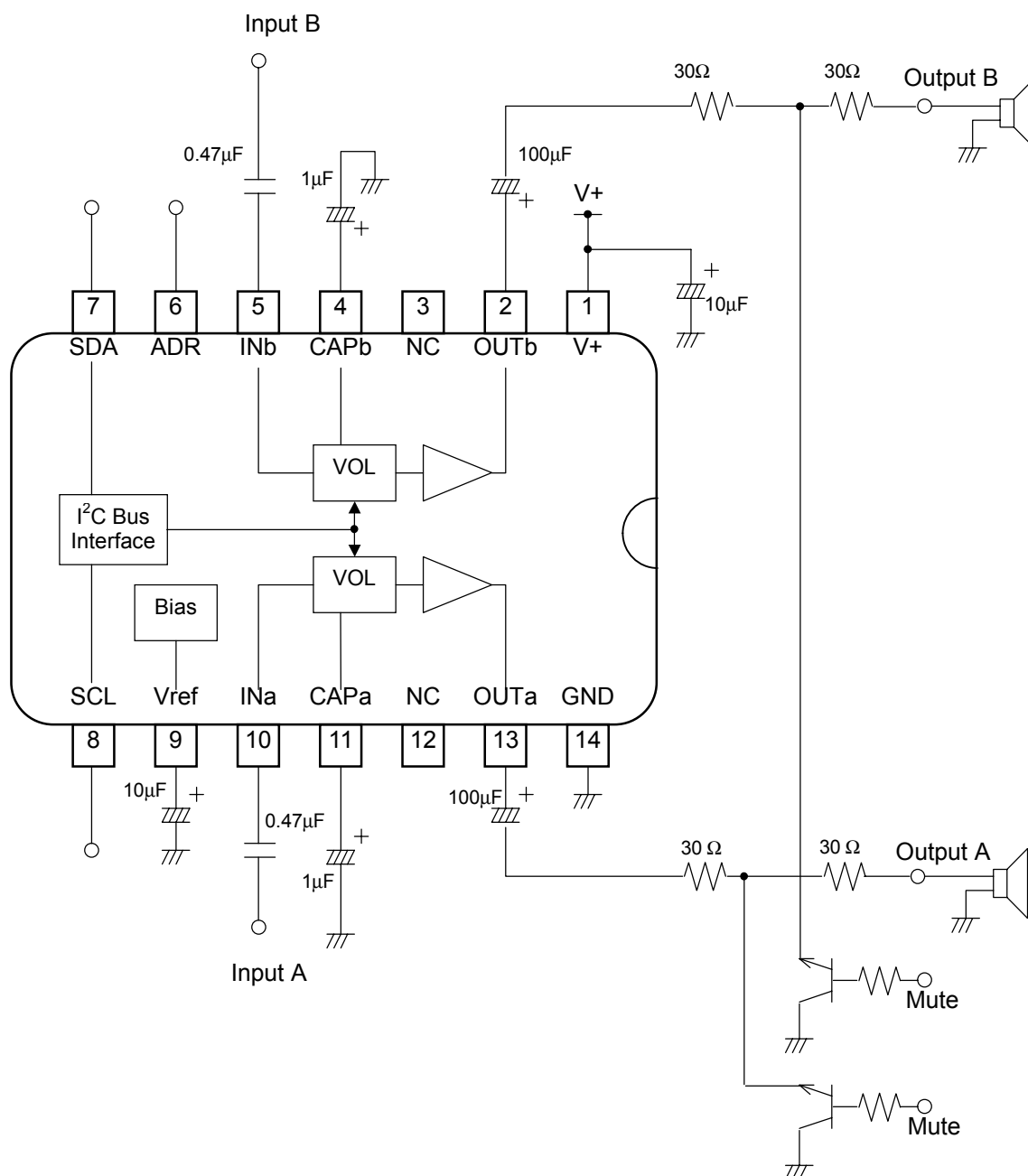
## TEST CIRCUIT 3 (CS)



TEST CIRCUIT 4 (PSRR)

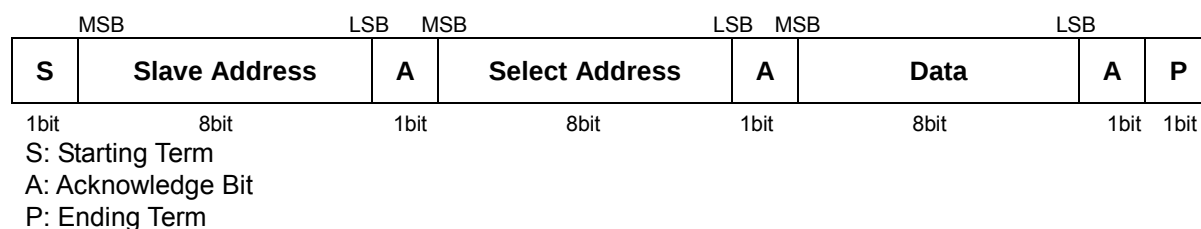


## ■ APPLICATION CIRCUIT



## ■ DEFINITION OF I<sup>2</sup>C REGISTER

### ● I<sup>2</sup>C BUS FORMAT



### ● SLAVE ADDRESS

|   |     |   |   |   |   |   |     |                                     |
|---|-----|---|---|---|---|---|-----|-------------------------------------|
|   | MSB |   |   |   |   |   | LSB |                                     |
| 1 | 0   | 0 | 0 | 0 | 0 | 0 | 0   | 80H (ADR = Low)<br>84H (ADR = High) |
| 1 | 0   | 0 | 0 | 0 | 1 | 0 | 0   |                                     |

### ● SELECT ADDRESS

The auto-increment function cycles the select address as follows.

00H→01H→00H

| Select Address | BIT |     |    |    |    |    |            |    |
|----------------|-----|-----|----|----|----|----|------------|----|
|                | D7  | D6  | D5 | D4 | D3 | D2 | D1         | D0 |
| 00H            | VOL |     |    |    |    |    |            |    |
| 01H            | CHS | BAL |    |    |    |    | Don't Care |    |

## ■ CONTROL REGISTER DEFAULT VALUE

Control register default value is all "0".

| Select Address | BIT |    |    |    |    |    |    |    |
|----------------|-----|----|----|----|----|----|----|----|
|                | D7  | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00H            | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 01H            | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

## ■ CONTROL COMMAND TABLE

### a) Master Volume

| Select Address | BIT |    |    |    |    |    |    |    |
|----------------|-----|----|----|----|----|----|----|----|
|                | D7  | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00H            | VOL |    |    |    |    |    |    |    |

#### ●VOL : Master Volume

Attenuation level : +20 to -80dB(0.5dB/step), MUTE

### b) Balance

| Select Address | BIT |     |    |    |    |    |            |    |
|----------------|-----|-----|----|----|----|----|------------|----|
|                | D7  | D6  | D5 | D4 | D3 | D2 | D1         | D0 |
| 01H            | CHS | BAL |    |    |    |    | Don't Care |    |

#### ●CHS : Balance channel select

"0" : Ach "Bch is attenuated"                      "1" : Bch "Ach is attenuated"

#### ●BAL : Ach and Bch Ach and Bch Balance

Balance Level : 0 to -30dB (1dB/Step) , MUTE

## ■CONTROL COMMAND TABLE

a) Master Volume (Select Address: 00H) Volume level : +20 to -80dB(0.5dB/step), MUTE

| Gain(dB) | HEX | VOL |     |     |     |     |     |     |     |
|----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|          |     | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
| 20       | FF  | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| 19.5     | FE  | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 0   |
| 19       | FD  | 1   | 1   | 1   | 1   | 1   | 1   | 0   | 1   |
| 18.5     | FC  | 1   | 1   | 1   | 1   | 1   | 1   | 0   | 0   |
| 18       | FB  | 1   | 1   | 1   | 1   | 1   | 0   | 1   | 1   |
| 17.5     | FA  | 1   | 1   | 1   | 1   | 1   | 0   | 1   | 0   |
| 17       | F9  | 1   | 1   | 1   | 1   | 1   | 0   | 0   | 1   |
| 16.5     | F8  | 1   | 1   | 1   | 1   | 1   | 0   | 0   | 0   |
| 16       | F7  | 1   | 1   | 1   | 1   | 0   | 1   | 1   | 1   |
| 15.5     | F6  | 1   | 1   | 1   | 1   | 0   | 1   | 1   | 0   |
| 15       | F5  | 1   | 1   | 1   | 1   | 0   | 1   | 0   | 1   |
| 14.5     | F4  | 1   | 1   | 1   | 1   | 0   | 1   | 0   | 0   |
| 14       | F3  | 1   | 1   | 1   | 1   | 0   | 0   | 1   | 1   |
| 13.5     | F2  | 1   | 1   | 1   | 1   | 0   | 0   | 1   | 0   |
| 13       | F1  | 1   | 1   | 1   | 1   | 0   | 0   | 0   | 1   |
| 12.5     | F0  | 1   | 1   | 1   | 1   | 0   | 0   | 0   | 0   |
| 12       | EF  | 1   | 1   | 1   | 0   | 1   | 1   | 1   | 1   |
| 11.5     | EE  | 1   | 1   | 1   | 0   | 1   | 1   | 1   | 0   |
| 11       | ED  | 1   | 1   | 1   | 0   | 1   | 1   | 0   | 1   |
| 10.5     | EC  | 1   | 1   | 1   | 0   | 1   | 1   | 0   | 0   |
| 10       | EB  | 1   | 1   | 1   | 0   | 1   | 0   | 1   | 1   |
| 9.5      | EA  | 1   | 1   | 1   | 0   | 1   | 0   | 1   | 0   |
| 9        | E9  | 1   | 1   | 1   | 0   | 1   | 0   | 0   | 1   |
| 8.5      | E8  | 1   | 1   | 1   | 0   | 1   | 0   | 0   | 0   |
| 8        | E7  | 1   | 1   | 1   | 0   | 0   | 1   | 1   | 1   |
| 7.5      | E6  | 1   | 1   | 1   | 0   | 0   | 1   | 1   | 0   |
| 7        | E5  | 1   | 1   | 1   | 0   | 0   | 1   | 0   | 1   |
| 6.5      | E4  | 1   | 1   | 1   | 0   | 0   | 1   | 0   | 0   |
| 6        | E3  | 1   | 1   | 1   | 0   | 0   | 0   | 1   | 1   |
| 5.5      | E2  | 1   | 1   | 1   | 0   | 0   | 0   | 1   | 0   |
| 5        | E1  | 1   | 1   | 1   | 0   | 0   | 0   | 0   | 1   |
| 4.5      | E0  | 1   | 1   | 1   | 0   | 0   | 0   | 0   | 0   |
| 4        | DF  | 1   | 1   | 0   | 1   | 1   | 1   | 1   | 1   |
| 3.5      | DE  | 1   | 1   | 0   | 1   | 1   | 1   | 1   | 0   |
| 3        | DD  | 1   | 1   | 0   | 1   | 1   | 1   | 0   | 1   |
| ...      | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| -79.5    | 38  | 0   | 0   | 1   | 1   | 1   | 0   | 0   | 0   |
| -80      | 37  | 0   | 0   | 1   | 1   | 0   | 1   | 1   | 1   |
| ...      | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| Mute     | 00  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |

b) Balance (Select Address: 01H) Balance level : 0 to -30dB(1dB/step), MUTE

| Channel Setting (CHS) | D7 |
|-----------------------|----|
| Attenuated Bch Gain   | 0  |
| Attenuated Ach Gain   | 1  |

| Gain(dB) | BAL |    |    |    |    |
|----------|-----|----|----|----|----|
|          | D6  | D5 | D4 | D3 | D2 |
| 0        | 0   | 0  | 0  | 0  | 0  |
| -1       | 0   | 0  | 0  | 0  | 1  |
| -2       | 0   | 0  | 0  | 1  | 0  |
| -3       | 0   | 0  | 0  | 1  | 1  |
| -4       | 0   | 0  | 1  | 0  | 0  |
| -5       | 0   | 0  | 1  | 0  | 1  |
| -6       | 0   | 0  | 1  | 1  | 0  |
| -7       | 0   | 0  | 1  | 1  | 1  |
| -8       | 0   | 1  | 0  | 0  | 0  |
| -9       | 0   | 1  | 0  | 0  | 1  |
| -10      | 0   | 1  | 0  | 1  | 0  |
| -11      | 0   | 1  | 0  | 1  | 1  |
| -12      | 0   | 1  | 1  | 0  | 0  |
| -13      | 0   | 1  | 1  | 0  | 1  |
| -14      | 0   | 1  | 1  | 1  | 0  |
| -15      | 0   | 1  | 1  | 1  | 1  |
| -16      | 1   | 0  | 0  | 0  | 0  |
| -17      | 1   | 0  | 0  | 0  | 1  |
| -18      | 1   | 0  | 0  | 1  | 0  |
| -19      | 1   | 0  | 0  | 1  | 1  |
| -20      | 1   | 0  | 1  | 0  | 0  |
| -21      | 1   | 0  | 1  | 0  | 1  |
| -22      | 1   | 0  | 1  | 1  | 0  |
| -23      | 1   | 0  | 1  | 1  | 1  |
| -24      | 1   | 1  | 0  | 0  | 0  |
| -25      | 1   | 1  | 0  | 0  | 1  |
| -26      | 1   | 1  | 0  | 1  | 0  |
| -27      | 1   | 1  | 0  | 1  | 1  |
| -28      | 1   | 1  | 1  | 0  | 0  |
| -29      | 1   | 1  | 1  | 0  | 1  |
| -30      | 1   | 1  | 1  | 1  | 0  |
| MUTE     | 1   | 1  | 1  | 1  | 1  |

## ■NOTE

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