

## TC74ACT373P, TC74ACT373F, TC74ACT373FW, TC74ACT373FT

### Octal D-Type Latch with 3-State Output

The TC74ACT373 is an advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

These 8-bit D-type latches are controlled by a latch enable ( $\overline{LE}$ ) and a output enable input ( $\overline{OE}$ ).

When the ( $\overline{OE}$ ) input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

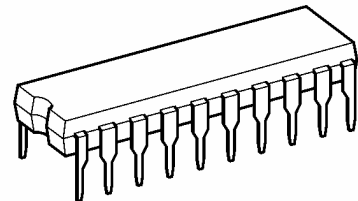
- High speed:  $t_{pd} = 5.2 \text{ ns (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 8 \mu\text{A (max)}$  at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs:  $V_{IL} = 0.8 \text{ V (max)}$   
 $V_{IH} = 2.0 \text{ V (min)}$
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 24 \text{ mA (min)}$   
Capability of driving  $50 \Omega$  transmission lines.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74F373

#### Weight

DIP20-P-300-2.54A	: 1.30 g (typ.)
SOP20-P-300-1.27A	: 0.22 g (typ.)
SOP20-P-300-1.27	: 0.22 g (typ.)
SOL20-P-300-1.27	: 0.46 g (typ.)
TSSOP20-P-0044-0.65A	: 0.08 g (typ.)

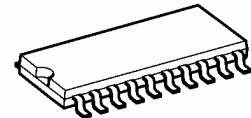
Note: xxxFW (JEDEC SOP) is not available in Japan.

TC74ACT373P

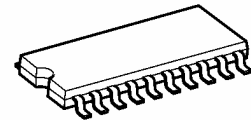


DIP20-P-300-2.54A

TC74ACT373F

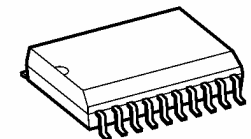


SOP20-P-300-1.27A



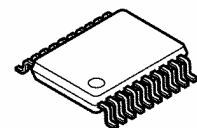
SOP20-P-300-1.27

TC74ACT373FW



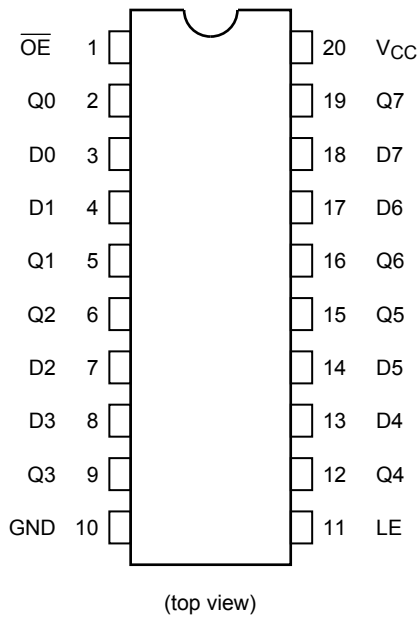
SOL20-P-300-1.27

TC74ACT373FT

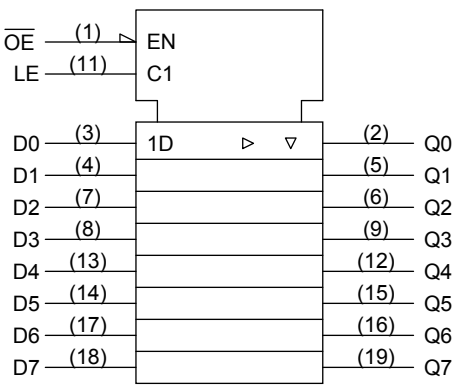


TSSOP20-P-0044-0.65A

Pin Assignment



IEC Logic Symbol



Truth Table

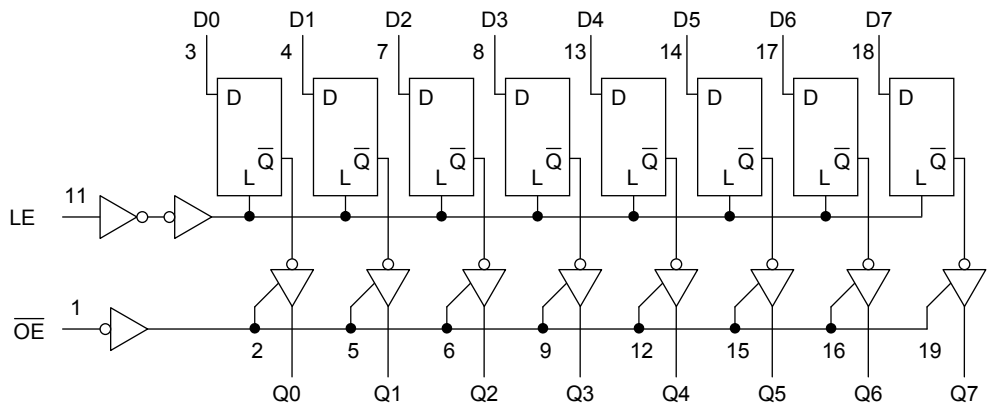
Inputs			Output
OE	LE	D	Q
H	X	X	Z
L	L	X	Q <sub>n</sub>
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Q<sub>n</sub>: Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 50$	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 200$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^\circ\text{C}$ . From  $T_a = 65$  to  $85^\circ\text{C}$  a derating factor of  $-10$  mW/°C should be applied up to 300 mW.

## Recommended Operating Conditions (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$dt/dV$	0 to 10	ns/V

Note: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to 85°C		Unit
					Min	Typ.	Max	Min	Max	
High-level input voltage	V <sub>IH</sub>	—		4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V <sub>IL</sub>	—		4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 µA	4.5	4.4	4.5	—	4.4	—	V
			I <sub>OH</sub> = -24 mA	4.5	3.94	—	—	3.80	—	
			I <sub>OH</sub> = -75 mA (Note)	5.5	—	—	—	3.85	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 µA	4.5	—	0.0	0.1	—	0.1	V
			I <sub>OL</sub> = 24 mA	4.5	—	—	0.36	—	0.44	
			I <sub>OL</sub> = 75 mA (Note)	5.5	—	—	—	—	1.65	
3-state output off-state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.5	—	±5.0	µA
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.1	—	±1.0	µA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	8.0	—	80.0	µA
	I <sub>C</sub>	Per input: V <sub>IN</sub> = 3.4 V Other input: V <sub>CC</sub> or GND		5.5	—	—	1.35	—	1.5	mA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

### Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit
				V <sub>CC</sub> (V)	Limit	Limit	
Minimum pulse width (LE)	t <sub>w</sub> (H)	—		5.0 ± 0.5	—	5.0	ns
Minimum set-up time	t <sub>s</sub>	—		5.0 ± 0.5	—	2.0	ns
Minimum hold time	t <sub>h</sub>	—		5.0 ± 0.5	—	3.0	ns

**AC Characteristics ( $C_L = 50 \text{ pF}$ ,  $R_L = 500 \Omega$ , input:  $t_r = t_f = 3 \text{ ns}$ )**

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (LE-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	—	5.0 ± 0.5	—	5.8	9.2	1.0	10.5	ns
Propagation delay time (D-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	—	5.0 ± 0.5	—	5.9	9.6	1.0	11.0	ns
Output enable time	t <sub>pZL</sub> t <sub>pZH</sub>	—	5.0 ± 0.5	—	6.5	10.5	1.0	12.0	ns
Output disable time	t <sub>pLZ</sub> t <sub>pHZ</sub>	—	5.0 ± 0.5	—	5.5	7.8	1.0	9.0	ns
Input capacitance	C <sub>IN</sub>	—		—	5	10	—	10	pF
Output capacitance	C <sub>OUT</sub>	—		—	10	—	—	—	pF
Power dissipation capacitance	C <sub>PD</sub>	(Note)		—	32	—	—	—	pF

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per latch)}$$

And the total C<sub>PD</sub> when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD (total)} = 20 + 12 \cdot n$$

## Package Dimensions

DIP20-P-300-2.54A

Unit : mm

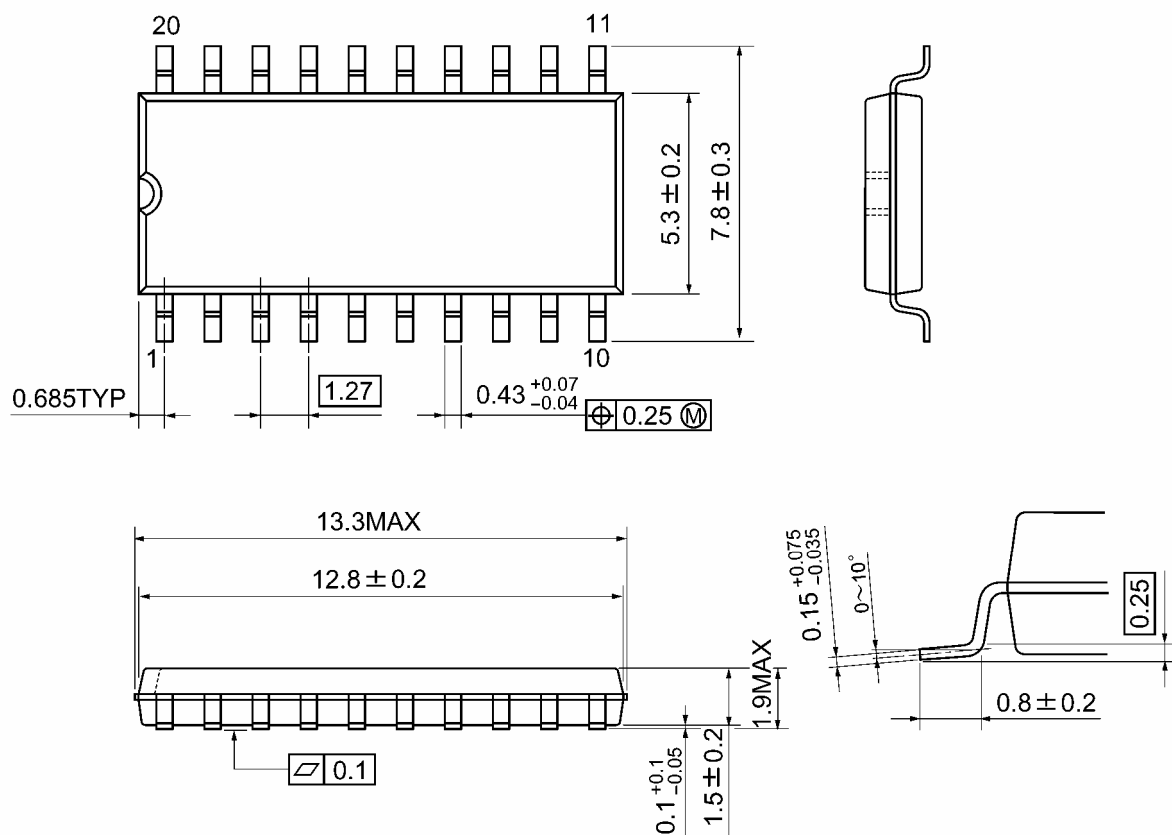


Weight: 1.30 g (typ.)

## Package Dimensions

SOP20-P-300-1.27A

Unit: mm

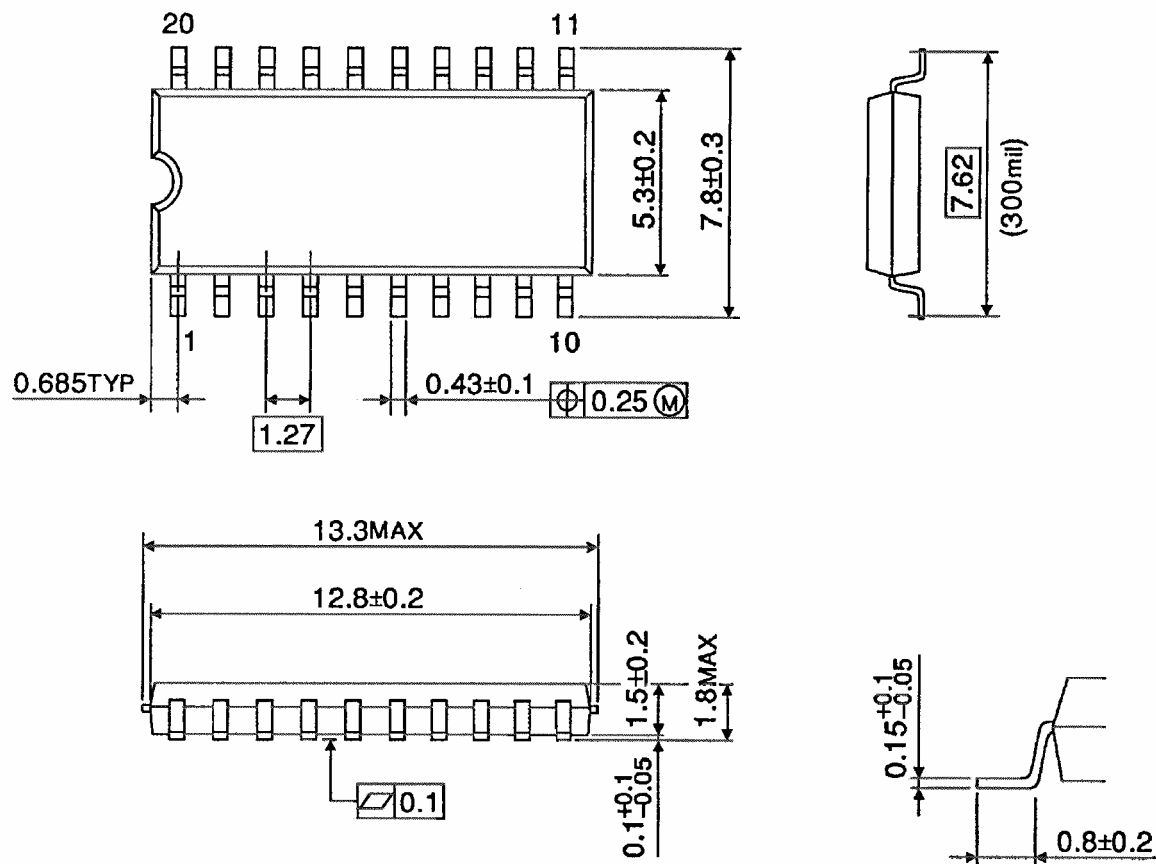


Weight: 0.22 g (typ.)

## Package Dimensions

SOP20-P-300-1.27

Unit : mm



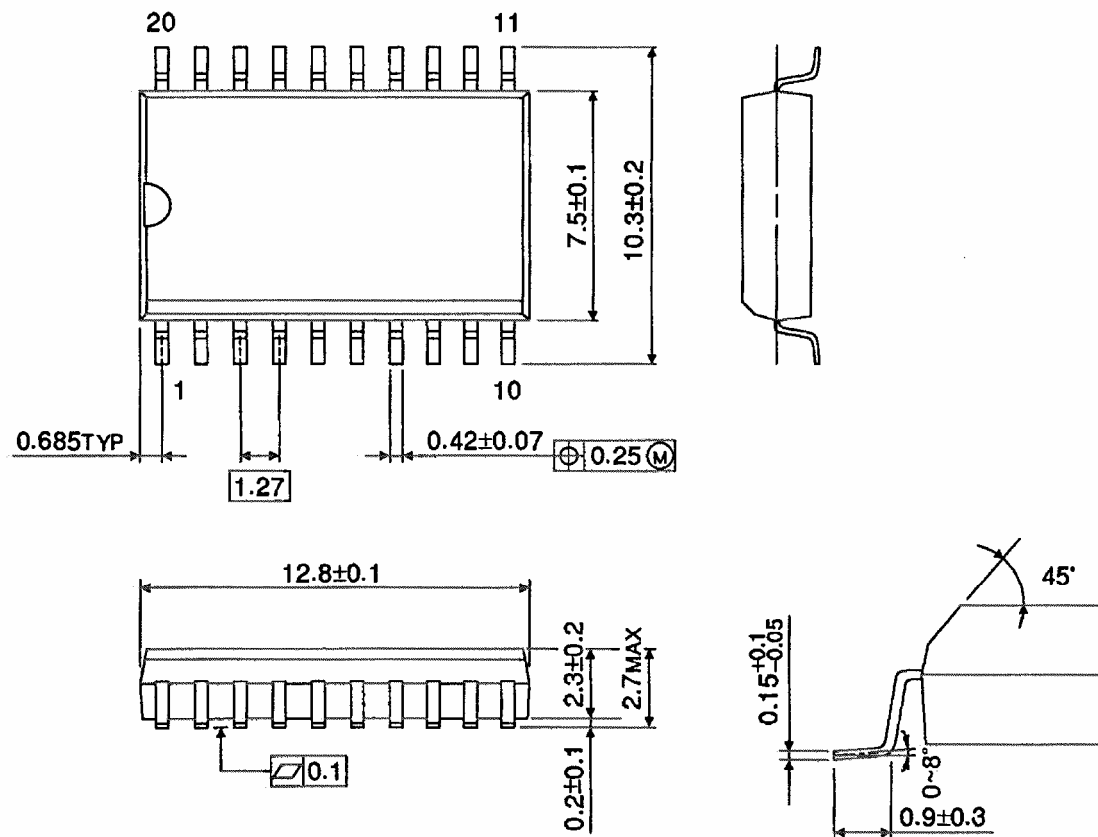
Weight: 0.22 g (typ.)



## Package Dimensions (Note)

SOL20-P-300-1.27

Unit : mm



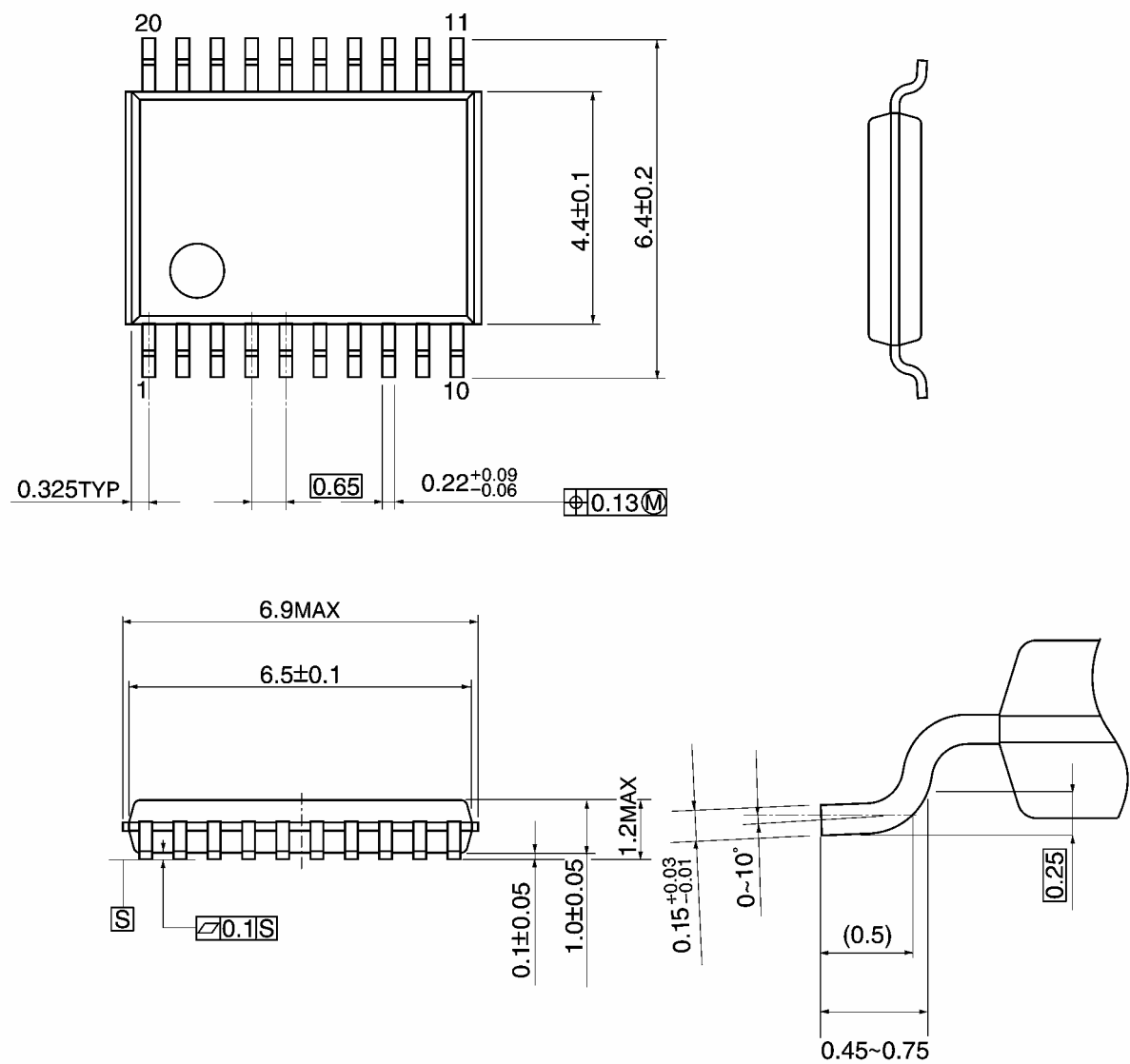
Note: This package is not available in Japan.

Weight: 0.46 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm



Weight: 0.08 g (typ.)

**Note: Lead (Pb)-Free Packages**

**DIP20-P-300-2.54A   SOP20-P-300-1.27A   TSSOP20-P-0044-0.65A**

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20070701-EN

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