

TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSVI)

SSM3J328R

○ Power Management Switch Applications

- 1.5-V drive
- Low ON-resistance: $R_{DS(ON)} = 88.4\text{m}\Omega$ (max) (@ $V_{GS} = -1.5\text{ V}$)
 $R_{DS(ON)} = 56.0\text{m}\Omega$ (max) (@ $V_{GS} = -1.8\text{ V}$)
 $R_{DS(ON)} = 39.7\text{m}\Omega$ (max) (@ $V_{GS} = -2.5\text{ V}$)
 $R_{DS(ON)} = 29.8\text{m}\Omega$ (max) (@ $V_{GS} = -4.5\text{ V}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	-20	V
Gate-source voltage		V_{GSS}	± 8	V
Drain current	DC	I_D (Note 1)	-6.0	A
	Pulse	I_{DP} (Note 1,2)	-24.0	
Power dissipation		P_D (Note 3)	1	W
		$t = 10\text{s}$	2	
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature range		T_{stg}	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

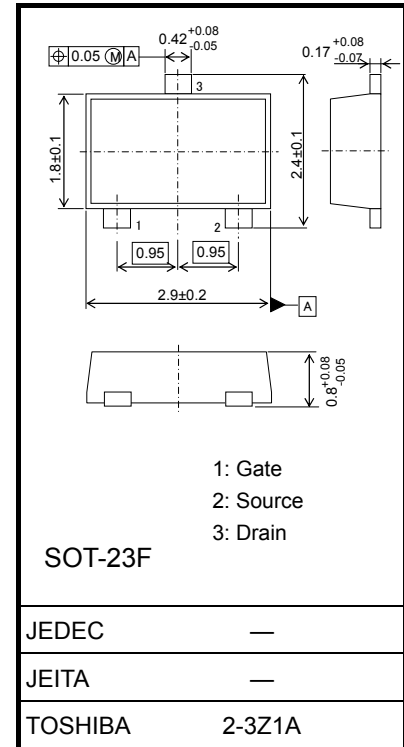
Note 1: The channel temperature should not exceed 150°C during use.

Note 2: $PW \leq 10\mu\text{s}$, Duty $\leq 1\%$

Note 3: Mounted on a FR4 board.

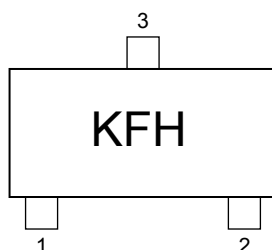
($25.4\text{ mm} \times 25.4\text{ mm} \times 1.6\text{ mm}$, Cu Pad: 645 mm^2)

Unit: mm

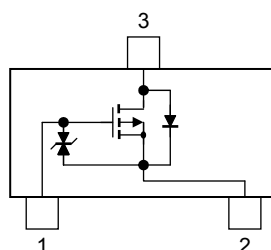


Weight: 11 mg (typ.)

Marking



Equivalent Circuit (Top view)



Start of commercial production
2010-08

Electrical Characteristics (Ta = 25°C)

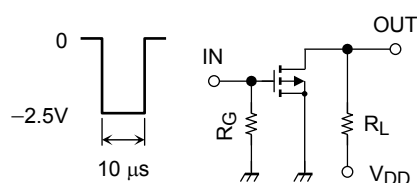
Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1 \text{ mA}$, $V_{GS} = 0 \text{ V}$	-20	—	—	V
	$V_{(BR)DSX}$	$I_D = -1 \text{ mA}$, $V_{GS} = 5 \text{ V}$ (Note 5)	-15	—	—	V
Drain cut-off current	I_{DSS}	$V_{DS} = -20 \text{ V}$, $V_{GS} = 0 \text{ V}$	—	—	-1	μA
Gate leakage current	I_{GSS}	$V_{GS} = \pm 8 \text{ V}$, $V_{DS} = 0 \text{ V}$	—	—	± 1	μA
Gate threshold voltage	V_{th}	$V_{DS} = -3 \text{ V}$, $I_D = -1 \text{ mA}$	-0.3	—	-1.0	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3 \text{ V}$, $I_D = -1.0 \text{ A}$ (Note 4)	4.5	9.1	—	S
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = -3.0 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ (Note 4)	—	24.9	29.8	$\text{m}\Omega$
		$I_D = -2.5 \text{ A}$, $V_{GS} = -2.5 \text{ V}$ (Note 4)	—	31.1	39.7	
		$I_D = -1.5 \text{ A}$, $V_{GS} = -1.8 \text{ V}$ (Note 4)	—	38.8	56.0	
		$I_D = -0.5 \text{ A}$, $V_{GS} = -1.5 \text{ V}$ (Note 4)	—	47.4	88.4	
Input capacitance	C_{iss}	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0 \text{ V}$ $f = 1 \text{ MHz}$	—	840	—	pF
Output capacitance	C_{oss}		—	118	—	
Reverse transfer capacitance	C_{rss}		—	99	—	
Total gate charge	Q_g	$V_{DD} = -10 \text{ V}$, $I_{DS} = -4.0 \text{ A}$, $V_{GS} = -4.5 \text{ V}$	—	12.8	—	nC
Gate-source charge	Q_{gs1}		—	1.4	—	
Gate-drain charge	Q_{gd}		—	3.0	—	
Switching time	Turn-on time	$V_{DD} = -10 \text{ V}$, $I_D = -2.0 \text{ A}$ $V_{GS} = 0 \text{ to } -2.5 \text{ V}$, $R_G = 4.7 \Omega$	—	32	—	ns
	Turn-off time		—	107	—	
Drain-Source forward voltage	V_{DSF}	$I_D = 6.0 \text{ A}$, $V_{GS} = 0 \text{ V}$ (Note 4)	—	0.87	1.2	V

Note4: Pulse test

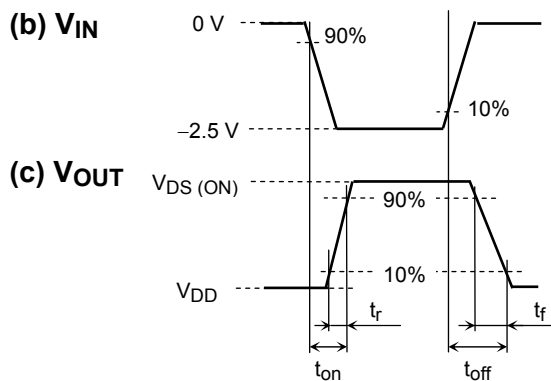
Note5: If a forward bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

(a) Test Circuit



$V_{DD} = -10 \text{ V}$
 $R_G = 4.7 \Omega$
 Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5 \text{ ns}$
 Common Source
 $T_a = 25^\circ\text{C}$



Notice on Usage

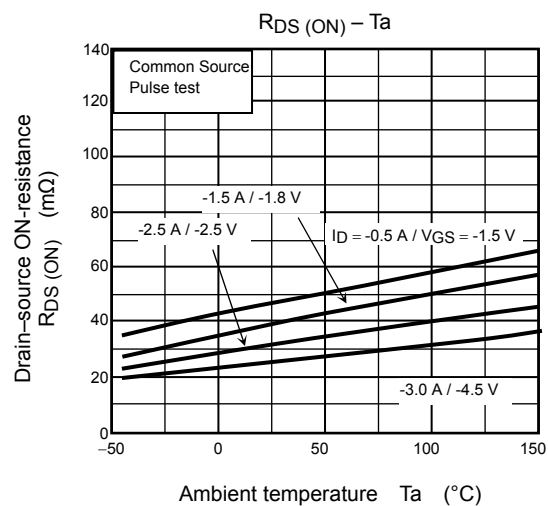
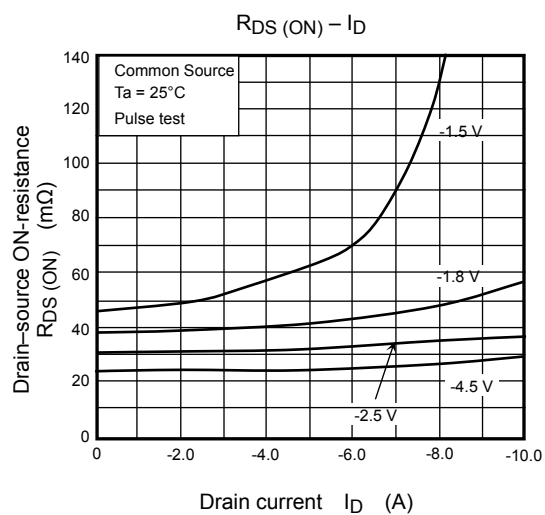
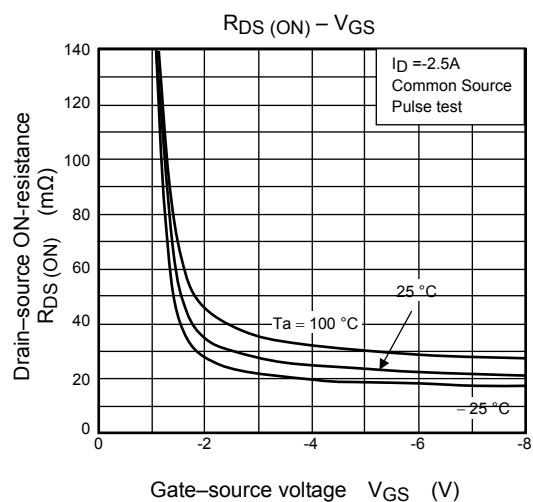
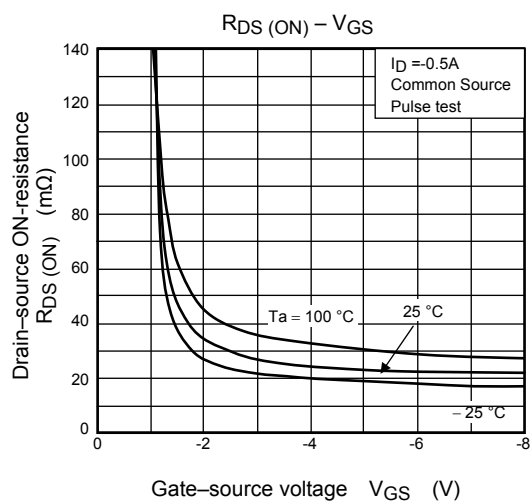
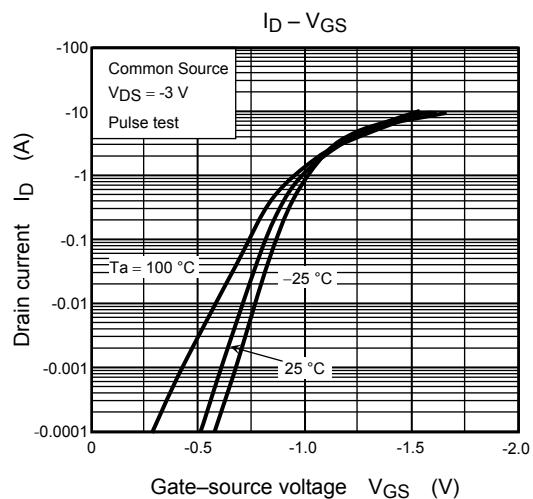
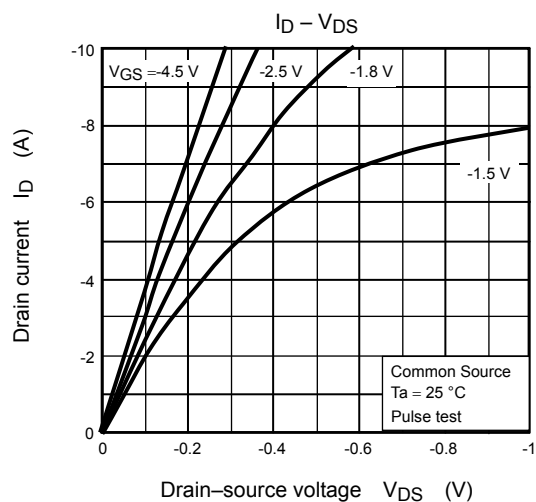
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (-1 mA for the SSM3J328R). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

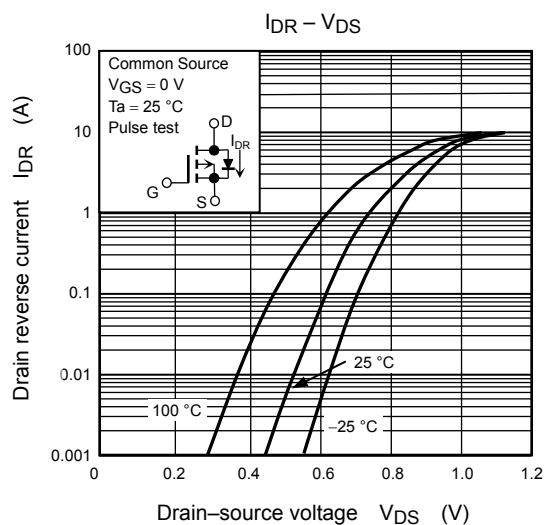
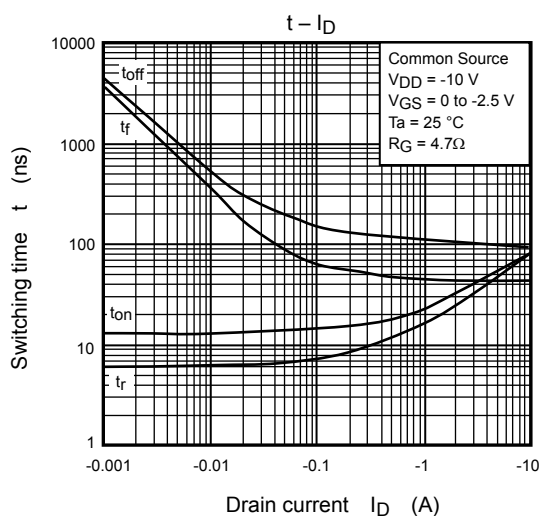
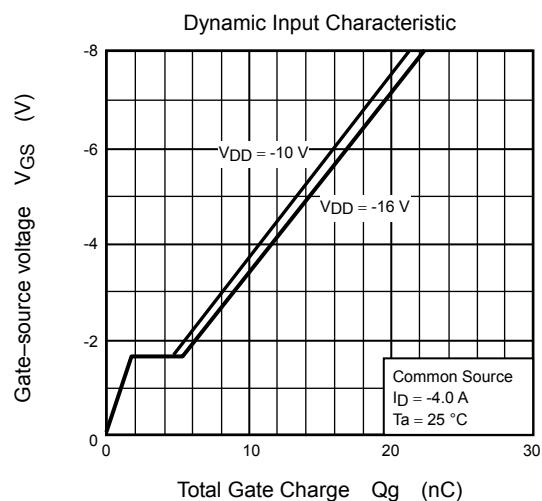
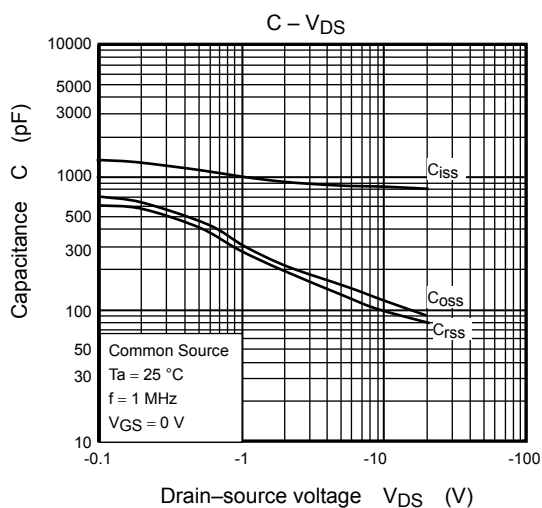
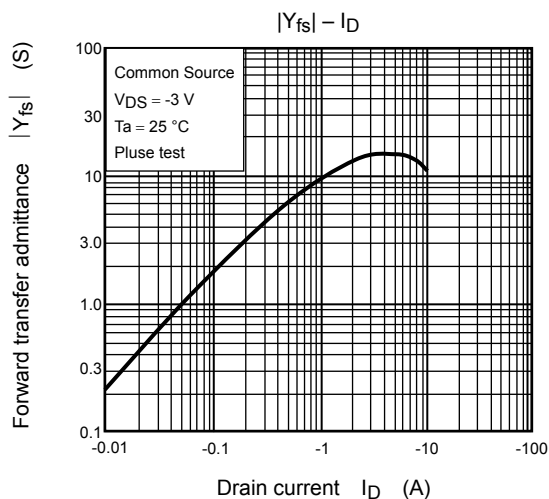
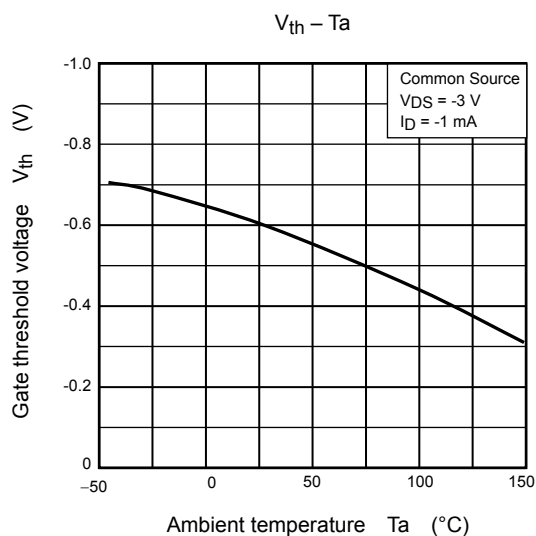
Take this into consideration when using the device.

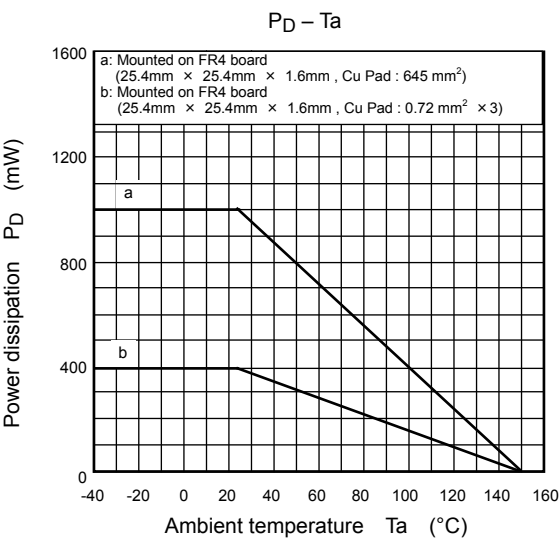
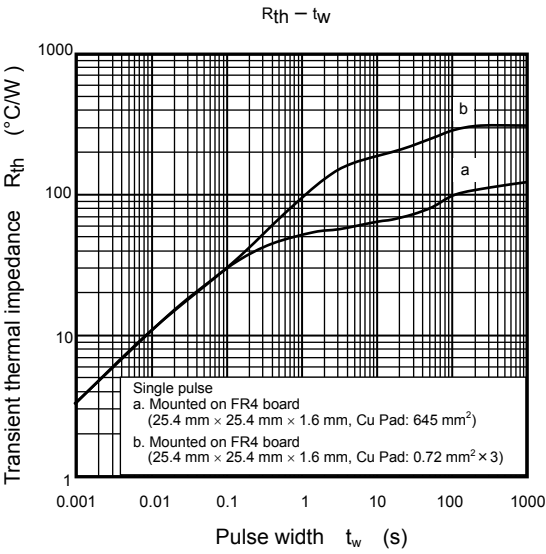
Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance $R_{th(ch-a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.







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