Single-Supply, Rail-to-Rail Low Power FET-Input Op Amp

AD822

FEATURES

True single-supply operation
    Output swings rail-to-rail
    Input voltage range extends below ground
    Single-supply capability from 3 V to 36 V
    Dual-supply capability from ±1.5 V to ±18 V
High load drive
    Capacitive load drive of 350 pF, G = +1
    Minimum output current of 15 mA
Excellent ac performance for low power
    800 μA maximum quiescent current per amplifier
    Unity gain bandwidth: 1.8 MHz
    Slew rate of 3.0 V/ms
Good dc performance
    800 μV maximum input offset voltage
    2 μV/°C typical offset voltage drift
    25 pA maximum input bias current
Low noise
13 nV/√Hz @ 10 kHz
No phase inversion

APPLICATIONS

Battery-powered precision instrumentation
Photodiode preamps
Active filters
12-bit to 14-bit data acquisition systems
Medical instrumentation
Low power references and regulators
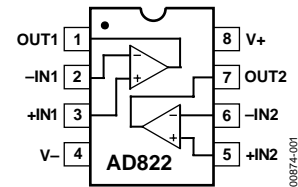
FUNCTIONAL BLOCK DIAGRAM

Figure 1. 8-Lead PDIP (N Suffix); 8-Lead MSOP (RM Suffix); and 8-Lead SOIC (R Suffix)

GENERAL DESCRIPTION

The AD822 is a dual precision, low power FET input op amp that can operate from a single supply of 3.0 V to 36 V or dual supplies of ±1.5 V to ±18 V. It has true single-supply capability with an input voltage range extending below the negative rail, allowing the AD822 to accommodate input signals below ground in the single-supply mode. Output voltage swing extends to within 10 mV of each rail, providing the maximum output dynamic range.
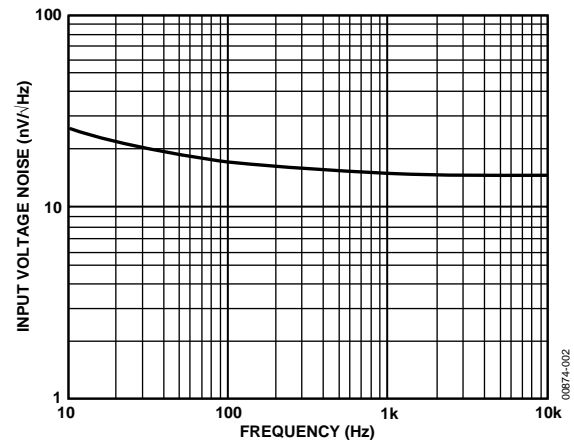

Figure 2. Input Voltage Noise vs. Frequency

Offset voltage of 800 μV maximum, offset voltage drift of 2 μV/°C, input bias currents below 25 pA, and low input voltage noise provide dc precision with source impedances up to a GΩ. 1.8 MHz unity gain bandwidth, −93 dB THD at 10 kHz, and 3 V/μs slew rate are provided with a low supply current of 800 μA per amplifier.

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REVISION HISTORY

GENERAL DESCRIPTION

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The AD822 drives up to 350 pF of direct capacitive load as a follower and provides a minimum output current of 15 mA. This allows the amplifier to handle a wide range of load conditions. Its combination of ac and dc performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for the single-supply user.

The AD822 is available in two performance grades. The A grade and B grade are rated over the industrial temperature range of −40°C to +85°C.

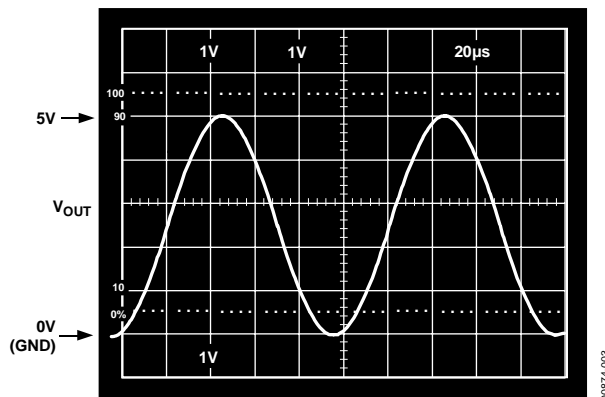The AD822 is offered in three varieties of 8-lead packages: PDIP, MSOP, and SOIC.

Figure 3. Gain-of-2 Amplifier; V_S = 5, 0, V_{IN} = 2.5 V Sine Centered at 1.25 V, R_L = 100 Ω

AD822

SPECIFICATIONS

$V_S = 0$, 5 V @ $T_A = 25°C$, $V_{CM} = 0$ V, $V_{OUT} = 0.2$ V, unless otherwise noted.

Table 1.

Parameter	Condition	AD822 A Grade			AD822 B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.1	0.4	mV
Maximum Offset Overtemperature			0.5	1.2		0.5	0.9	mV
Offset Drift			2			2		μV/°C
Input Bias Current	$V_{CM} = 0$ V to 4 V		2	25		2	10	pA
at T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	$V_O = 0.2$ V to 4 V							
	$R_L = 100$ kΩ	500	1000		500	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	$R_L = 10$ kΩ	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	$R_L = 1$ kΩ	15	30		15	30		V/mV
T_{MIN} to T_{MAX}		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		μV p-p
$f = 10$ Hz			25			25		nV/√Hz
$f = 100$ Hz			21			21		nV/√Hz
$f = 1$ kHz			16			16		nV/√Hz
$f = 10$ kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
$f = 1$ kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	$R_L = 10$ kΩ to 2.5 V							
$f = 10$ kHz	$V_O = 0.25$ V to 4.75 V		−93			−93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.8			1.8		MHz
Full Power Response	V_O p-p = 4.5 V		210			210		kHz
Slew Rate			3			3		V/μs
Settling Time								
to 0.1%	$V_O = 0.2$ V to 4.5 V		1.4			1.4		μs
to 0.01%			1.8			1.8		μs
MATCHING CHARACTERISTICS								
Initial Offset				1.0			0.5	mV
Maximum Offset overtemperature				1.6			1.3	mV
Offset Drift			3			3		μV/°C
Input Bias Current				20			10	pA
Crosstalk @ $f = 1$ kHz	$R_L = 5$ kΩ		−130			−130		dB
$f = 100$ kHz			−93			−93		dB
INPUT CHARACTERISTICS								
Input Voltage Range[1]		−0.2		+4	−0.2		+4	V
T_{MIN} to T_{MAX}		−0.2		+4	−0.2		+4	V
Common-Mode Rejection Ratio (CMRR)	$V_{CM} = 0$ V to 2 V	66	80		69	80		dB
T_{MIN} to T_{MAX}	$V_{CM} = 0$ V to 2 V	66			66			dB

Parameter	Condition	AD822 A Grade			AD822 B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Impedance								
Differential			$10^{13}\|\|0.5$			$10^{13}\|\|0.5$		Ω||pF
Common Mode			$10^{13}\|\|2.8$			$10^{13}\|\|2.8$		Ω||pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
$V_{OL} - V_{EE}$	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
$V_{OL} - V_{EE}$	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
$V_{OL} - V_{EE}$	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current T_{MIN} to T_{MAX}			1.24	1.6		1.24	1.6	mA
Power Supply Rejection	V_S+ = 5 V to 15 V	66	80		70	80		dB
T_{MIN} to T_{MAX}		66			70			dB

[1] This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range $(+V_s - 1 \text{ V})$ to $+V_s$. Common-mode effort voltage is typically less than 5 mV with the common-mode voltage set at 1 V below the positive supply.

[2] $V_{OL} - V_{EE}$ is defined as the difference between the lowest possible output voltage (V_{OL}) and the negative voltage supply rail (V_{EE}). $V_{CC} - V_{OH}$ is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

$V_S = \pm 5$ V @ T_A = 25°C, V_{CM} = 0 V, V_{OUT} = 0 V, unless otherwise noted.

Table 2.

Parameter	Conditions	AD822 A Grade			AD822 B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.1	0.4	mV
Maximum Offset Overtemperature			0.5	1.5		0.5	1	mV
Offset Drift			2			2		µV/°C
Input Bias Current	V_{CM} = −5 V to +4 V		2	25		2	10	pA
at T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = −4 V to +4 V							
	R_L = 100 kΩ	400	1000		400	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	R_L = 10 kΩ	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	R_L = 1 kΩ	20	30		20	30		V/mV
T_{MIN} to T_{MAX}		10			10			V/mV

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Parameter	Conditions	AD822 A Grade			AD822 B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		µV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	$R_L = 10\ k\Omega$							
f = 10 kHz	$V_O = \pm4.5\ V$		−93			−93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.9		MHz
Full Power Response	V_O p-p = 9 V		105			105		kHz
Slew Rate			3			3		V/µs
Settling Time								
to 0.1%	$V_O = 0\ V$ to $\pm4.5\ V$		1.4			1.4		µs
to 0.01%			1.8			1.8		µs
MATCHING CHARACTERISTICS								
Initial Offset				1.0			0.5	mV
Maximum Offset Overtemperature				3			2	mV
Offset Drift			3			3		µV/°C
Input Bias Current				25			10	pA
Crosstalk @ f = 1 kHz	$R_L = 5\ k\Omega$		−130			−130		dB
f = 100 kHz			−93			−93		dB
INPUT CHARACTERISTICS								
Input Voltage Range[1]		−5.2		+4	−5.2		+4	V
T_{MIN} to T_{MAX}		−5.2		+4	−5.2		+4	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = −5 V to +2 V	66	80		69	80		dB
T_{MIN} to T_{MAX}	V_{CM} = −5 V to +2 V	66			66			dB
Input Impedance								
Differential			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
$V_{OL} - V_{EE}$	$I_{SINK} = 20\ µA$		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
$V_{CC} - V_{OH}$	$I_{SOURCE} = 20\ µA$		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
$V_{OL} - V_{EE}$	$I_{SINK} = 2\ mA$		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
$V_{CC} - V_{OH}$	$I_{SOURCE} = 2\ mA$		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
$V_{OL} - V_{EE}$	$I_{SINK} = 15\ mA$		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
$V_{CC} - V_{OH}$	$I_{SOURCE} = 15\ mA$		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Capacitive Load Drive			350			350		pF

Parameter	Conditions	AD822 A Grade Min	Typ	Max	AD822 B Grade Min	Typ	Max	Unit
POWER SUPPLY								
Quiescent Current T$_{MIN}$ to T$_{MAX}$			1.3	1.6		1.3	1.6	mA
Power Supply Rejection	V$_{S+}$ = 5 V to 15 V	66	80		70	80		dB
T$_{MIN}$ to T$_{MAX}$		66			70			dB

[1] This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range (+V$_s$ − 1 V) to +V$_s$. Common-mode effort voltage is typically less than 5 mV with the common-mode voltage set at 1 V below the positive supply.

[2] V$_{OL}$ − V$_{EE}$ is defined as the difference between the lowest possible output voltage (V$_{OL}$) and the negative voltage supply rail (V$_{EE}$). V$_{CC}$ − V$_{OH}$ is defined as the difference between the highest possible output voltage (V$_{OH}$) and the positive supply voltage (V$_{CC}$).

V$_S$ = ±15 V @ T$_A$ = 25°C, V$_{CM}$ = 0 V, V$_{OUT}$ = 0 V, unless otherwise noted.

Table 3.

Parameter	Conditions	AD822 A Grade Min	Typ	Max	AD822 B Grade Min	Typ	Max	Unit
DC PERFORMANCE								
Initial Offset			0.4	2		0.3	1.5	mV
Maximum Offset Overtemperature			0.5	3		0.5	2.5	mV
Offset Drift			2			2		µV/°C
Input Bias Current	V$_{CM}$ = 0 V		2	25		2	12	pA
	V$_{CM}$ = −10 V		40			40		pA
at T$_{MAX}$	V$_{CM}$ = 0 V		0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	12	pA
at T$_{MAX}$			0.5			0.5		nA
Open-Loop Gain	V$_O$ = +10 V to −10 V							
R$_L$ = 100 kΩ		500	2000		500	2000		V/mV
T$_{MIN}$ to T$_{MAX}$		500			500			V/mV
R$_L$ = 10 kΩ		100	500		100	500		V/mV
T$_{MIN}$ to T$_{MAX}$		100			100			V/mV
R$_L$ = 1 kΩ		30	45		30	45		V/mV
T$_{MIN}$ to T$_{MAX}$		20			20			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		µV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R$_L$ = 10 kΩ							
f = 10 kHz	V$_O$ = ±10 V		−85			−85		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.9		MHz
Full Power Response	V$_O$ p-p = 20 V		45			45		kHz
Slew Rate			3			3		V/µs
Settling Time								
to 0.1%	V$_O$ = 0 V to ±10 V		4.1			4.1		µs
to 0.01%			4.5			4.5		µs

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Parameter	Conditions	AD822 A Grade			AD822 B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
MATCHING CHARACTERISTICS								
Initial Offset				3			2	mV
Maximum Offset Overtemperature				4			2.5	mV
Offset Drift			3			3		µV/°C
Input Bias Current				25			12	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ		−130			−130		dB
f = 100 kHz			−93			−93		dB
INPUT CHARACTERISTICS								
Input Voltage Range[1]		−15.2		+14	−15.2		+4	V
T_{MIN} to T_{MAX}		−15.2		+14	−15.2		+4	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = −15 V to +12 V	70	80		74	90		dB
T_{MIN} to T_{MAX}	V_{CM} = −15 V to +12 V		70			74		dB
Input Impedance								
Differential			10^{13}||0.5			10^{13}||0.5		Ω||pF
Common Mode			10^{13}||2.8			10^{13}||2.8		Ω||pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
$V_{OL} − V_{EE}$	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
$V_{CC} − V_{OH}$	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
$V_{OL} − V_{EE}$	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
$V_{CC} − V_{OH}$	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
$V_{OL} − V_{EE}$	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
$V_{CC} − V_{OH}$	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		20			20			mA
T_{MIN} to T_{MAX}		15			15			mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current T_{MIN} to T_{MAX}			1.4	18		1.4	1.8	mA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70			dB

[1] This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range (+V_s − 1 V) to +V_s. Common-mode effort voltage is typically less than 5 mV with the common-mode voltage set at 1 V below the positive supply.

[2] $V_{OL} − V_{EE}$ is defined as the difference between the lowest possible output voltage (V_{OL}) and the negative voltage supply rail (V_{EE}). $V_{CC} − V_{OH}$ is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

V_S = 0, 3 V @ T_A = 25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V, unless otherwise noted.

Table 4.

Parameter	Conditions	Typ	Unit
DC PERFORMANCE			
Initial Offset		0.2	mV
Maximum Offset Overtemperature		0.5	mV
Offset Drift		1	µV/°C
Input Bias Current	V_{CM} = 0 V to 2 V	2	pA
at T_{MAX}		0.5	nA
Input Offset Current		2	pA
at T_{MAX}		0.5	nA

Parameter	Conditions	Typ	Unit
Open-Loop Gain	V_O = 0.2 V to 2 V		
R_L = 100 kΩ		1000	V/mV
R_L = 10 kΩ		150	V/mV
R_L = 1 kΩ		30	V/mV
NOISE/HARMONIC PERFORMANCE			
Input Voltage Noise		2	µV p-p
0.1 Hz to 10 Hz		25	nV/√Hz
f = 10 Hz		21	nV/√Hz
f = 100 Hz		16	nV/√Hz
f = 1 kHz		13	nV/√Hz
f = 10 kHz			
Input Current Noise			
0.1 Hz to 10 Hz		18	fA p-p
f = 1 kHz		0.8	fA/√Hz
Harmonic Distortion	R_L = 10 kΩ to 1.5 V		
f = 10 kHz	V_O = ±1.25 V	−92	dB
DYNAMIC PERFORMANCE			
Unity Gain Frequency		1.5	MHz
Full Power Response	V_O p-p = 2.5 V	240	kHz
Slew Rate		3	V/µs
Settling Time			
to 0.1%	V_O = 0.2 V to 2.5 V	1	µs
to 0.01%		1.4	µs
MATCHING CHARACTERISTICS			
Offset Drift		2	µV/°C
Crosstalk @ f = 1 kHz	R_L = 5 kΩ	−130	dB
f = 100 kHz		−93	dB
INPUT CHARACTERISTICS			
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0 V to 1 V	74	dB
Input Impedance			
Differential		10^{13}‖0.5	Ω‖pF
Common Mode		10^{13}‖2.8	Ω‖pF
OUTPUT CHARACTERISTICS			
Output Saturation Voltage[1]			
$V_{OL} - V_{EE}$	I_{SINK} = 20 µA	5	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 20 µA	10	mV
$V_{OL} - V_{EE}$	I_{SINK} = 2 mA	40	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 2 mA	80	mV
$V_{OL} - V_{EE}$	I_{SINK} = 10 mA	200	mV
$V_{CC} - V_{OH}$	I_{SOURCE} = 10 mA	500	mV
Capacitive Load Drive		350	pF
POWER SUPPLY			
Quiescent Current		1.24	mA
Power Supply Rejection	V_S+ = 3 V to 15 V	80	dB

[1] $V_{OL} - V_{EE}$ is defined as the difference between the lowest possible output voltage (V_{OL}) and the negative voltage supply rail (V_{EE}). $V_{CC} - V_{OH}$ is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation[1]	
PDIP (N)	Observe Derating Curves
SOIC (R)	Observe Derating Curves
Input Voltage	$(+V_S + 0.2\text{ V})$ to $-(20\text{ V} + V_S)$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	±30 V
Storage Temperature Range (N)	−65°C to +125°C
Storage Temperature Range (R, RM)	−65°C to +150°C
Operating Temperature Range	
AD822 A Grade and B Grade	−40°C to +85°C
Lead Temperature Range (Soldering, 60 sec)	260°C

[1] 8-lead PDIP package: $\theta_{JA} = 90$°C/Ω.
8-lead SOIC package: $\theta_{JA} = 160$°C/Ω.
8-lead MSOP package: $\theta_{JA} = 190$°C/Ω.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD822 is limited by the associated rise in junction temperature. For plastic packages, the maximum safe junction temperature is 145°C. If these maximums are exceeded momentarily, proper circuit operation is restored as soon as the die temperature is reduced. Leaving the device in the overheated condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves shown in Figure 27.

While the AD822 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. With power supplies ±12 V (or less) at an ambient temperature of 25°C or less, if the output node is shorted to a supply rail, then the amplifier is not destroyed, even if this condition persists for an extended period.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS
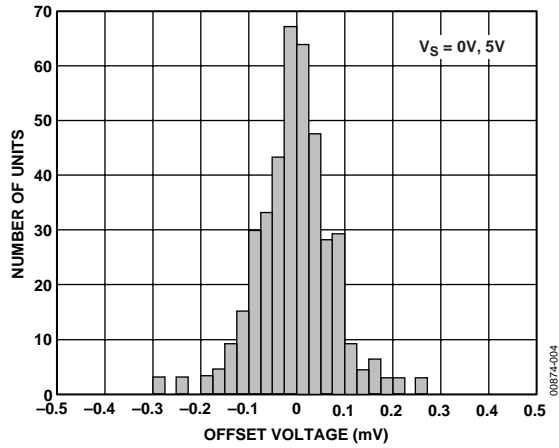
Figure 4. Typical Distribution of Offset Voltage (390 Units)
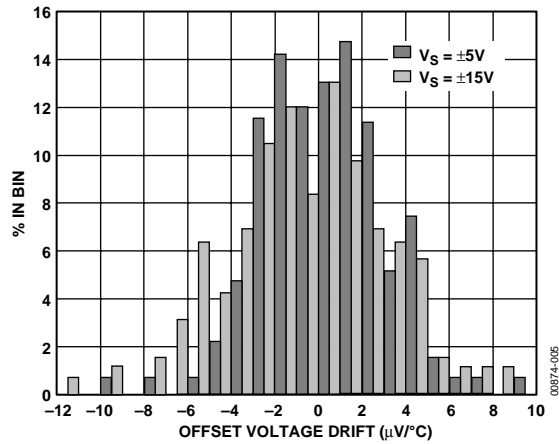
Figure 5. Typical Distribution of Offset Voltage Drift (100 Units)
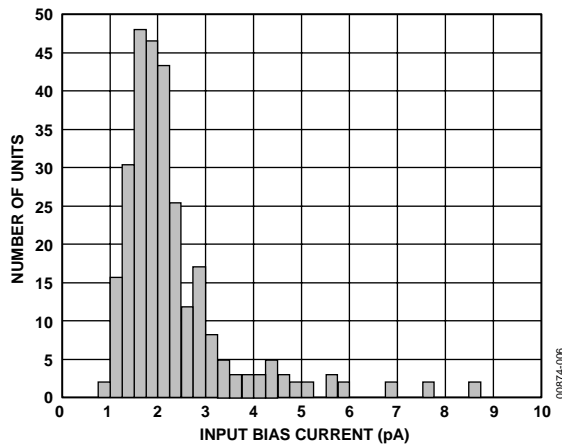
Figure 6. Typical Distribution of Input Bias Current (213 Units)
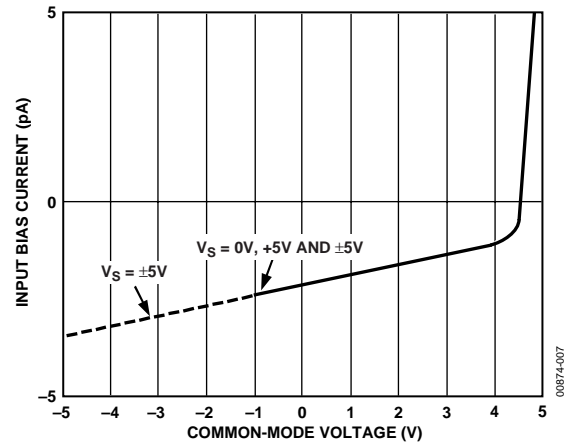
Figure 7. Input Bias Current vs. Common-Mode Voltage; $V_S = 5$ V, 0 V, and $V_S = \pm5$ V
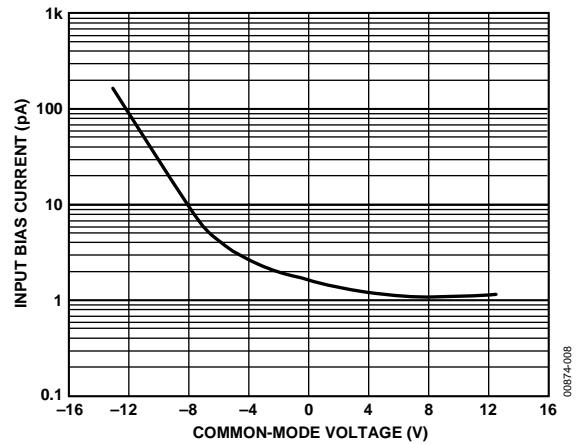
Figure 8. Input Bias Current vs. Common-Mode Voltage; $V_S = \pm15$ V
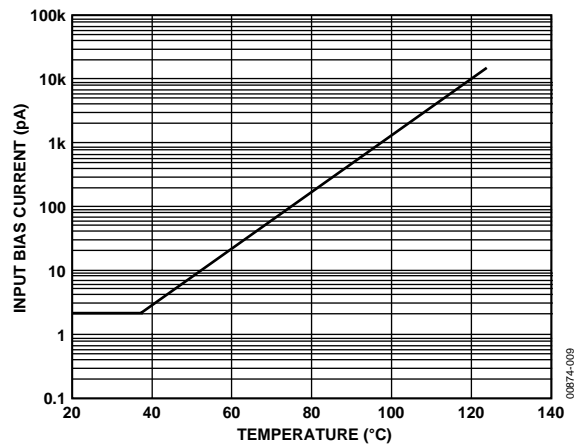
Figure 9. Input Bias Current vs. Temperature; $V_S = 5$ V, $V_{CM} = 0$
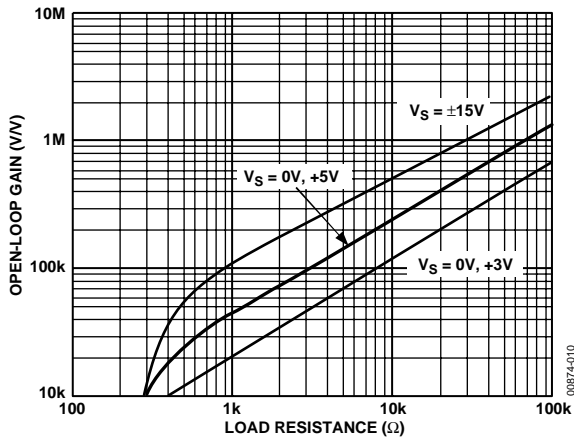
Figure 10. Open-Loop Gain vs. Load Resistance
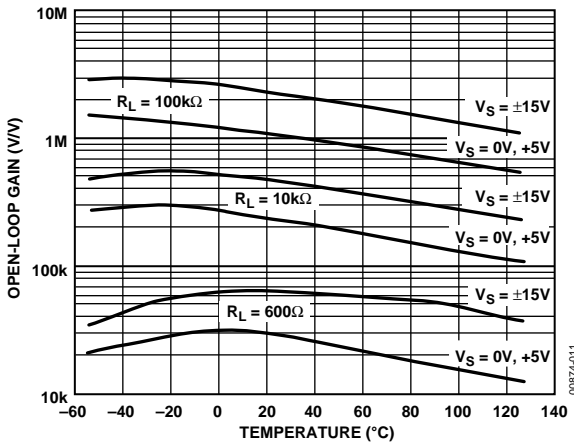
Figure 11. Open-Loop Gain vs. Temperature
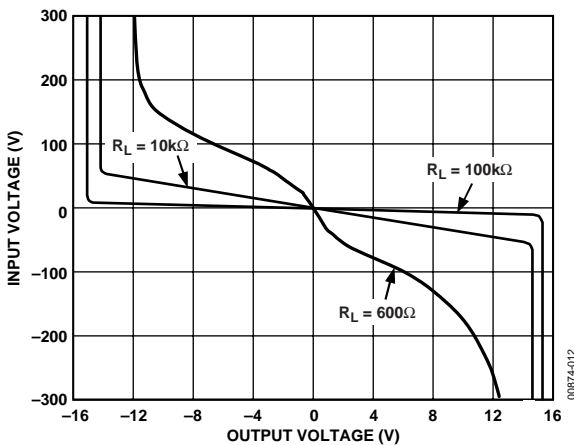
Figure 12. Input Error Voltage vs. Output Voltage for Resistive Loads
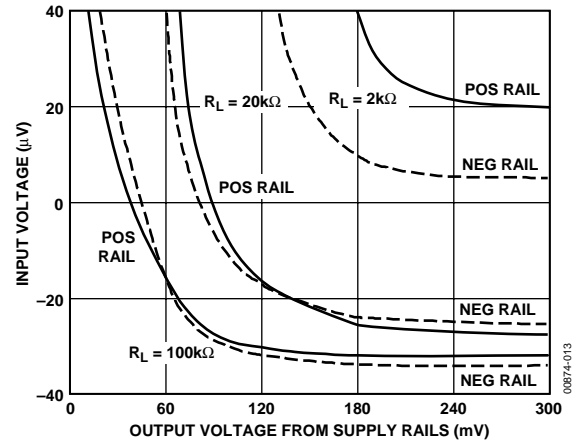
Figure 13. Input Effort Voltage with Output Voltage Within 300 mV of Either Supply Rail for Various Resistive Loads; $V_S = \pm 5$ V
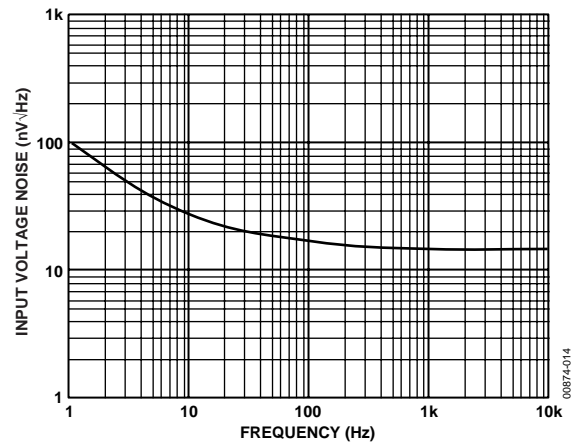
Figure 14. Input Voltage Noise vs. Frequency
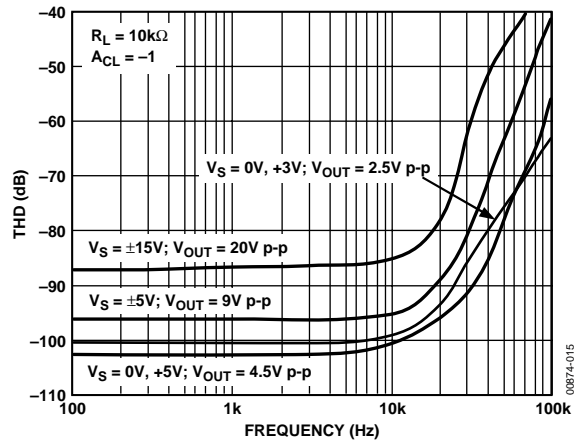
Figure 15. Total Harmonic Distortion (THD) vs. Frequency
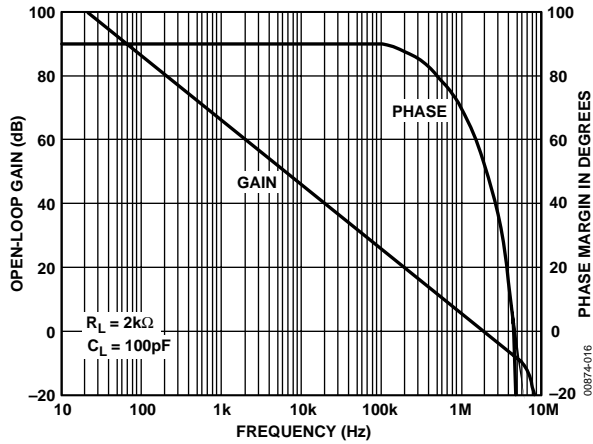
Figure 16. Open-Loop Gain and Phase Margin vs. Frequency

Figure 17. Output Impedance vs. Frequency

Figure 18. Output Swing and Error vs. Settling Time

Figure 19. Common-Mode Rejection vs. Frequency

Figure 20. Absolute Common-Mode Error vs. Common-Mode Voltage from Supply Rails ($V_S − V_{CM}$)
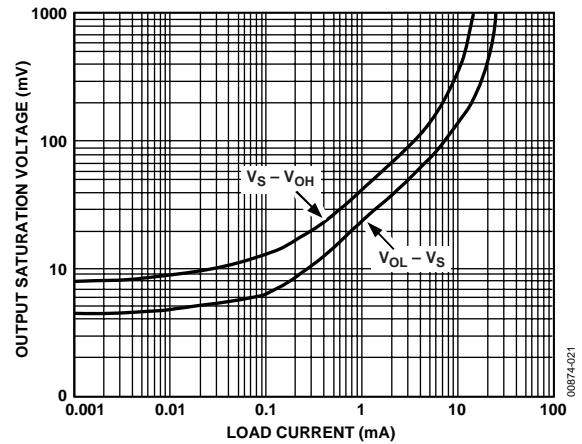
Figure 21. Output Saturation Voltage vs. Load Current
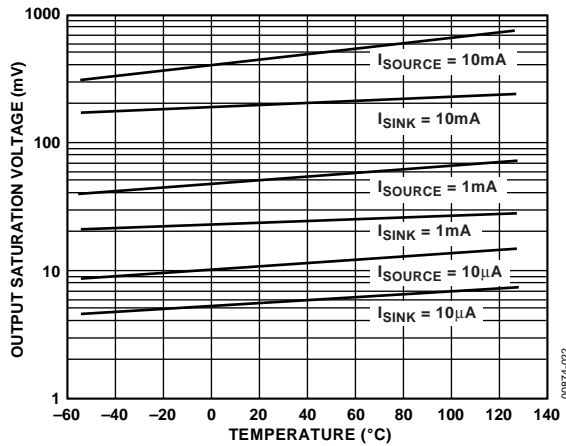
Figure 22. Output Saturation Voltage vs. Temperature

Figure 23. Short Circuit Current Limit vs. Temperature

Figure 24. Quiescent Current vs. Supply Voltage vs. Temperature

Figure 25. Power Supply Rejection vs. Frequency

Figure 26. Large Signal Frequency Response
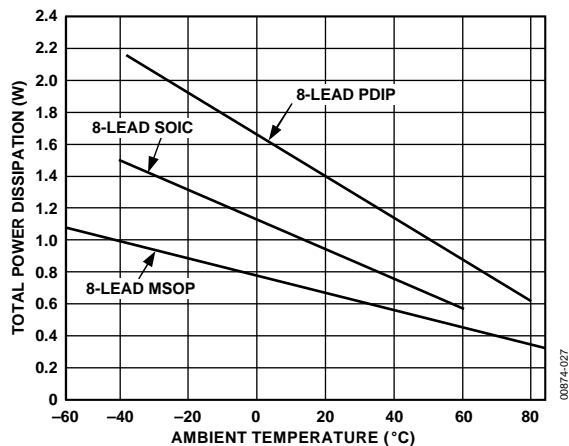
Figure 27. Maximum Power Dissipation vs. Temperature for Packages
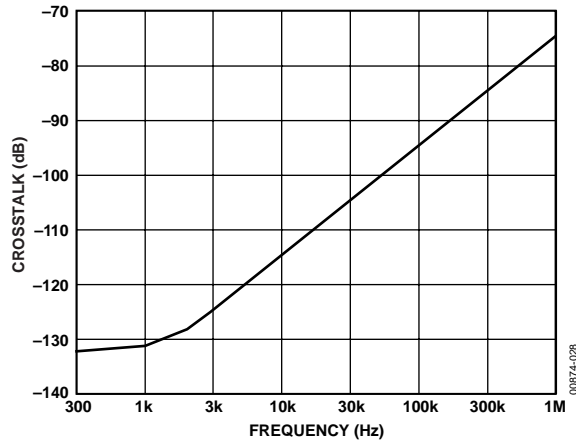
Figure 28. Crosstalk vs. Frequency
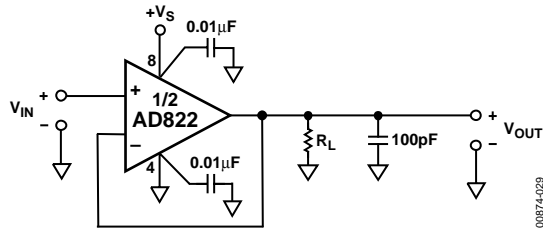
Figure 29. Unity Gain Follower
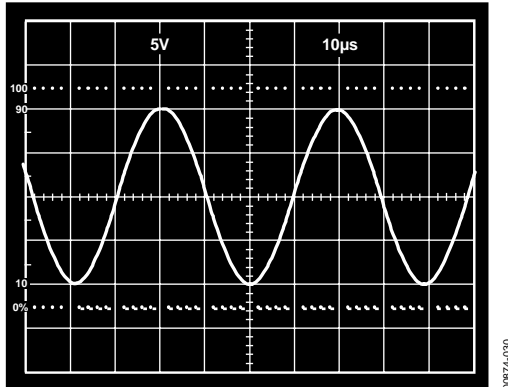
Figure 30. 20 V p-p, 25 kHz Sine Wave Input; Unity Gain Follower; $R_L = 600\,\Omega$, $V_S = \pm 15\,V$
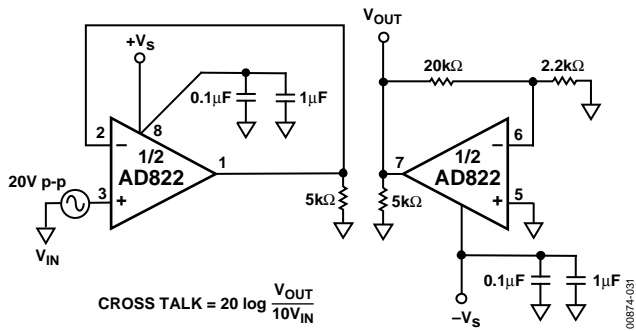
Figure 31. Crosstalk Test Circuit

$$CROSS\ TALK = 20\ log\frac{V_{OUT}}{10V_{IN}}$$
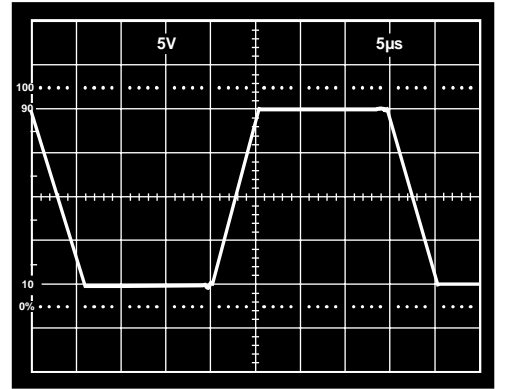
Figure 32. Large Signal Response Unity Gain Follower; $V_S = \pm15\,V$, $R_L = 10\,k\Omega$
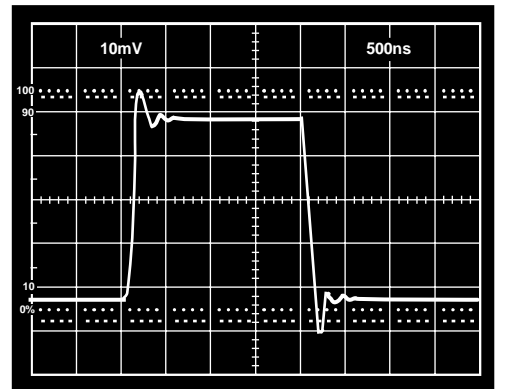
Figure 33. Small Signal Response Unity Gain Follower; $V_S = \pm15\,V$, $R_L = 10\,k\Omega$
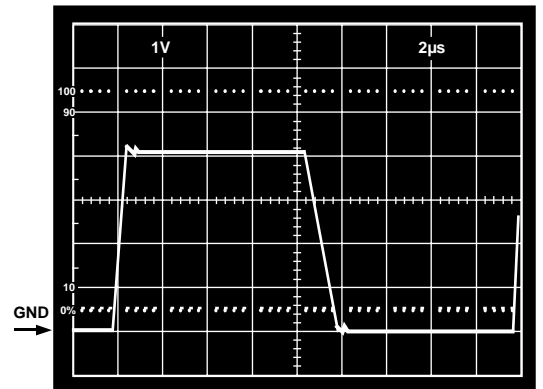
Figure 34. $V_S = 5\,V$, 0 V; Unity Gain Follower Response to 0 V to 4 V Step
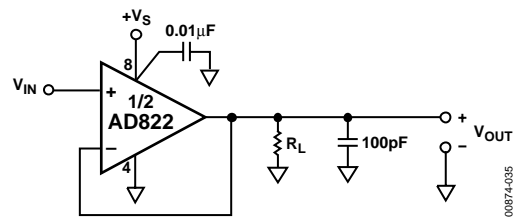
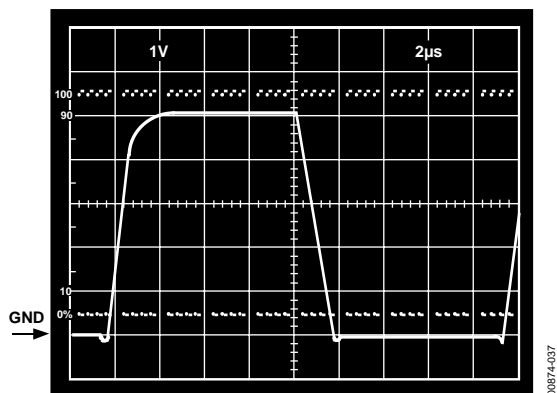Figure 35. Unity Gain Follower
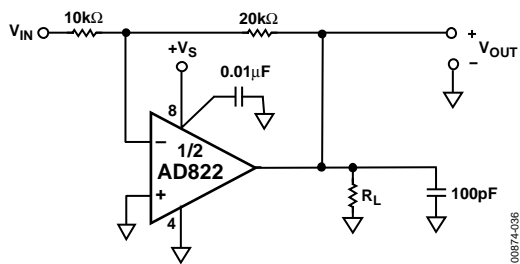
Figure 36. Gain-of-T2 Inverter

Figure 38. $V_S = 5$ V, 0 V; Unity Gain Follower Response to 40 mV Step, Centered 40 mV above Ground, $R_L = 10$ kΩ
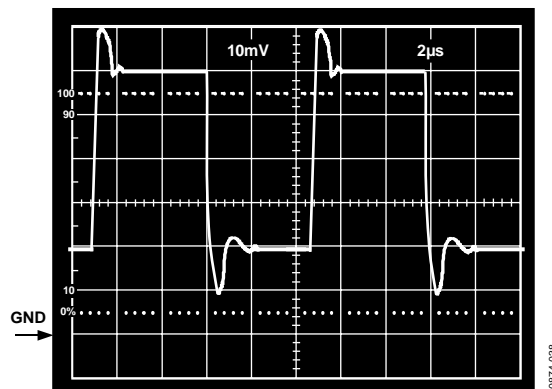

Figure 37. $V_S = 5$ V, 0 V; Unity Gain Follower Response to 0 V to 5 V Step

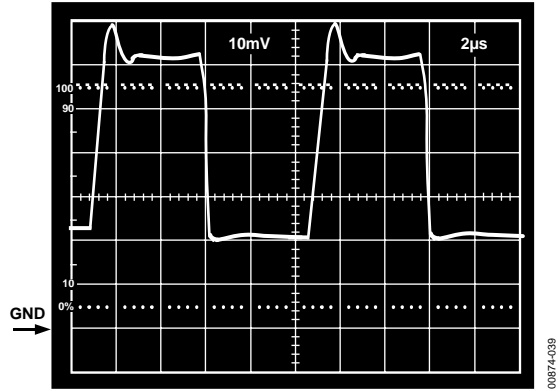Figure 39. $V_S = 5$ V, 0 V; Gain-of-2 Inverter Response to 20 mV Step, Centered 20 mV below Ground, $R_L = 10$ kΩ
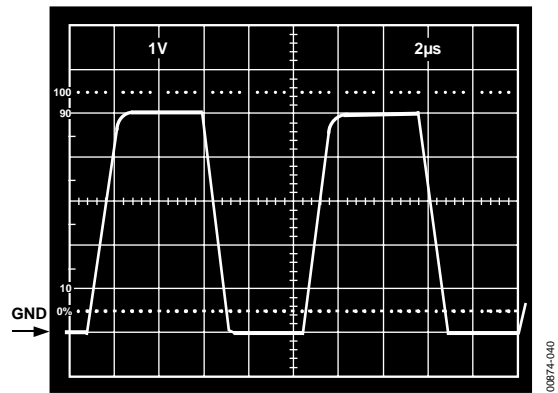

Figure 40. $V_S = 5$ V, 0 V; Gain-of-2 Inverter Response to 2.5 V Step, Centered −1.25 V below Ground, $R_L = 10$ kΩ
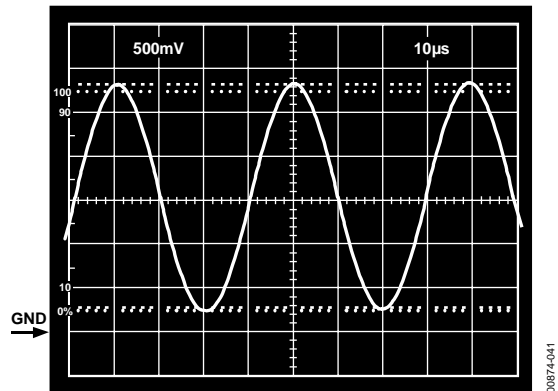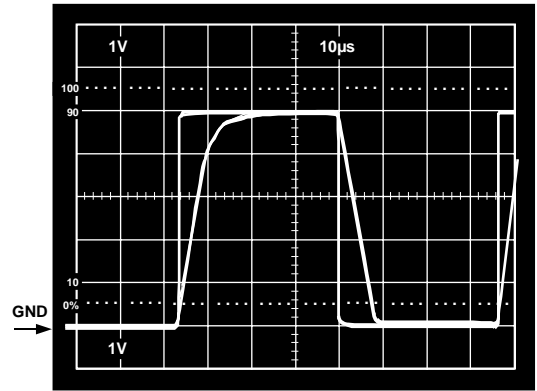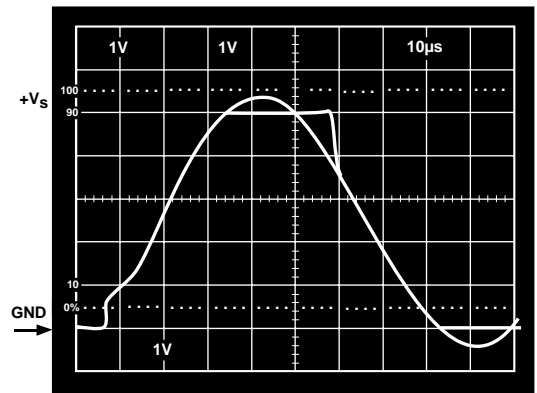

Figure 41. $V_S = 3$ V, 0 V; Gain-of-2 Inverter, $V_{IN} = 1.25$ V, 25 kHz, Sine Wave Centered at −0.75 V, $R_L = 600$ Ω
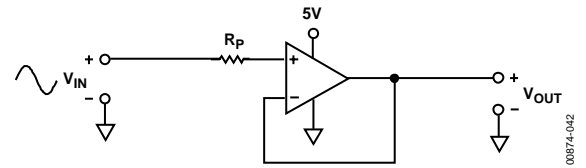

(a)

(b)

Figure 42. (a) Response with $R_P = 0$; V_{IN} from 0 to $+V_S$
(b) $V_{IN} = 0$ to $+V_S + 200$ mV
$V_{OUT} = 0$ to $+V_S$
$R_P = 49.9$ kΩ

APPLICATION NOTES

INPUT CHARACTERISTICS

In the AD822, n-channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $-V_S$ to 1 V less than $+V_S$. Driving the input voltage closer to the positive rail causes a loss of amplifier bandwidth (as can be seen by comparing the large signal responses shown in Figure 34 and Figure 37) and increased common-mode voltage error as illustrated in Figure 20.

The AD822 does not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 42 shows the response of an AD822 voltage follower to a 0 V to 5 V ($+V_S$) square wave input. The input and output are superimposed. The output tracks the input up to $+V_S$ without phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output waveform. For input voltages greater than $+V_S$, a resistor in series with the AD822's noninverting input prevents phase reversal, at the expense of greater input voltage noise. This is illustrated in Figure 42.

Since the input stage uses n-channel JFETs, input current during normal operation is negative; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S - 0.4$ V, then the input current reverses direction as internal device junctions become forward biased. This is illustrated in Figure 7.

A current limiting resistor should be used in series with the input of the AD822 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV, or if an input voltage is applied to the AD822 when $\pm V_S = 0$. The amplifier is damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 V of continuous overvoltage and increases the input voltage noise by a negligible amount.

Input voltages less than $-V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 V below the negative supply voltage as long as the total voltage from the positive supply to the input terminal is less than 36 V. In addition, the input stage typically maintains picoampere (pA) level input currents across that input voltage range.

The AD822 is designed for 13 nV/√Hz wideband input voltage noise and maintains low noise performance to low frequencies (refer to Figure 14). This noise performance, along with the AD822's low input current and current noise, means that the AD822 contributes negligible noise for applications with source resistances greater than 10 kΩ and signal bandwidths greater than 1 kHz. This is illustrated in Figure 43.
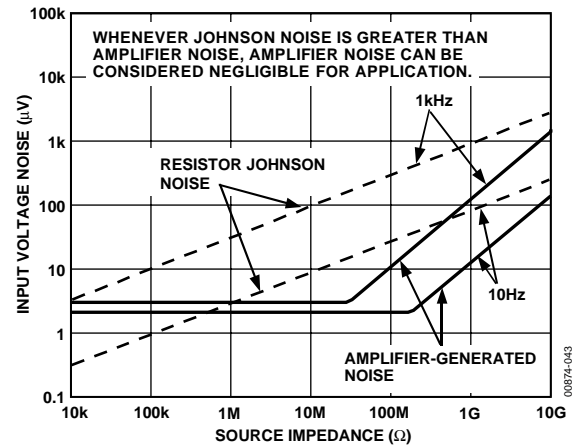

Figure 43. Total Noise vs. Source Impedance

OUTPUT CHARACTERISTICS

The AD822's unique bipolar rail-to-rail output stage swings within 5 mV of the negative supply and 10 mV of the positive supply with no external resistive load. The AD822's approximate output saturation resistance is 40 Ω sourcing and 20 Ω sinking. This can be used to estimate output saturation voltage when driving heavier current loads. For instance, when sourcing 5 mA, the saturation voltage to the positive supply rail is 200 mV; when sinking 5 mA, the saturation voltage to the negative rail is 100 mV.

The amplifier's open-loop gain characteristic changes as a function of resistive load, as shown in Figure 10 to Figure 13. For load resistances over 20 kΩ, the AD822's input error voltage is virtually unchanged until the output voltage is driven to 180 mV of either supply.

If the AD822's output is overdriven so as to saturate either of the output devices, the amplifier recovers within 2 μs of its input returning to the amplifier's linear operating region.

Direct capacitive loads interact with the amplifier's effective output impedance to form an additional pole in the amplifier's feedback loop, which can cause excessive peaking on the pulse response or loss of stability. Worst case is when the amplifier is used as a unity gain follower. Figure 44 shows the AD822's pulse response as a unity gain follower driving 350 pF. This amount of overshoot indicates approximately 20° of phase margin—the system is stable, but nearing the edge. Configurations with less loop gain, and as a result less loop bandwidth, are much less sensitive to capacitance load effects.
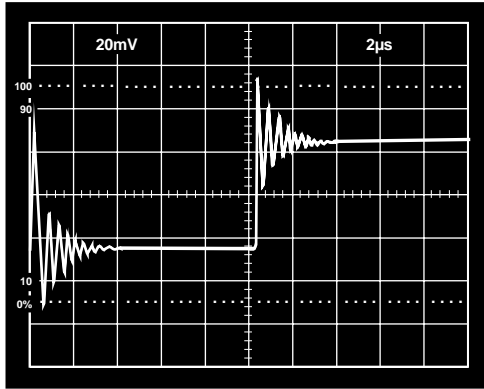
Figure 44. Small Signal Response of AD822 as
Unity Gain Follower Driving 350 pF

Figure 45 is a plot of capacitive load that results in a 20° phase margin vs. noise gain for the AD822. Noise gain is the inverse of the feedback attenuation factor provided by the feedback network in use.
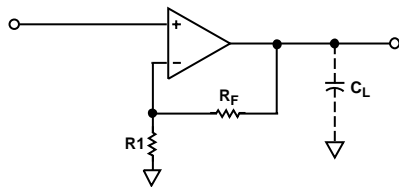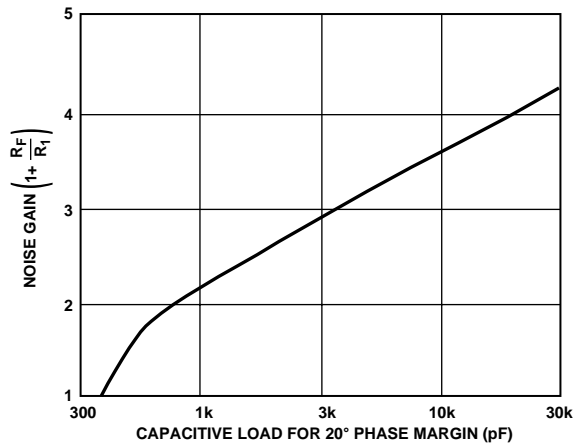

Figure 45. Capacitive Load Tolerance vs. Noise Gain

Figure 46 shows a method for extending capacitance load drive capability for a unity gain follower. With these component values, the circuit drives 5000 pF with a 10% overshoot.
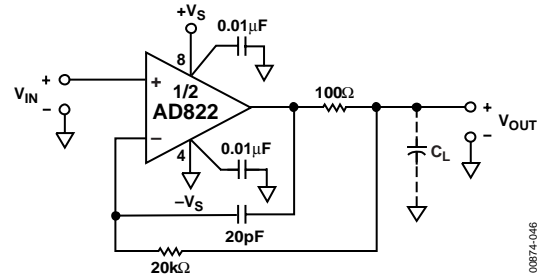

Figure 46. Extending Unity Gain Follower Capacitive Load Capability
Beyond 350 pF

APPLICATIONS

SINGLE-SUPPLY VOLTAGE-TO-FREQUENCY CONVERTER

The circuit shown in Figure 47 uses the AD822 to drive a low power timer that produces a stable pulse of width t_1. The positive going output pulse is integrated by R1 – C1 and used as one input to the AD822 that is connected as a differential integrator. The other input (nonloading) is the unknown voltage, V_{IN}. The AD822 output drives the timer trigger input, closing the overall feedback loop.

NOTES
1. $f_{OUT} = V_{IN}/(V_{REF} \times t_1)$, $t_1 = 1.1 \times R3 \times C6$. $= 25kHz$ F_S AS SHOWN.
2. * = 1% METAL FILM <50ppm/°C TC.
3. ** = 10% 20T FILM <100ppm/°C TC.
4. t_1 = 33μF FOR f_{OUT} = 20kHz @ V_{IN} = 2.0V.
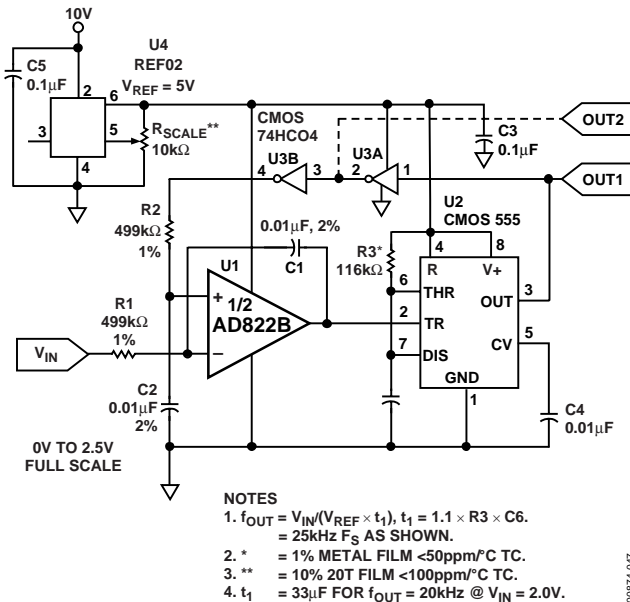
Figure 47. Single-Supply Voltage-to-Frequency Converter

Typical AD822 bias currents of 2 pA allow MΩ range source impedances with negligible dc errors. Linearity errors on the order of 0.01% full scale can be achieved with this circuit. This performance is obtained with a 5 V single supply that delivers less than 1 mA to the entire circuit.

SINGLE-SUPPLY PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

The AD822 can be configured as a single-supply instrumentation amplifier that is able to operate from single supplies down to 3 V or dual supplies up to ±15 V. Using only one AD822 rather than three separate op amps, this circuit is cost and power efficient. The AD822 FET inputs' 2 pA bias currents minimize offset errors caused by high unbalanced source impedances.

An array of precision thin-film resistors sets the in amp gain to be either 10 or 100. These resistors are laser trimmed to ratio match to 0.01% and have a maximum differential TC of 5 ppm/°C.

Table 6. In Amp Performance

Parameters	$V_S = 3\,V, 0\,V$	$V_S = 65\,V$
CMRR 74 dB	80 dB	
Common-Mode Voltage Range	−0.2 V to +2 V	−5.2 V to +4 V
3 dB BW, G = 10	180 kHz	180 kHz
G = 100	18 kHz	18 kHz
$t_{SETTLING}$		
2 V Step (V_S = 0 V, 3 V)	2 μs	
5 V (V_S = ± 5 V)		5 μs
Noise @ f = 1 kHz, G = 10	270 nV/√Hz	270 nV/√Hz
G = 100	2.2 μV/√Hz	2.2 μV/√Hz
I_{SUPPLY} (Total)	1.10 mA	1.15 mA
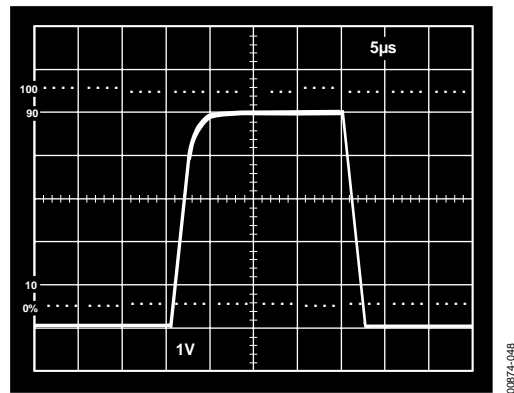
Figure 48. Pulse Response of In Amp to a 500 mV p-p Input Signal; V_S = 5 V, 0 V; Gain = 0

$$(G = 10) \quad V_{OUT} = (V_{IN1} - V_{IN2})\left(1 + \frac{R6}{R4 + R5}\right) + V_{REF}$$

$$(G = 100) \quad V_{OUT} = (V_{IN1} - V_{IN2})\left(1 + \frac{R5 + R6}{R4}\right) + V_{REF}$$
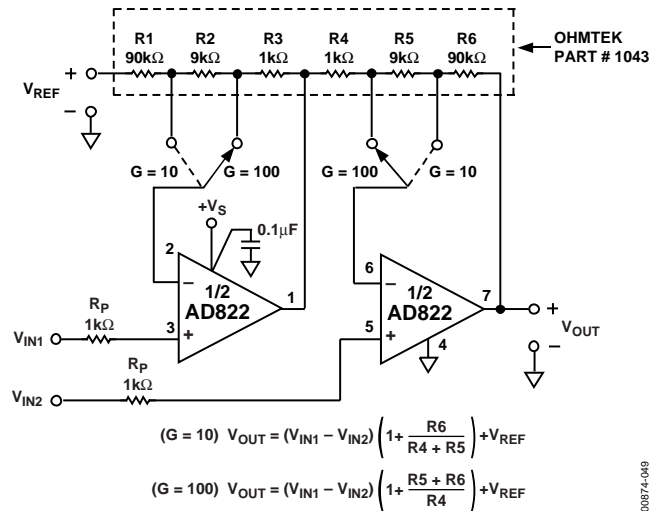
Figure 49. A Single-Supply Programmable Instrumentation Amplifier

3 V, SINGLE-SUPPLY STEREO HEADPHONE DRIVER

The AD822 exhibits good current drive and THD + N performance, even at 3 V single supplies. At 1 kHz, total harmonic distortion plus noise (THD + N) equals –62 dB (0.079%) for a 300 mV p-p output signal. This is comparable to other single-supply op amps that consume more power and cannot run on 3 V power supplies.
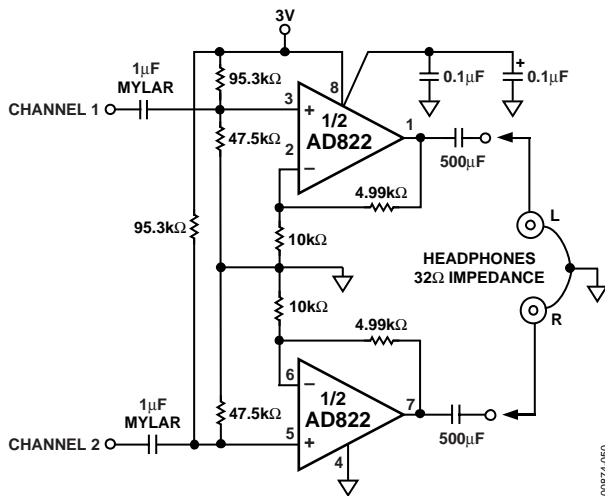

Figure 50. 3 V Single-Supply Stereo Headphone Driver

In Figure 50, each channel's input signal is coupled via a 1 µF Mylar capacitor. Resistor dividers set the dc voltage at the non-inverting inputs so that the output voltage is midway between the power supplies (1.5 V). The gain is 1.5. Each half of the AD822 can then be used to drive a headphone channel. A 5 Hz high-pass filter is realized by the 500 µF capacitors and the headphones that can be modeled as 32 Ω load resistors to ground. This ensures that all signals in the audio frequency range (20 Hz to 20 kHz) are delivered to the headphones.

LOW DROPOUT BIPOLAR BRIDGE DRIVER

The AD822 can be used for driving a 350 Ω Wheatstone bridge. Figure 51 shows one-half of the AD822 being used to buffer the AD589, a 1.235 V low power reference. The output of 4.5 V can be used to drive an ADC converter front end. The other half of the AD822 is configured as a unity gain inverter and generates the other bridge input of –4.5 V. Resistor R1 and Resistor R2 provide a constant current for bridge excitation. The AD620 low power instrumentation amplifier is used to condition the differential output voltage of the bridge. The gain of the AD620 is programmed using an external resistor RG and determined by
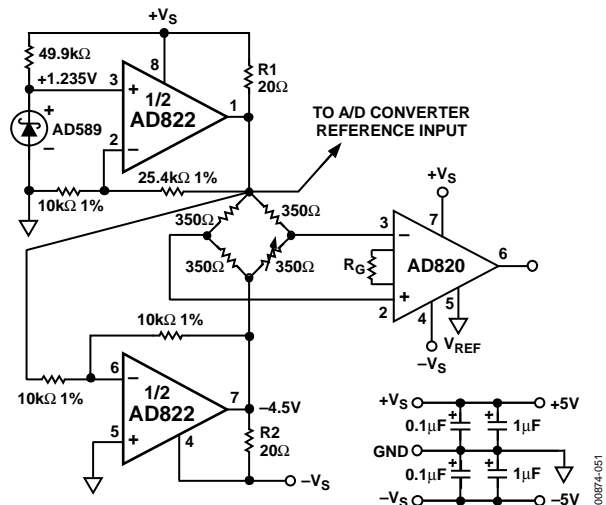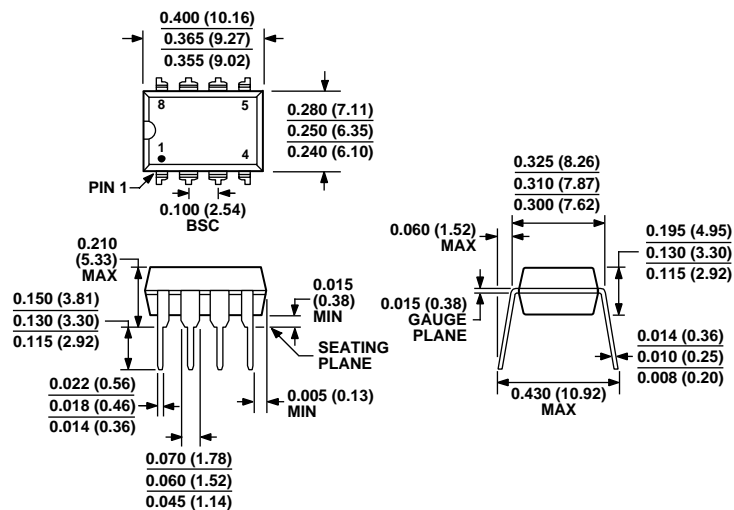
$$G = \frac{49.4\ \text{k}\Omega}{R_G} + 1$$

Figure 51. Low Dropout Bipolar Bridge Driver

OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MS-001-BA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 52. 8-Lead Plastic Dual In-Line Package [PDIP]
*Narrow Body*
(N-8)
Dimensions shown in inches and (millimeters)
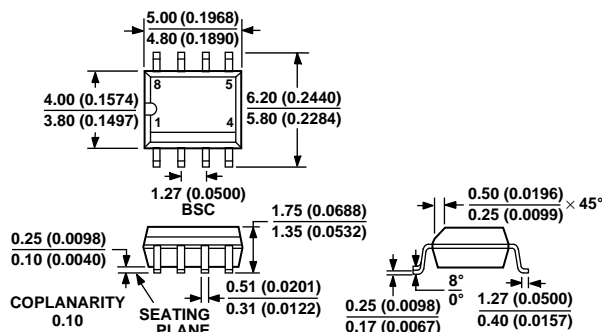
COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 53. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)
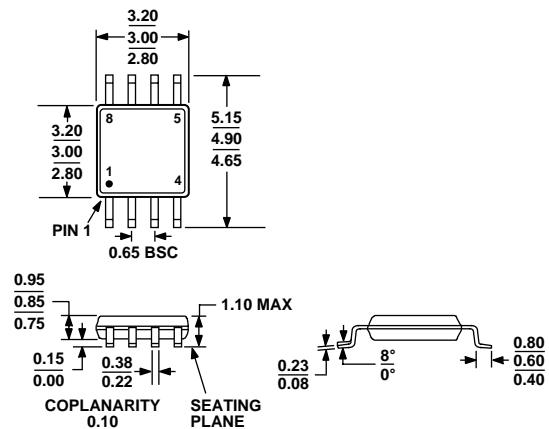
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 54. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD822AN	–40°C to +85°C	8-Lead PDIP	N-8	
AD822ANZ[1]	–40°C to +85°C	8-Lead PDIP	N-8	
AD822AR	–40°C to +85°C	8-Lead SOIC	R-8	
AD822AR-REEL	–40°C to +85°C	8-Lead SOIC	R-8	
AD822AR-REEL7	–40°C to +85°C	8-Lead SOIC	R-8	
AD822ARZ[1]	–40°C to +85°C	8-Lead SOIC	R-8	
AD822ARZ-REEL[1]	–40°C to +85°C	8-Lead SOIC	R-8	
AD822ARZ-REEL7[1]	–40°C to +85°C	8-Lead SOIC	R-8	
AD822ARM-R2	–40°C to +85°C	8-Lead MSOP	RM-8	B4A
AD822ARM-REEL	–40°C to +85°C	8-Lead MSOP	RM-8	B4A
AD822ARMZ-R2[1]	–40°C to +85°C	8-Lead MSOP	RM-8	#B4A
AD822ARMZ-REEL[1]	–40°C to +85°C	8-Lead MSOP	RM-8	#B4A
AD822BR	–40°C to +85°C	8-Lead SOIC	R-8	
AD822BR-REEL	–40°C to +85°C	8-Lead SOIC	R-8	
AD822BR-REEL7	–40°C to +85°C	8-Lead SOIC	R-8	
AD822BRZ[1]	–40°C to +85°C	8-Lead SOIC	R-8	
AD822BRZ-REEL[1]	–40°C to +85°C	8-Lead SOIC	R-8	
AD822BRZ-REEL7[1]	–40°C to +85°C	8-Lead SOIC	R-8	

[1] Z = Pb-free part, # denotes lead-free product may be top or bottom marked.

SPICE model is available at www.analog.com.

NOTES

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