SN54LS465 THRU SN54LS468, SN74LS465 THRU SN74LS468
OCTAL BUFFERS WITH 3-STATE OUTPUTS

SDLS179 – JANUARY 1981 – REVISED MARCH 1988

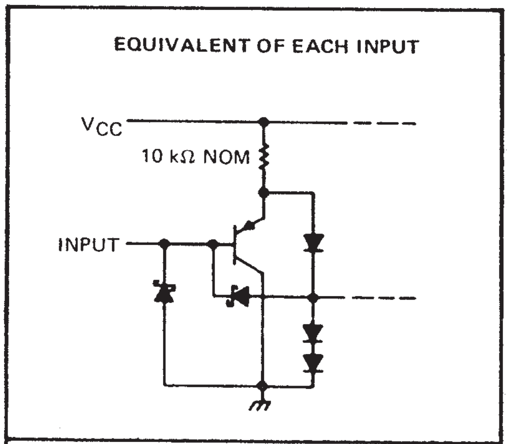
- **Mechanically and Functionally Interchangeable With DM71/81LS95 thru DM71/81LS98**
- **P-N-P Inputs Reduce Bus Loading**
- **3-State Outputs Rated at I_{OL} of 12 mA and 24 mA for 54LS and 74LS, Respectively**

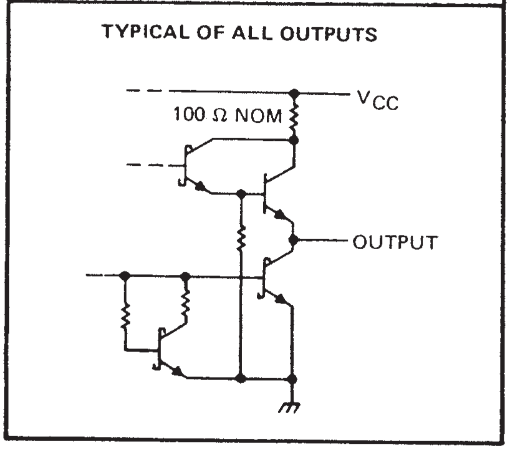
DEVICE	DATA PATH
'LS465	True
'LS466	Inverting
'LS467	True
'LS468	Inverting

description

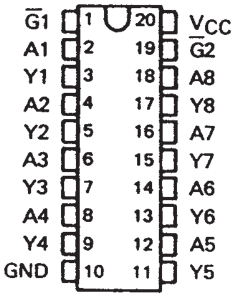
These octal buffers utilize the latest low-power Schottky technology. The 'LS465 and 'LS466 have a two-input active-low AND enable gate controlling all eight data buffers. The 'LS467 and 'LS468 have two separate active-low enable inputs each controlling four data buffers. In either case, a high level on any $\overline{G}$ places the affected outputs at high impedance.

schematics of inputs and outputs

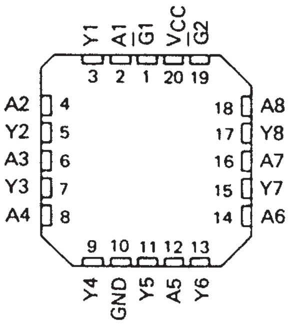

EQUIVALENT OF EACH INPUT


TYPICAL OF ALL OUTPUTS

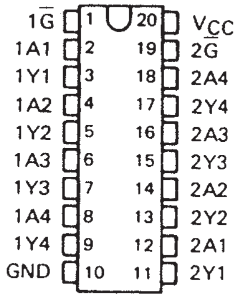
SN54LS465 AND SN54LS466 . . . J PACKAGE
SN74LS465 AND SN74LS466 . . . DW OR N PACKAGE
(TOP VIEW)



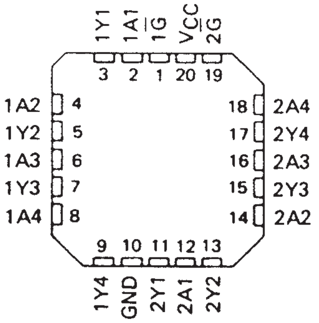
SN54LS465 AND SN54LS466 . . . FK PACKAGE
(TOP VIEW)



SN54LS467 AND SN54LS468 . . . J PACKAGE
SN74LS467 AND SN74LS468 . . . DW OR N PACKAGE
(TOP VIEW)



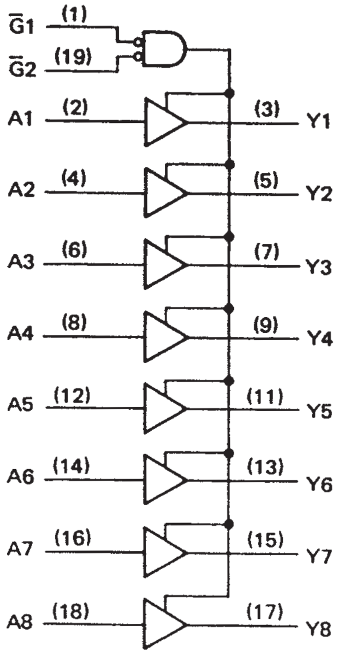
SN54LS467 AND SN54LS468 . . . FK PACKAGE
(TOP VIEW)



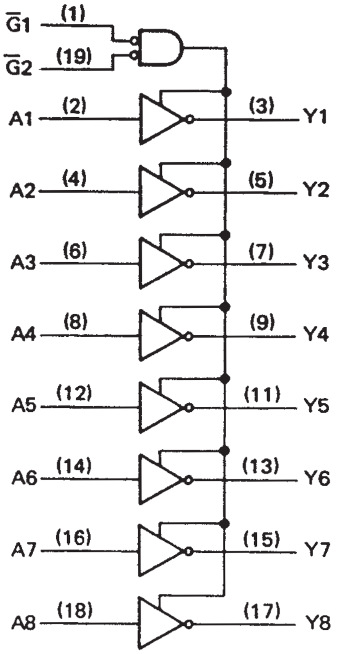
TEXAS INSTRUMENTS

logic diagrams (positive logic)

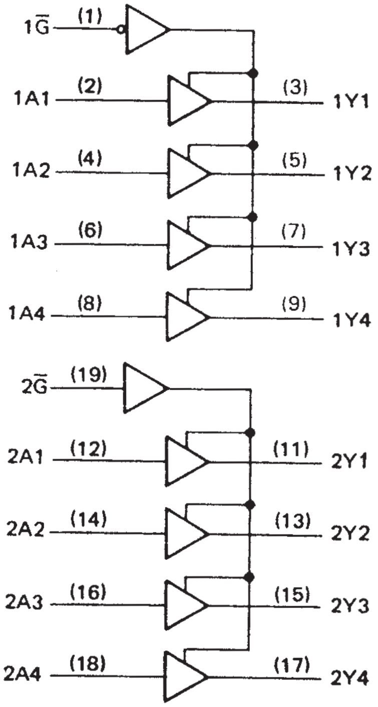
'LS465



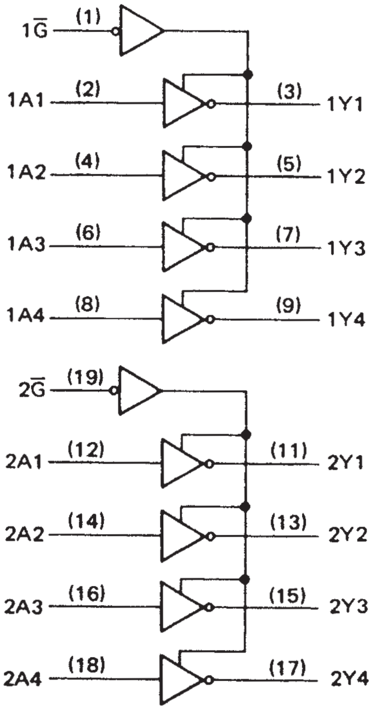
'LS466



'LS467



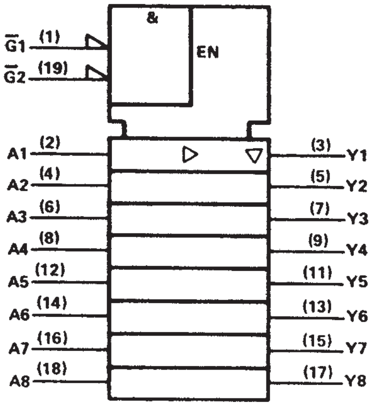
'LS468



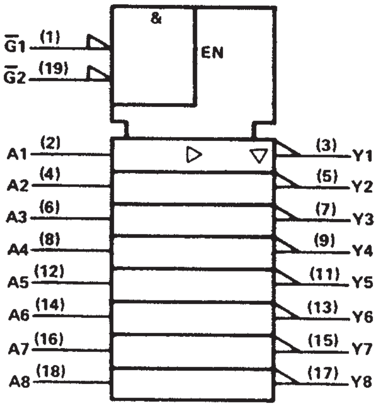
Pin numbers shown are for DW, J, and N packages.

logic symbols†

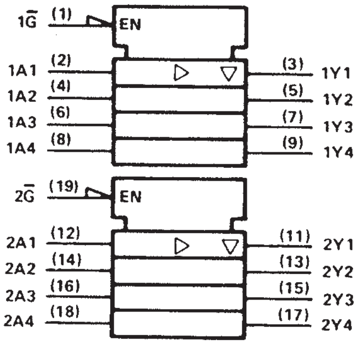
'LS465



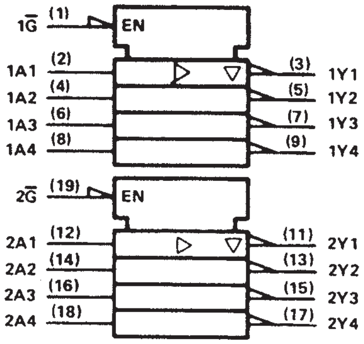
'LS466



'LS467



'LS468



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		7 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54LS465 thru SN54LS468	−55°C to 125°C
	SN74LS465 thru SN74LS468	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, $I_I = -18$ mA				−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, $V_{IL} = V_{IL}$ max	$I_{OH} = -1$ mA	2.4	3.3					V
			$I_{OH} = -2.6$ mA				2.4	3.1		
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, $V_{IL} = V_{IL}$ max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH} Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, $V_{IL} = V_{IL}$ max, V_O = 2.7 V				20			20	μA
I_{OZL} Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, $V_{IL} = V_{IL}$ max, V_O = 0.4 V				−20			−20	μA
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH} High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL} Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
I_{OS} Short-circuit output current§		V_{CC} = MAX, V_O = 0 V		−30		−130	−30		−130	mA
I_{CC} Supply current	'LS465, 'LS467	V_{CC} = MAX	Outputs low		19	32		19	32	mA
			Outputs high		13	22		13	22	
			Output Hi-Z		22	37		22	37	
	'LS466, 'LS468		Outputs low		14	23		14	23	
			Outputs high		6	10		6	10	
			Outputs Hi-Z		17	28		17	28	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS465, 'LS467			'LS466, 'LS468			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Ai	Yi	$R_L = 667\ \Omega$, C_L = 45 pF		9	15		7	12	ns
t_{PHL}	Ai	Yi			12	18		9	15	ns
t_{PZH}	$\overline{G}\downarrow$	Y			25	40		25	40	ns
t_{PZL}	$\overline{G}\downarrow$	Y			29	45		29	45	ns
t_{PHZ}	$\overline{G}\uparrow$	Y	$R_L = 667\ \Omega$, C_L = 5 pF		25	40		25	40	ns
t_{PLZ}	$\overline{G}\uparrow$	Y			30	45		30	45	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LS465DW	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS465DWE4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS465DWE4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS465DWG4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS465DWG4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS465N	NRND	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS465N	NRND	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS465NE4	NRND	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS465NE4	NRND	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS466DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74LS466DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74LS466N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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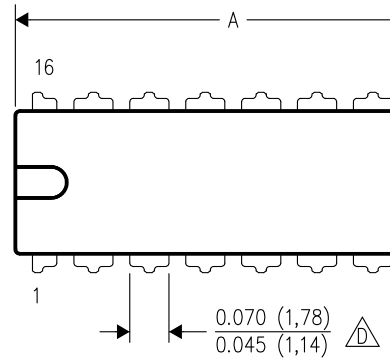
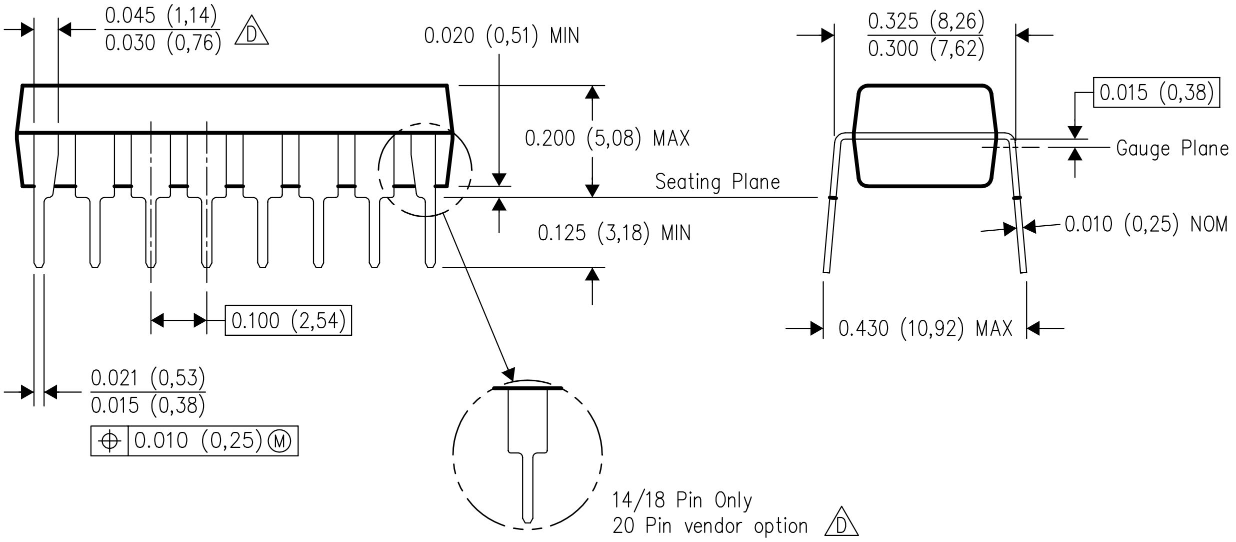
N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



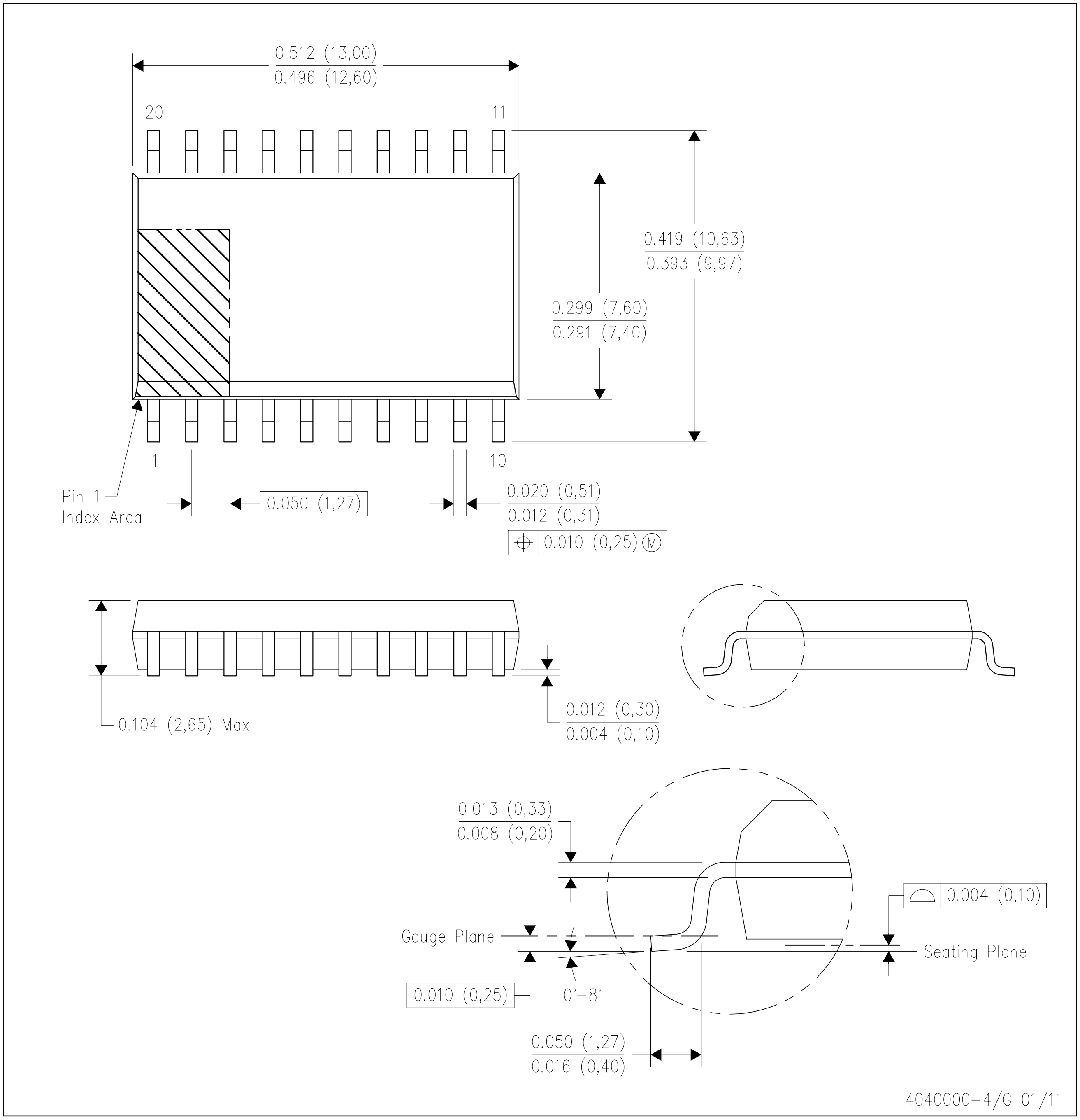
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

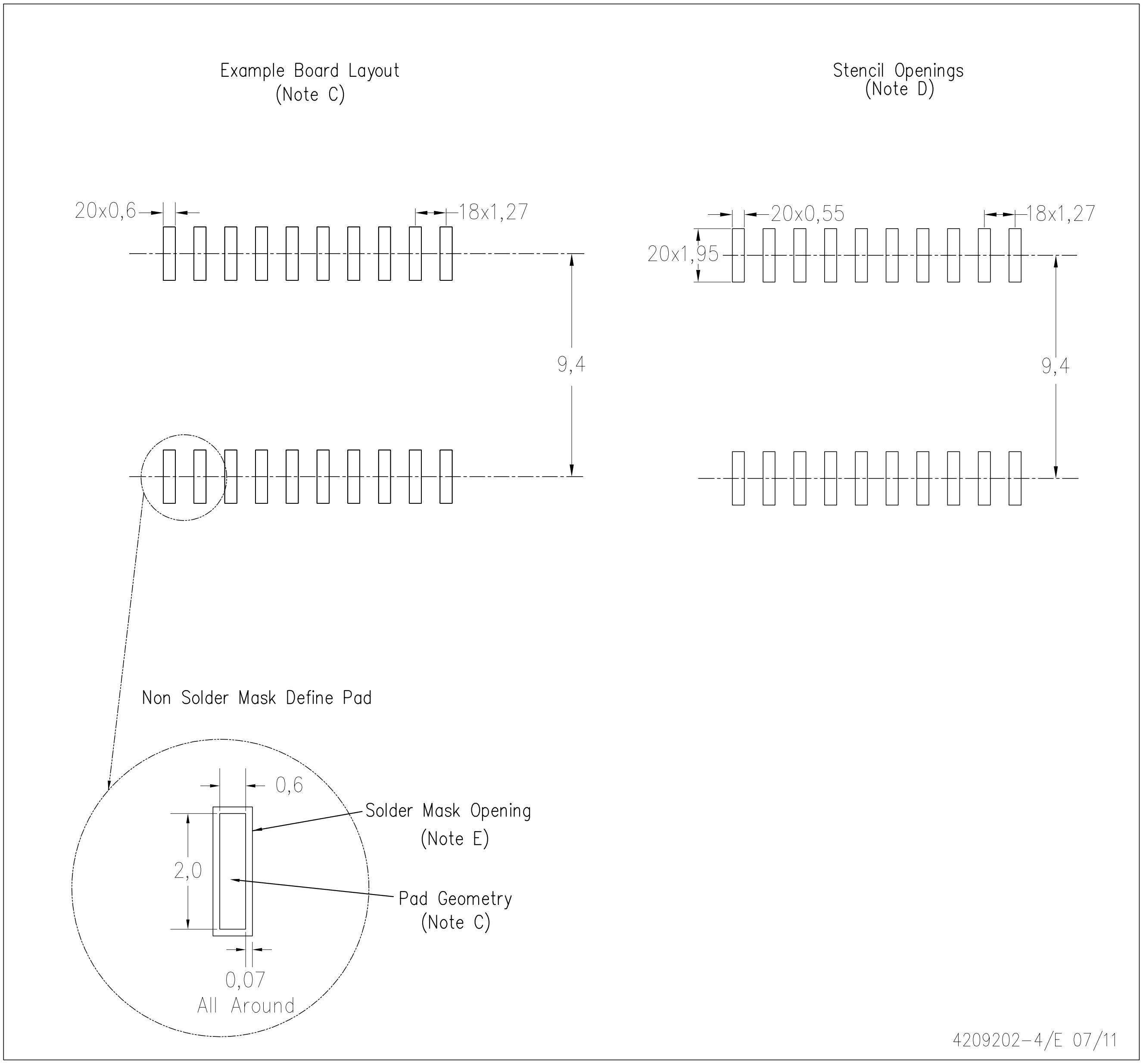
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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