

FQP13N50 / FQPF13N50

N-Channel QFET MOSFET

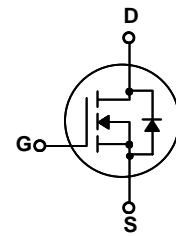
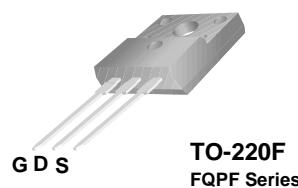
500 V, 12.5 A, 430 mΩ

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 12.5 A, 500 V, $R_{DS(on)} = 430 \text{ mΩ}$ (Max) @ $V_{GS} = 10 \text{ V}$, $I_D = 6.25 \text{ A}$
- Low Gate Charge (Typ. 45 nC)
- Low C_{rss} (Typ. 25 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQP13N50	FQPF13N50	Unit	
V_{DSS}	Drain-Source Voltage	500		V	
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	12.5	12.5 *	A	
	- Continuous ($T_C = 100^\circ\text{C}$)	7.9	7.9 *	A	
I_{DM}	Drain Current - Pulsed	(Note 1)	50	50 *	A
V_{GSS}	Gate-Source Voltage		± 30	V	
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	810	mJ	
I_{AR}	Avalanche Current	(Note 1)	12.5	A	
E_{AR}	Repetitive Avalanche Energy	(Note 1)	17	mJ	
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns	
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	170	56	W	
	- Derate above 25°C	1.35	0.45	W/ $^\circ\text{C}$	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$	
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	$^\circ\text{C}$	

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FQP13N50	FQPF13N50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.74	2.23	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.5	--	$^\circ\text{C}/\text{W}$

Electrical Characteristics						
$T_C = 25^\circ\text{C}$ unless otherwise noted						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	500	--	--	V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	--	0.48	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 500 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$	--	--	1	μA
		$V_{\text{DS}} = 400 \text{ V}$, $T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{\text{GS}} = 30 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{\text{GS}} = -30 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$	--	--	-100	nA
On Characteristics						
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 250 \mu\text{A}$	3.0	--	5.0	V
$R_{\text{DS(on)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}} = 10 \text{ V}$, $I_D = 6.25 \text{ A}$	--	0.33	0.43	Ω
g_{FS}	Forward Transconductance	$V_{\text{DS}} = 50 \text{ V}$, $I_D = 6.25 \text{ A}$ (Note 4)	--	10	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{\text{DS}} = 25 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$	--	1800	2300	pF
C_{oss}	Output Capacitance		--	245	320	pF
C_{rss}	Reverse Transfer Capacitance		--	25	35	pF
Switching Characteristics						
$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}} = 250 \text{ V}$, $I_D = 13.4 \text{ A}$, $R_G = 25 \Omega$	--	40	90	ns
t_r	Turn-On Rise Time		--	140	290	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		--	100	210	ns
t_f	Turn-Off Fall Time		--	85	180	ns
Q_g	Total Gate Charge	$V_{\text{DS}} = 400 \text{ V}$, $I_D = 13.4 \text{ A}$, $V_{\text{GS}} = 10 \text{ V}$	--	45	60	nC
Q_{gs}	Gate-Source Charge		--	11	--	nC
Q_{gd}	Gate-Drain Charge		--	22	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	12.5	--	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	50	--	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_S = 12.5 \text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{\text{GS}} = 0 \text{ V}$, $I_S = 13.4 \text{ A}$, $dI_F / dt = 100 \text{ A}/\mu\text{s}$	--	290	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.6	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 9.3\text{mH}$, $I_{AS} = 12.5\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25 \Omega$. Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 13.4\text{A}$, $dI/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq \text{BV}_{\text{DSS}}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

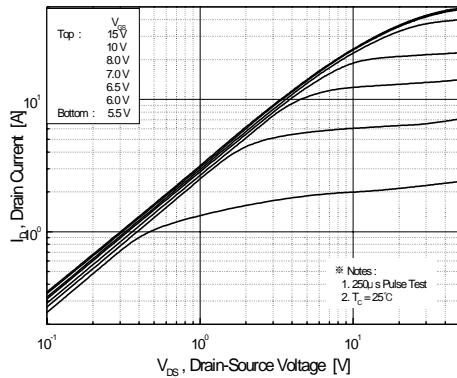


Figure 1. On-Region Characteristics

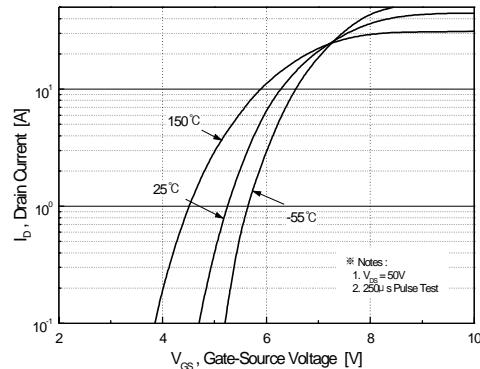


Figure 2. Transfer Characteristics

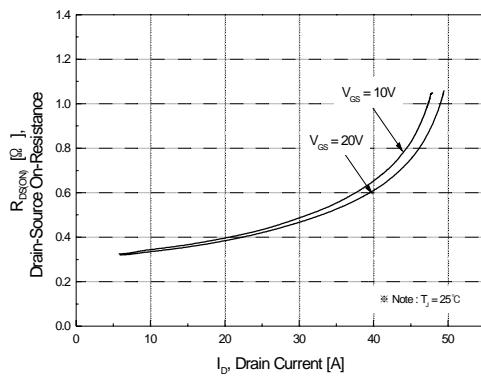


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

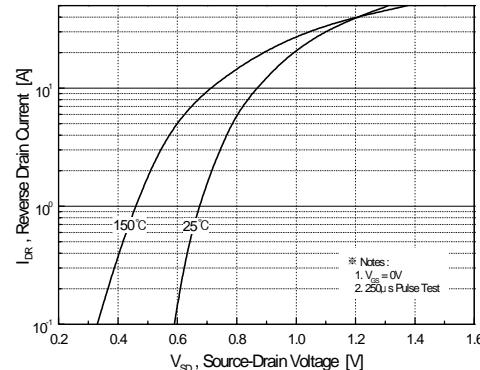


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

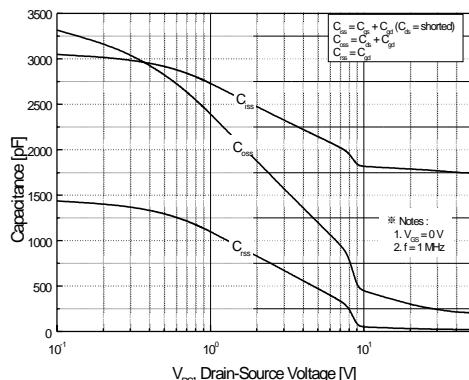


Figure 5. Capacitance Characteristics

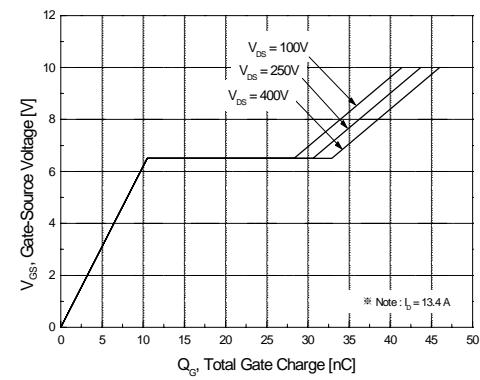


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

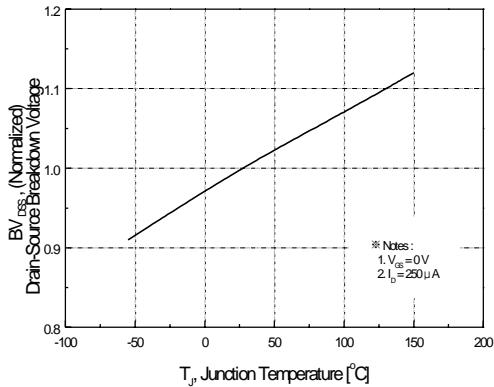


Figure 7. Breakdown Voltage Variation vs. Temperature

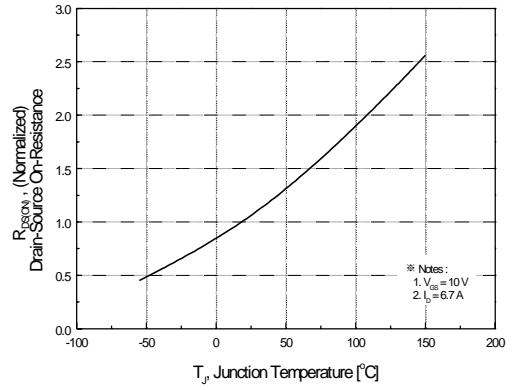


Figure 8. On-Resistance Variation vs. Temperature

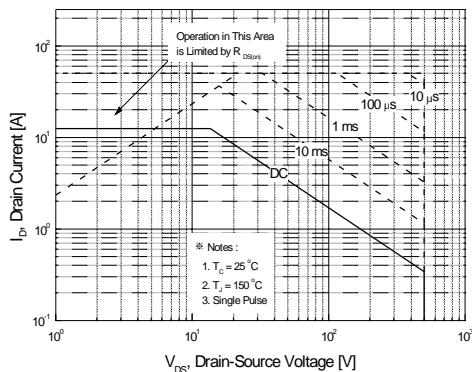


Figure 9-1. Maximum Safe Operating Area for FQP13N50

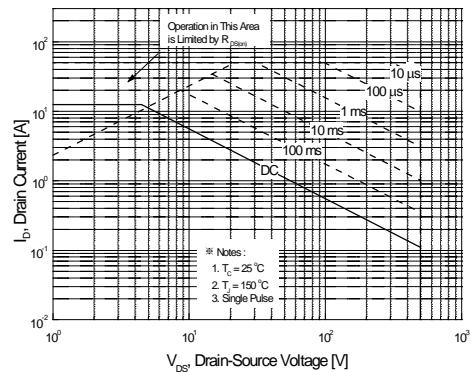


Figure 9-2. Maximum Safe Operating Area for FQPF13N50

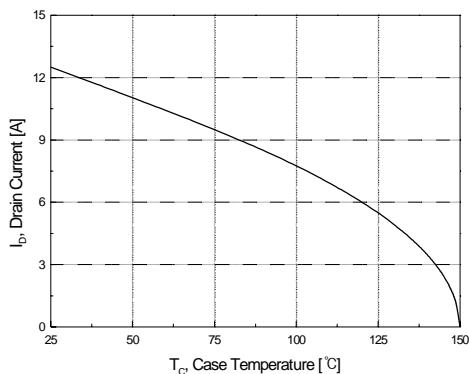


Figure 10. Maximum Drain Current vs. Case Temperature

Typical Characteristics (Continued)

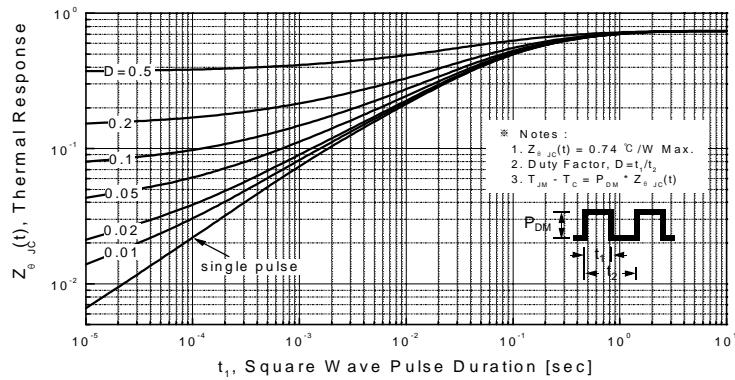


Figure 11-1. Transient Thermal Response Curve for FQP13N50

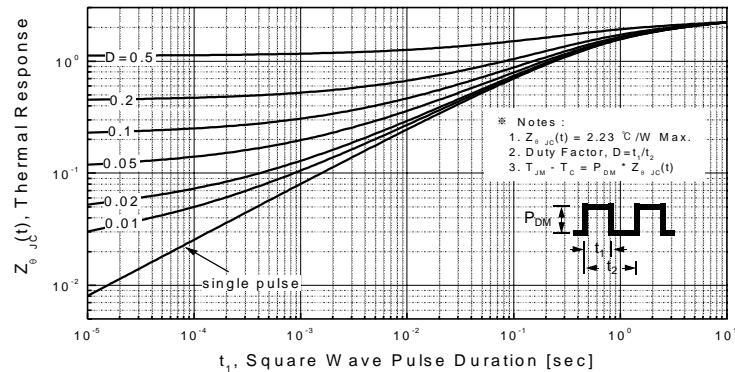
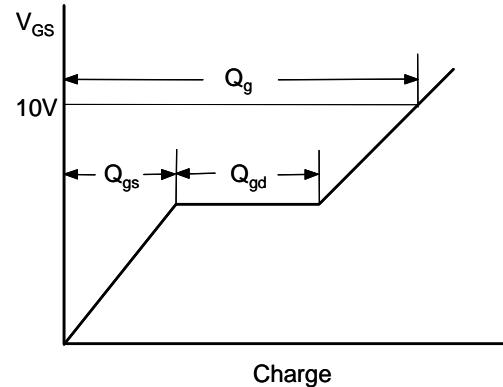
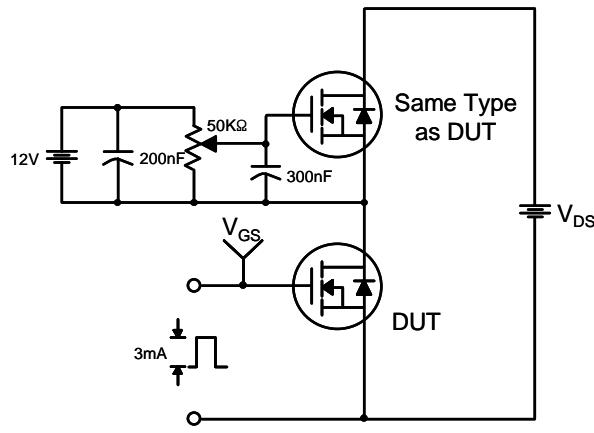
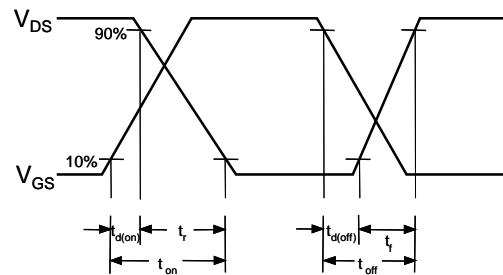
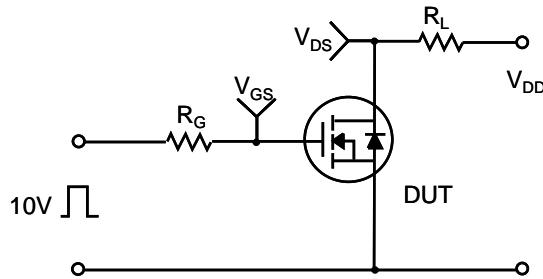


Figure 11. Transient Thermal Response Curve for FQPF13N50

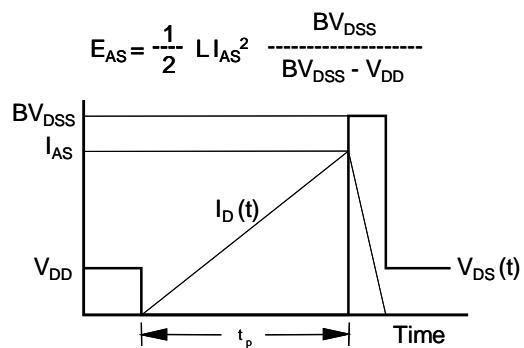
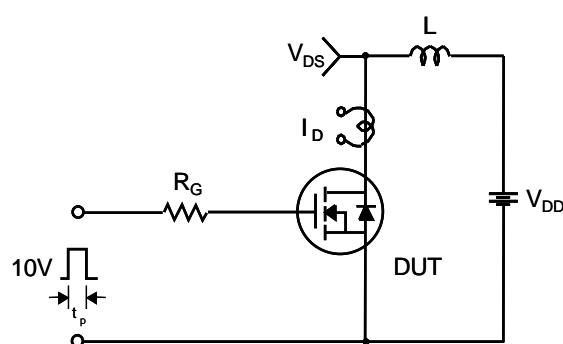
Gate Charge Test Circuit & Waveform



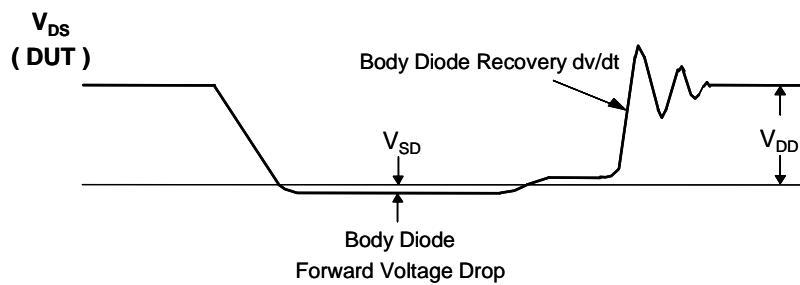
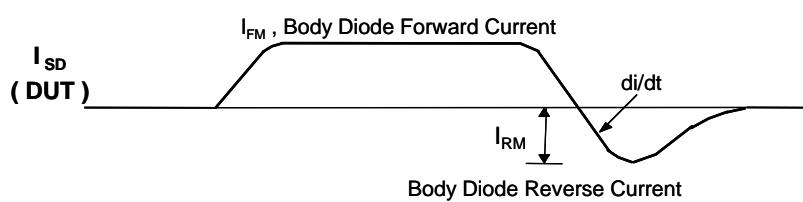
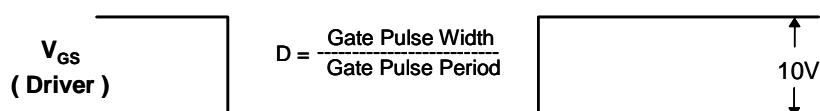
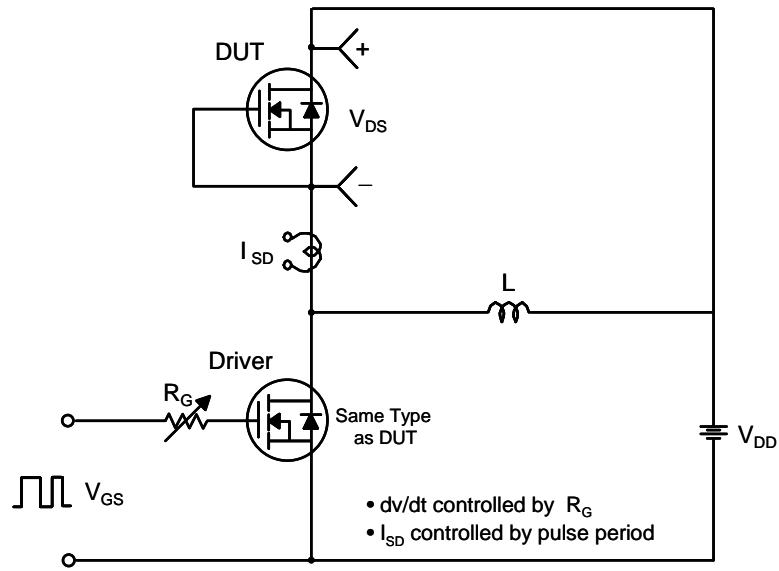
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

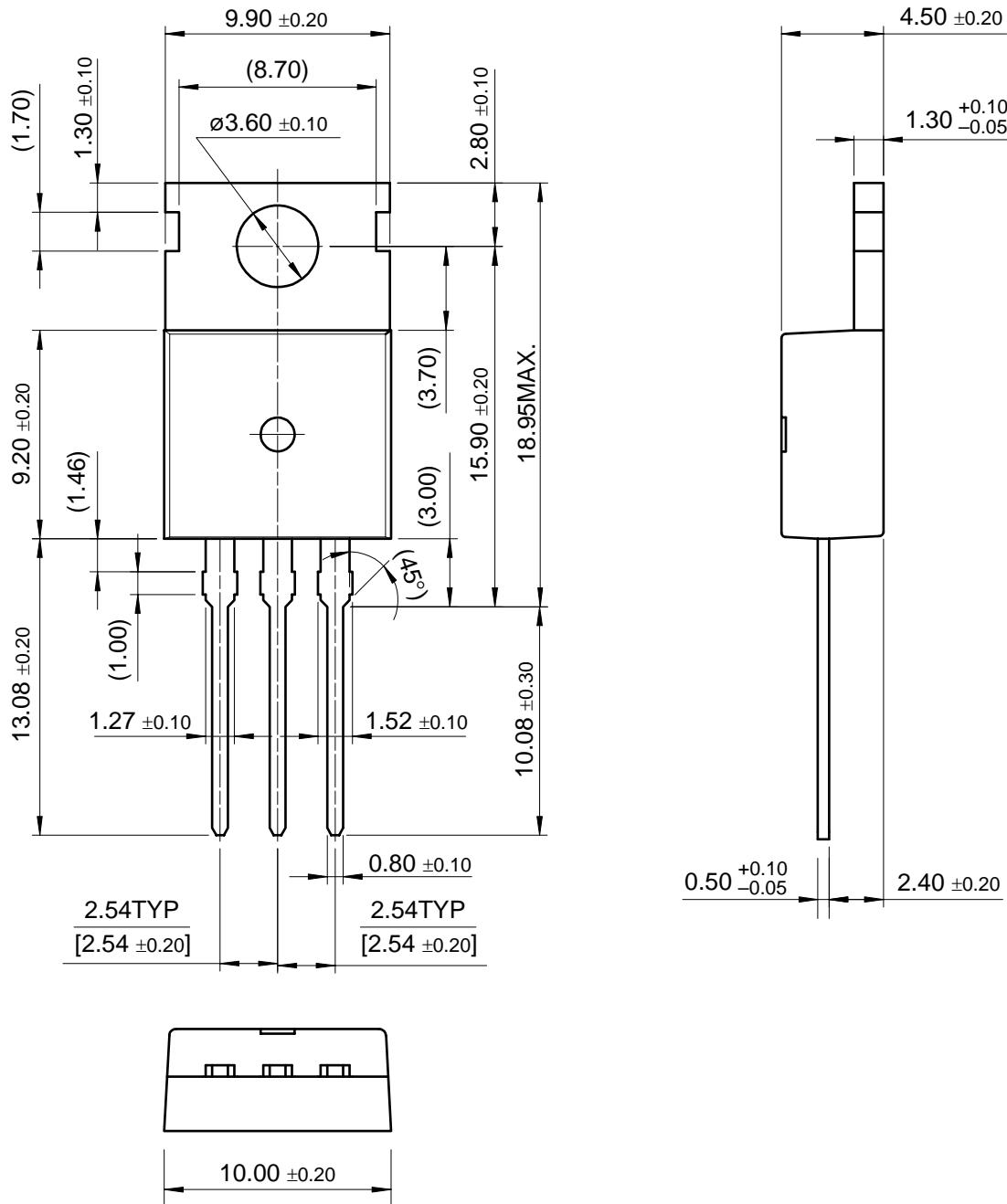


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

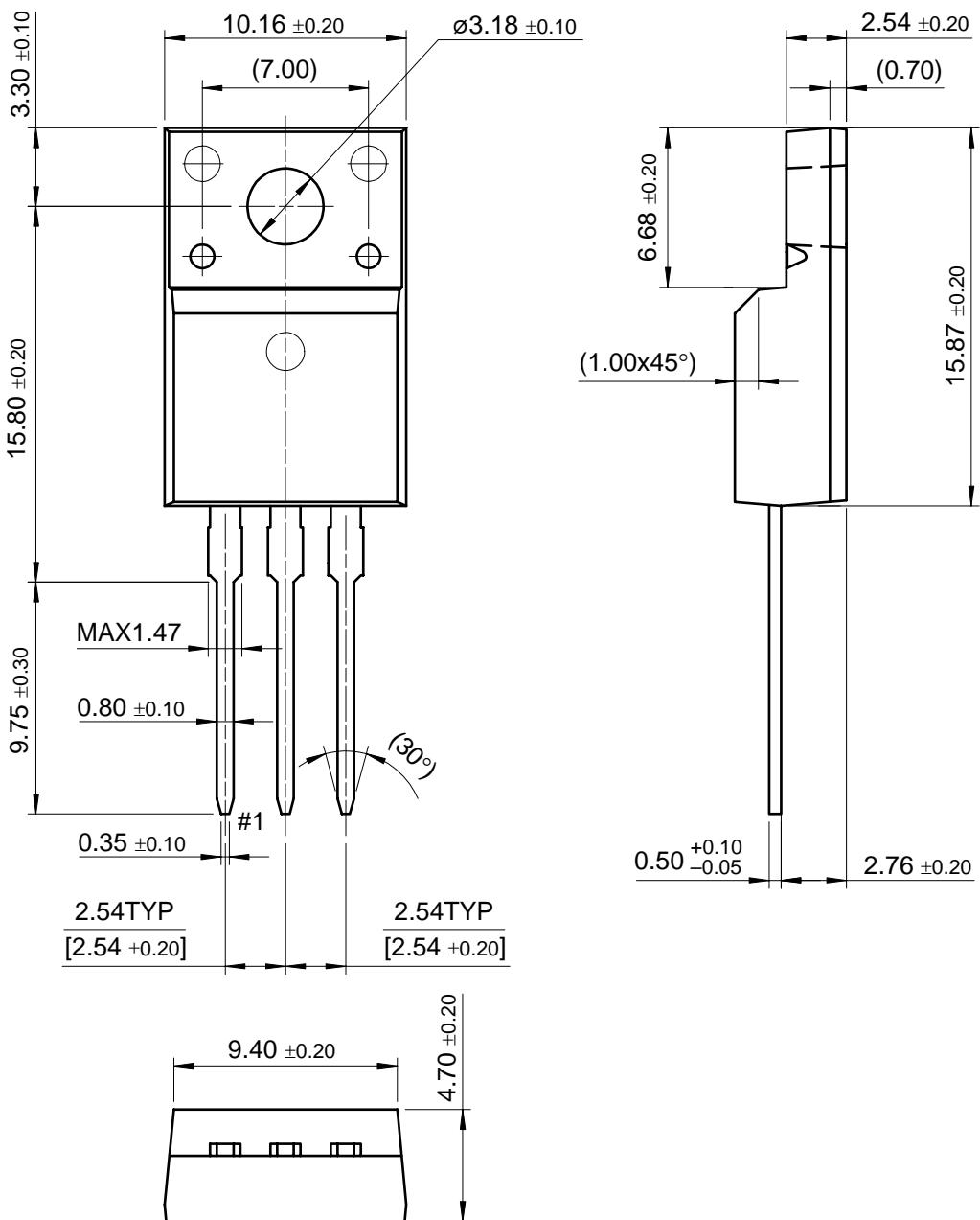
TO-220



Dimensions in Millimeters

Package Dimensions (Continued)

TO-220F



Dimensions in Millimeters

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PRODUCT STATUS

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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