SPANSION™ Flash Memory

Data Sheet

September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.

FLASH MEMORY

CMOS

4 M (512 K × 8/256 K × 16) BIT

MBM29DL400TC/BC-55/70/90

■ DESCRIPTION

The MBM29DL400TC/BC are a 4 M-bit, 3.0 V-only Flash memory organized as 512 Kbytes of 8 bits each or 256 Kwords of 16 bits each. The MBM29DL400TC/BC are offered in a 48-pin TSOP (I) package. These devices are designed to be programmed in-system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The devices can also be reprogrammed in standard EPROM programmers.
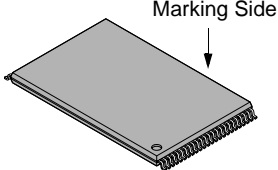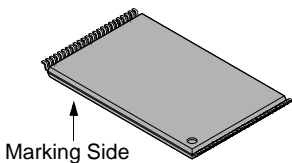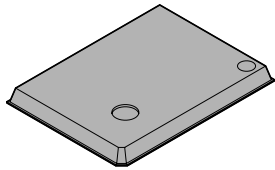
MBM29DL400TC/BC provides simultaneous operation which can read data while program/erase. The simultaneous operation architecture provides simultaneous operation by dividing the memory space into two banks. The devices can allow a host system to program or erase in one bank, then immediately and simultaneously read from the other bank.

(Continued)

■ PRODUCT LINE UP

Part No.	MBM29DL400TC/MBM29DL400BC		
	−55	**−70**	**−90**
Power Supply Voltage V_{CC} (V)	$3.3 \, ^{+0.3}_{-0.3}$		$3.0 \, ^{+0.6}_{-0.3}$
Max Address Access Time (ns)	55	70	90
Max $\overline{CE}$ Access Time (ns)	55	70	90
Max $\overline{OE}$ Access Time (ns)	30	30	35

■ PACKAGES

48-pin plastic TSOP (I)

Marking Side

(FPT-48P-M19)

48-pin plastic TSOP (I)

Marking Side

(FPT-48P-M20)

48-pin plastic FBGA

(BGA-48P-M11)

FUJITSU

(Continued)

The standard MBM29DL400TC/BC offer access times 55 ns, 70 ns and 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the devices feature separate chip enable ($\overline{CE}$) , write enable ($\overline{WE}$) , and output enable ($\overline{OE}$) controls.

The MBM29DL400TC/BC are pin and command set compatible with JEDEC standard E^{2}PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the devices is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29DL400TC/BC are programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the devices automatically time the erase pulse widths and verify proper cell margin.

One sector is typically erased and verified in 1.0 second. (If already completely preprogrammed.)

The devices also feature a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29DL400TC/BC are erased when shipped from the factory.
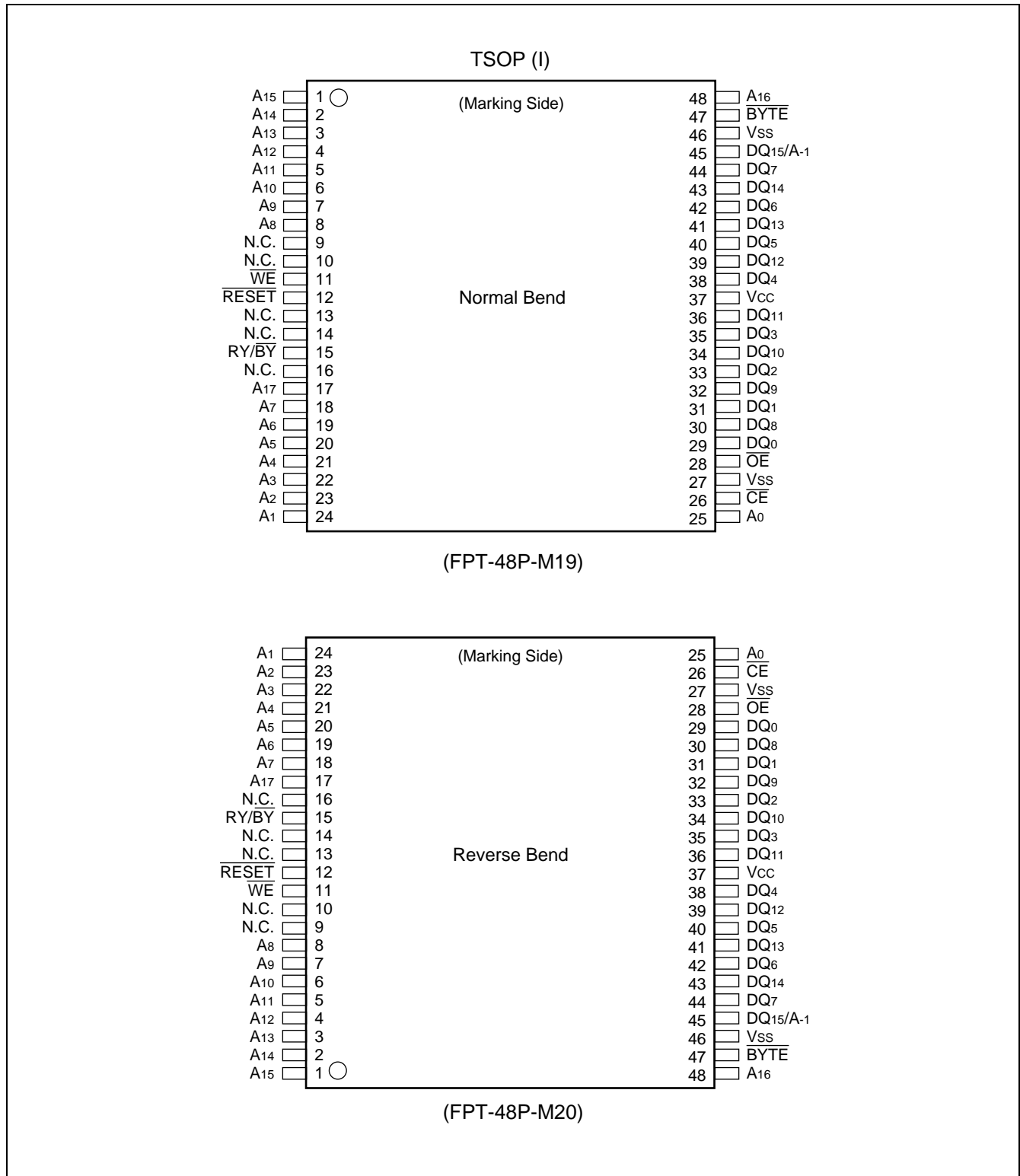
The devices feature single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, or the RY/$\overline{BY}$ output pin. Once the end of a program or erase cycle is completed, the devices internally reset to the read mode.

Fujitsu's Flash technology integrates years of EPROM and E2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29DL400TC/BC memories electrically erase the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.
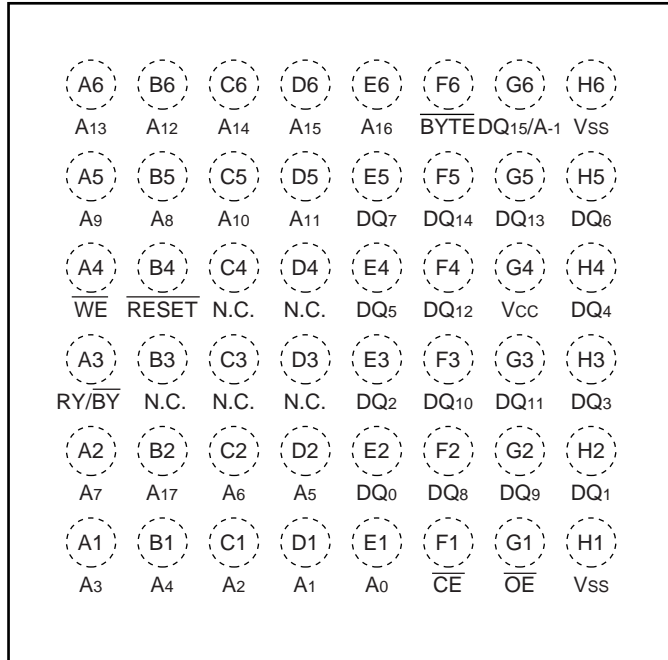
■ FEATURES

- **Single 3.0 V Read, Program, and Erase**
  Minimizes system level power requirements
- **Simultaneous Operations**
  Read-while-Erase or Read-while-Program
- **Compatible with JEDEC-standard Commands**
  Uses same software commands as E^{2}PROMs
- **Compatible with JEDEC-standard World-wide Pinouts (Pin Compatible with MBM29LV400TC/BC)**
  48-pin TSOP (I) (Package suffix : PFTN – Normal Bend Type, PFTR – Reversed Bend Type)
- **Minimum 100,000 Program/Erase Cycles**
- **High Performance**
  55 ns maximum access time
- **Sector Erase Architecture**
  Two 16 Kbyte, four 8 Kbytes, two 32 Kbyte, and six 64 Kbytes.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **Data Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion**
- **Ready/Busy Output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic Sleep Mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Low V$_{CC}$ Write Inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device
- **Sector Protection**
  Hardware method disables any combination of sectors from program or erase operations
- **Sector Protection Set function by Extended Sector Protection Command**
- **Fast Programming Function by Extended Command**
- **Temporary Sector Unprotection**
  Temporary sector unprotection via the $\overline{\text{RESET}}$ pin.

Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

■ PIN ASSIGNMENTS

TSOP (I)

(FPT-48P-M19) — Normal Bend (Marking Side)

Left pin	#		#	Right pin
A_{15}	1 ○		48	A_{16}
A_{14}	2		47	$\overline{BYTE}$
A_{13}	3		46	V_{SS}
A_{12}	4		45	DQ_{15}/A_{-1}
A_{11}	5		44	DQ_7
A_{10}	6		43	DQ_{14}
A_9	7		42	DQ_6
A_8	8		41	DQ_{13}
N.C.	9		40	DQ_5
N.C.	10		39	DQ_{12}
$\overline{WE}$	11		38	DQ_4
$\overline{RESET}$	12		37	V_{CC}
N.C.	13		36	DQ_{11}
N.C.	14		35	DQ_3
RY/$\overline{BY}$	15		34	DQ_{10}
N.C.	16		33	DQ_2
A_{17}	17		32	DQ_9
A_7	18		31	DQ_1
A_6	19		30	DQ_8
A_5	20		29	DQ_0
A_4	21		28	$\overline{OE}$
A_3	22		27	V_{SS}
A_2	23		26	$\overline{CE}$
A_1	24		25	A_0

(FPT-48P-M19)

(FPT-48P-M20) — Reverse Bend (Marking Side)

Left pin	#		#	Right pin
A_1	24		25	A_0
A_2	23		26	$\overline{CE}$
A_3	22		27	V_{SS}
A_4	21		28	$\overline{OE}$
A_5	20		29	DQ_0
A_6	19		30	DQ_8
A_7	18		31	DQ_1
A_{17}	17		32	DQ_9
N.C.	16		33	DQ_2
RY/$\overline{BY}$	15		34	DQ_{10}
N.C.	14		35	DQ_3
N.C.	13		36	DQ_{11}
$\overline{RESET}$	12		37	V_{CC}
$\overline{WE}$	11		38	DQ_4
N.C.	10		39	DQ_{12}
N.C.	9		40	DQ_5
A_8	8		41	DQ_{13}
A_9	7		42	DQ_6
A_{10}	6		43	DQ_{14}
A_{11}	5		44	DQ_7
A_{12}	4		45	DQ_{15}/A_{-1}
A_{13}	3		46	V_{SS}
A_{14}	2		47	$\overline{BYTE}$
A_{15}	1 ○		48	A_{16}

(FPT-48P-M20)

(Continued)

FBGA
(TOP VIEW)
(Making Side)

A6	B6	C6	D6	E6	F6	G6	H6
A_{13}	A_{12}	A_{14}	A_{15}	A_{16}	$\overline{BYTE}$	DQ_{15}/A_{-1}	V_{SS}
A5	B5	C5	D5	E5	F5	G5	H5
A_9	A_8	A_{10}	A_{11}	DQ_7	DQ_{14}	DQ_{13}	DQ_6
A4	B4	C4	D4	E4	F4	G4	H4
$\overline{WE}$	$\overline{RESET}$	N.C.	N.C.	DQ_5	DQ_{12}	V_{CC}	DQ_4
A3	B3	C3	D3	E3	F3	G3	H3
$RY/\overline{BY}$	N.C.	N.C.	N.C.	DQ_2	DQ_{10}	DQ_{11}	DQ_3
A2	B2	C2	D2	E2	F2	G2	H2
A_7	A_{17}	A_6	A_5	DQ_0	DQ_8	DQ_9	DQ_1
A1	B1	C1	D1	E1	F1	G1	H1
A_3	A_4	A_2	A_1	A_0	$\overline{CE}$	$\overline{OE}$	V_{SS}

(BGA-48P-M11)

■ PIN DESCRIPTION

MBM29DL400TC/BC Pin Configuration

Pin Name	Function
A_{17} to A_0, A_{-1}	Address Inputs
DQ_{15} to DQ_0	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready/Busy Output
$\overline{RESET}$	Hardware Reset
$\overline{BYTE}$	8-bit or 16-bit mode
N.C.	No Connection
V_{SS}	Ground
V_{CC}	Power Supply

■ BLOCK DIAGRAM
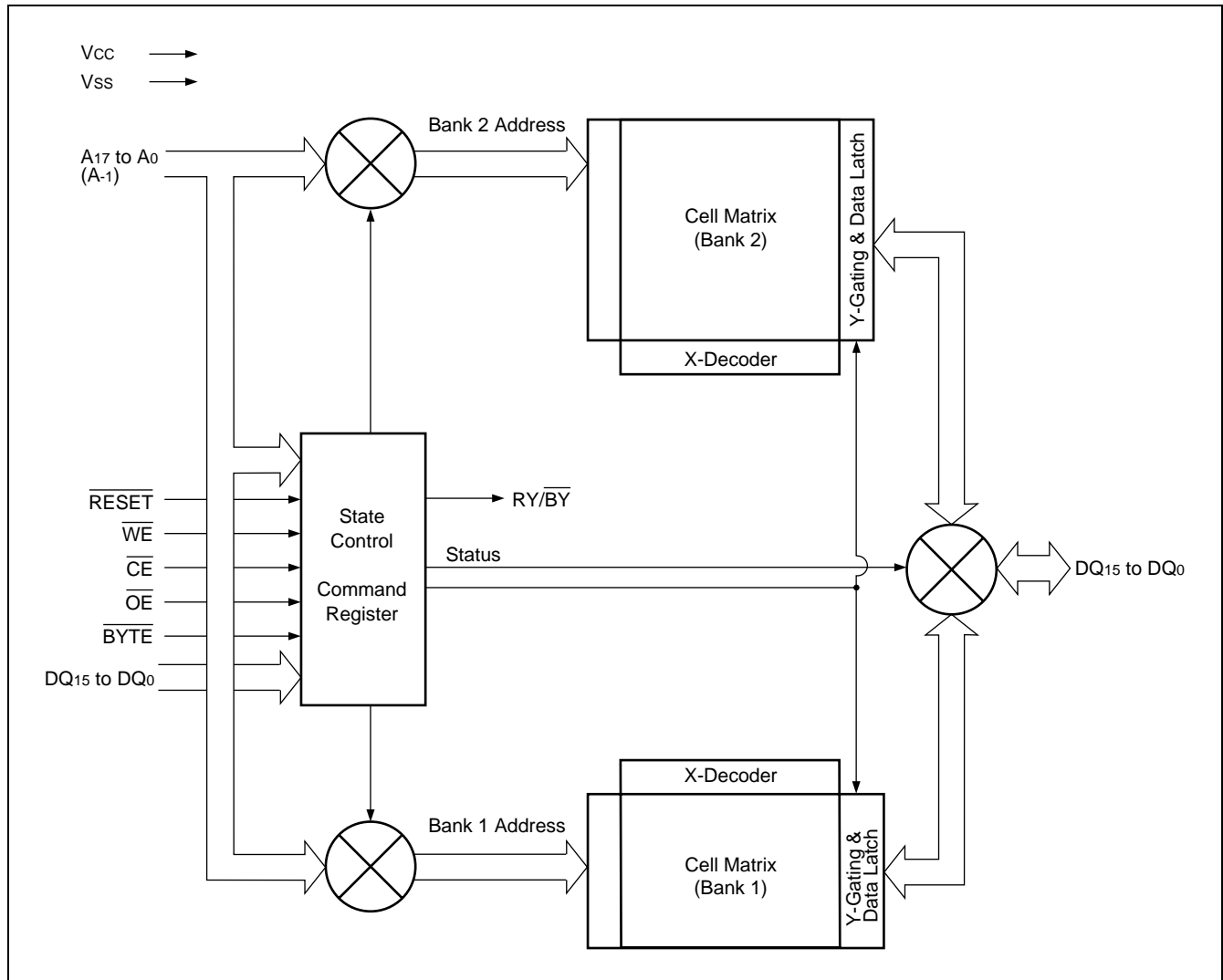
■ LOGIC SYMBOL
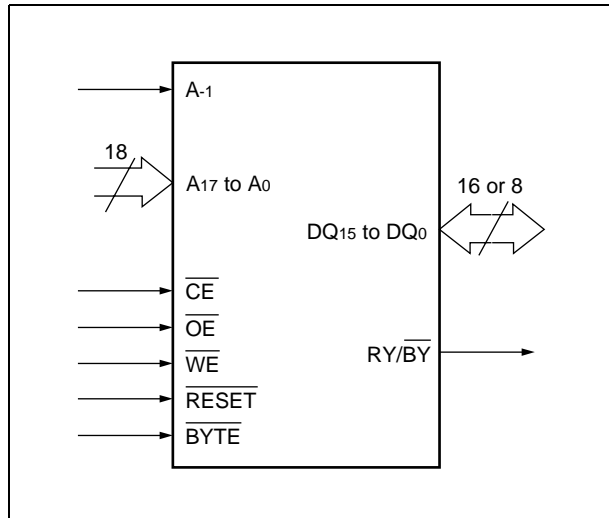
MBM29DL400TC/BC-55/70/90

■ DEVICE BUS OPERATION

MBM29DL400TC/BC User Bus Operations ($\overline{\text{BYTE}}$ = V_{IH})

Operation	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A_0	A_1	A_6	A_9	DQ_{15} to DQ_0	$\overline{\text{RESET}}$
Auto-Select Manufacturer Code [1]	L	L	H	L	L	L	V_{ID}	Code	H
Auto-Select Device Code [1]	L	L	H	H	L	L	V_{ID}	Code	H
Read [3]	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	High-Z	H
Write (Program/Erase)	L	H	L	A_0	A_1	A_6	A_9	D_{IN}	H
Enable Sector Protection [2], [4]	L	V_{ID}	⌐‾	L	H	L	V_{ID}	X	H
Verify Sector Protection [2], [4]	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotection [5]	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware) /Standby	X	X	X	X	X	X	X	High-Z	L

MBM29DL400TC/BC User Bus Operations ($\overline{\text{BYTE}}$ = V_{IL})

Operation	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	DQ_{15}/ A_{-1}	A_0	A_1	A_6	A_9	DQ_7 to DQ_0	$\overline{\text{RESET}}$
Auto-Select Manufacturer Code [1]	L	L	H	L	L	L	L	V_{ID}	Code	H
Auto-Select Device Code [1]	L	L	H	L	H	L	L	V_{ID}	Code	H
Read [3]	L	L	H	A_{-1}	A_0	A_1	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	X	High-Z	H
Write (Program/Erase)	L	H	L	A_{-1}	A_0	A_1	A_6	A_9	D_{IN}	H
Enable Sector Protection [2], [4]	L	V_{ID}	⌐‾	L	L	H	L	V_{ID}	X	H
Verify Sector Protection [2], [4]	L	L	H	L	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotection [5]	X	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware) /Standby	X	X	X	X	X	X	X	X	High-Z	L

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, ⌐‾ = Pulse input. See "■DC CHARACTERISTICS" for voltage levels.

[1]: Manufacturer and device codes may also be accessed via command register write sequence. See "MBM29DL400TC/BC Command Definitions" Table.

[2]: Refer to the section on Sector Protection.

[3]: $\overline{\text{WE}}$ can be V_{IL} if $\overline{\text{OE}}$ is V_{IL}, $\overline{\text{OE}}$ at V_{IH} initiates the write operations.

[4]: V_{CC} = 3.3 V ± 10%

[5]: Also used for the extended sector protection.

MBM29DL400TC/BC Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	Word	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
	Byte													
Read/Reset	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Autoselect	Word	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
	Byte		AAAh		555h		(BA) AAAh							
Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh		555h		AAAh		AAAh		555h		AAAh	
Sector Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Erase Suspend		1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume		1	BA	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Fast Program *	Word	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
	Byte		XXXh											
Reset from Fast Mode *	Word	2	BA	90h	XXXh	F0h	—	—	—	—	—	—	—	—
	Byte		BA		XXXh									
Extended Sector Protect	Word	4	XXXh	60h	SPA	60h	SPA	40h	SPA	SD	—	—	—	—
	Byte													

* : This command is valid while Fast Mode.

Notes : 1. Address bits A_{17} to $A_{11} = X =$ "H" or "L" for all address commands except or Program Address (PA) , Sector Address (SA) , and Bank Address (BA) .

2. Bus operations are defined in "MBM29DL400TC/BC User Bus Operations ($\overline{BYTE} = V_{IH}$) and ($\overline{BYTE} = V_{IL}$)" Tables.

3. RA = Address of the memory location to be read
PA = Address of the memory location to be programmed
Addresses are latched on the falling edge of the write pulse.
SA = Address of the sector to be erased. The combination of A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
BA = Bank Address (A_{16} and A_{17})

4. RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.

5. SPA = Sector address to be protected. Set sector address (SA) and $(A_6, A_1, A_0) = (0, 1, 0)$.
SD = Sector protection verify data. Output 01h at protected sector addresses and output 00h at unprotected sector addresses.
6. The system should generate the following address patterns :
Word Mode : 555h or 2AAh to addresses A_0 to A_{10}
Byte Mode : AAAh or 555h to addresses A_{-1} and A_0 to A_{10}
7. Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
8. Command combinations not described in "MBM29DL400TC/BC Command Definitions" Table are illegal.

MBM29DL400TC/BC Sector Protection Verify Autoselect Codes

Type			A_{12} to A_{17}	A_6	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacture's Code			BA	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	MBM29DL400TC	Byte	BA	V_{IL}	V_{IL}	V_{IH}	V_{IL}	0Ch
		Word					X	220Ch
	MBM29DL400BC	Byte	BA	V_{IL}	V_{IL}	V_{IH}	V_{IL}	0Fh
		Word					X	220Fh
Sector Protection			Sector Addresses	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01h*2

*1 : A_{-1} is for Byte mode.

*2 : Outputs 01h at protected sector address and outputs 00h at unprotected sector address.

Expanded Autoselect Code Table

Type			Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer's Code			04h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29DL 400TC	(B)	0Ch	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	0	0	0	1	1	0	0
		(W)	220Ch	0	0	1	0	0	0	1	0	0	0	0	0	1	1	0	0
	MBM29DL 400BC	(B)	0Fh	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	0	0	0	1	1	1	1
		(W)	220Fh	0	0	1	0	0	0	1	0	0	0	0	0	1	1	1	1
Sector Protection			01h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B) : Byte mode
(W) : Word mode
HI-Z : High-Z

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

Sector Address Table (MBM29DL400TC)

Bank	Sector	Sector Address						Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		Bank Address								
		A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}			
Bank 2	SA0	0	0	0	X	X	X	64/32	00000h to 0FFFFh	00000h to 07FFFh
	SA1	0	0	1	X	X	X	64/32	10000h to 1FFFFh	08000h to 0FFFFh
	SA2	0	1	0	X	X	X	64/32	20000h to 2FFFFh	10000h to 17FFFh
	SA3	0	1	1	X	X	X	64/32	30000h to 3FFFFh	18000h to 1FFFFh
	SA4	1	0	0	X	X	X	64/32	40000h to 4FFFFh	20000h to 27FFFh
	SA5	1	0	1	X	X	X	64/32	50000h to 5FFFFh	28000h to 2FFFFh
Bank 1	SA6	1	1	0	0	0	X	16/8	60000h to 63FFFh	30000h to 31FFFh
	SA7	1	1	0	0 / 1	1 / 0	X	32/16	64000h to 67FFFh 68000h to 6BFFFh	32000h to 33FFFh 34000h to 35FFFh
	SA8	1	1	0	1	1	0	8/4	6C000h to 6DFFFh	36000h to 36FFFh
	SA9	1	1	0	1	1	1	8/4	6E000h to 6FFFFh	37000h to 37FFFh
	SA10	1	1	1	0	0	0	8/4	70000h to 71FFFh	38000h to 38FFFh
	SA11	1	1	1	0	0	1	8/4	72000h to 73FFFh	39000h to 39FFFh
	SA12	1	1	1	0 / 1	1 / 0	X	32/16	74000h to 77FFFh 78000h to 7BFFFh	3A000h to 3BFFFh 3C000h to 3DFFFh
	SA13	1	1	1	1	1	X	16/8	7C000h to 7FFFFh	3E000h to 3FFFFh

Note : The address range is A_{17} : A_{-1} if in byte mode ($\overline{BYTE} = V_{IL}$) .
The address range is A_{17} : A_0 if in word mode ($\overline{BYTE} = V_{IH}$) .

Sector Address Table (MBM29DL400BC)

Bank	Sector	Sector Address						Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		Bank Address								
		A$_{17}$	A$_{16}$	A$_{15}$	A$_{14}$	A$_{13}$	A$_{12}$			
Bank 2	SA13	1	1	1	X	X	X	64/32	70000h to 7FFFFh	38000h to 3FFFFh
	SA12	1	1	0	X	X	X	64/32	60000h to 6FFFFh	30000h to 37FFFh
	SA11	1	0	1	X	X	X	64/32	50000h to 5FFFFh	28000h to 2FFFFh
	SA10	1	0	0	X	X	X	64/32	40000h to 4FFFFh	20000h to 27FFFh
	SA9	0	1	1	X	X	X	64/32	30000h to 3FFFFh	18000h to 1FFFFh
	SA8	0	1	0	X	X	X	64/32	20000h to 2FFFFh	10000h to 17FFFh
Bank 1	SA7	0	0	1	1	1	X	16/8	1C000h to 1FFFFh	0E000h to 0FFFFh
	SA6	0	0	1	1	0	X	32/16	14000h to 17FFFh, 18000h to 1BFFFh	0A000h to 0BFFFh, 0C000h to 0DFFFh
					0	1	X			
	SA5	0	0	1	0	0	1	8/4	12000h to 13FFFh	09000h to 09FFFh
	SA4	0	0	1	0	0	0	8/4	10000h to 11FFFh	08000h to 08FFFh
	SA3	0	0	0	1	1	1	8/4	0E000h to 0FFFFh	07000h to 07FFFh
	SA2	0	0	0	1	1	0	8/4	0C000h to 0DFFFh	06000h to 06FFFh
	SA1	0	0	0	1	0	X	32/16	08000h to 0BFFFh, 04000h to 07FFFh	04000h to 05FFFh, 02000h to 03FFFh
					0	1	X			
	SA0	0	0	0	0	0	X	16/8	00000h to 03FFFh	00000h to 01FFFh

Note : The address range is A$_{17}$: A$_{-1}$ if in byte mode ($\overline{BYTE}$ = V$_{IL}$) .
The address range is A$_{17}$: A$_0$ if in word mode ($\overline{BYTE}$ = V$_{IH}$) .

MBM29DL400TC

16 KB	7FFFFh
32 KB	7C000h
8 KB	74000h
8 KB	72000h
8 KB	70000h
8 KB	6E000h
32 KB	6C000h
16 KB	64000h
64 KB	60000h
64 KB	50000h
64 KB	40000h
64 KB	30000h
64 KB	20000h
64 KB	10000h
	00000h

Bank 1 (top portion), Bank 2 (bottom portion)

MBM29DL400BC

64 KB	7FFFFh
64 KB	70000h
64 KB	60000h
64 KB	50000h
64 KB	40000h
64 KB	30000h
16 KB	20000h
32 KB	1C000h
8 KB	14000h
8 KB	12000h
8 KB	10000h
8 KB	0E000h
32 KB	0C000h
16 KB	04000h
	00000h

Bank 2 (top portion), Bank 1 (bottom portion)
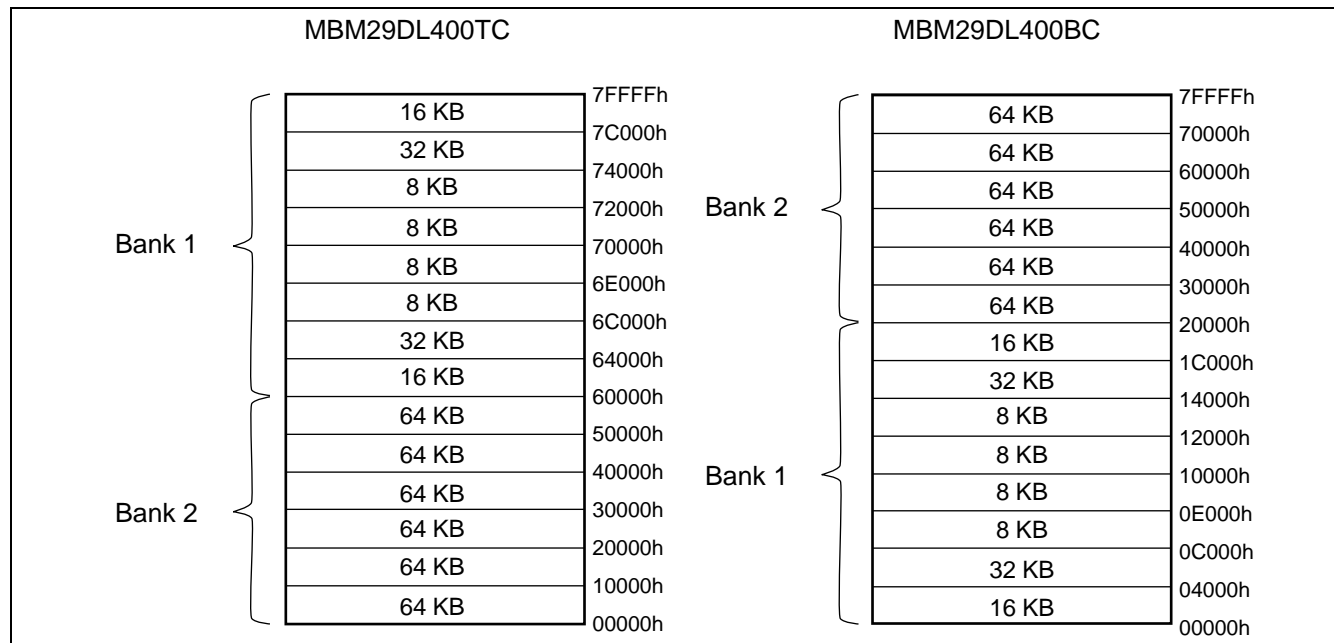
■ FUNCTIONAL DESCRIPTION

Simultaneous Operation

MBM29DL400TC/BC features reading data from one bank of memory while either programming or erase oper-ation is in progress in the other bank of memory (simultaneous operation) , in addition to the conventional features (read, program, erase, erase-suspend read, and erase-suspend program) . The bank selection can be selected by bank address (A_{16}, A_{17}) with zero latency.

The MBM29DL400TC/BC have two banks which contain Bank 1 (16 KB, 32 KB, 8 KB, 8 KB, 8 KB, 8 KB, 32 KB, and 16 KB) and Bank 2 (64 KB × six sectors) .

The simultaneous operation can not execute multi-function mode in the same bank. "Simultaneous Operation" Table shows combination to be possible for simultaneous operation.

Simultaneous Operation

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode *
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode *	Read mode

* : Erase operation may also be supended to read from or program to a sector not being erased.

Read Mode

The MBM29DL400TC/BC have two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins. (Assuming the addresses have been stable for at least t_{ACC}-t_{OE} time.) When reading out a data without changing addresses after power-up, it is necessary to input hardware reset or to change $\overline{CE}$ pin from "H" to "L"

Standby Mode

There are two ways to implement the standby mode on the MBM29DL400TC/BC devices, one using both the $\overline{CE}$ and $\overline{RESET}$ pins; the other via the $\overline{RESET}$ pin only.

When using both pins, a CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ inputs both held at $V_{CC} \pm 0.3$ V. Under this condition the current consumed is less than 5 μA Max During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even $\overline{CE}$ = "H". The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the $\overline{RESET}$ pin only, a CMOS standby mode is achieved with $\overline{RESET}$ input held at $V_{SS} \pm 0.3$ V ($\overline{CE}$ = "H" or "L") . Under this condition the current is consumed is less than 5 μA Max Once the $\overline{RESET}$ pin is taken high, the device requires t_{RH} of wake up time before outputs are valid for read access.

In the standby mode the outputs are in the high impedance state, independent of the $\overline{OE}$ input.

Automatic Sleep Mode

There is a function called automatic sleep mode to restrain power consumption during read-out of MBM29DL400TC/BC data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To activate this mode, MBM29DL400TC/BC automatically switch themselves to low power mode when MBM29DL400TC/BC addresses remain stably during access fine of 150 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ on the mode. Under the mode, the current consumed is typically 1 μA (CMOS Level) .

During simultaneous operation, V_{CC} active current (I_{CC2}) is required.

Since the data are latched during this mode, the data are read-out continuously. If the addresses are changed, the mode is canceled automatically and MBM29DL400TC/BC read-out the data for changed addresses.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}) , output from the devices is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the devices and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the devices to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the devices.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A_9. Two identifier bytes may then be sequenced from the devices outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are DON'T CARES except A_0, A_1, and A_6 (A_{-1}) . (See "MBM29DL400TC/BC User Bus Operations ($\overline{BYTE}$ = V_{IH}) and ($\overline{BYTE}$ = V_{IL})" Tables in "■DEVICE BUS OPERATION".)

The manufacturer and device codes may also be read via the command register, for instances when the MBM29DL400TC/BC are erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in "MBM29DL400TC/BC Command Definitions" Table in "■DEVICE BUS OPERATION". (Refer to Autoselect Command section.)

Word 0 (A_0 = V_{IL}) represents the manufacturer's code (Fujitsu = 04h) and word 1 (A_0 = V_{IH}) represents the device identifier code (MBM29DL400TC = 0Ch and MBM29DL400BC = 0Fh for ×8 mode; MBM29DL400TC = 220Ch and MBM29DL400BC = 220Fh for ×16 mode) . These two bytes/words are given in the "MBM29DL400TC/BC Sector Protection Verify Autoselect Codes" and "Expanded Autoselect Code" Tables in "■DEVICE BUS OPERATION". All identifiers for manufactures and device will exhibit odd parity with DQ_7 defined as the parity bit. In order to read the proper device codes when executing the autoselect, A_1 must be V_{IL}. (See "MBM29DL400TC/BC Sector Protection Verify Autoselect Codes" and "Expanded Autoselect Code" Tables in "■DEVICE BUS OPERATION".)

In case of applying V_{ID} on A_9, since both Bank 1 and Bank 2 enters Autoselect mode, the simultenous operation can not be executed.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

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Sector Protection

The MBM29DL400TC/BC feature hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 13) . The sector protection feature is enabled using programming equipment at the user's site. The devices are shipped with all sectors unprotected. Alternatively, Fujitsu may program and protect sectors in the factory prior to shiping the device.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, (suggest V_{ID} = 11.5 V) , $\overline{CE}$ = V_{IL}, and A_0 = A_6 = V_{IL}, A_1 = V_{IH}. The sector addresses (A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) should be set to the sector to be protected. MBM29DL400TC/BC's "Sector Address" Tables in "■FLEXIBLE SECTOR-ERASE ARCHITECTURE" define the sector address for each of the forteen (14) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. See "Sector Protection Timing Diagram" in "■TIMING DIAGRAM" and "Sector Protection Algorithm" in "■FLOW CHART" for sector protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" code at device output DQ_0 for a protected sector. Otherwise the devices will read 00h for unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, and A_6 are DON'T CARES. Address locations with A_1 = V_{IL} are reserved for Autoselect manufacturer and device codes. A_{-1} requires to apply to V_{IL} on byte mode.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the higher order addresses (A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) are the desired sector address will produce a logical "1" at DQ_0 for a protected sector. See "MBM29DL400TC/BC Sector Protection Verify Autoselect Codes" and "Expanded Autoselect Code" Tables in "■DEVICE BUS OPERATION" for Autoselect codes.

Temporary Sector Unprotection

This feature allows temporary unprotection of previously protected sectors of the MBM29DL400TC/BC devices in order to change data. The Sector Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage (12 V) . During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the 12 V is taken away from the $\overline{RESET}$ pin, all the previously protected sectors will be protected again. See "Temporary Sector Unprotection Timing Diagram" in "■TIMING DIAGRAM" and "Temporary Sector Unprotection Algorithm" in "■FLOW CHART".

$\overline{RESET}$
Hardware Reset

The MBM29DL400TC/BC devices may be reset by driving the $\overline{RESET}$ pin to V_{IL}. The $\overline{RESET}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least 500 ns in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode 20 μs after the $\overline{RESET}$ pin is driven low. Furthermore, once the $\overline{RESET}$ pin goes high, the devices require an additional t_{RH} before it will allow read access. When the $\overline{RESET}$ pin is low, the devices will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/$\overline{BY}$ output signal should be ignored during the $\overline{RESET}$ pulse. See "$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram" in "■TIMING DIAGRAM" for the timing diagram. Refer to Temporary Sector Unprotection for additional functionality.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Some commands are required Bank Address (BA) input. When command sequences are inputed to bank being read, the commands have priority than reading. "Hardware Sequence Flags" Table defines the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Moreover both Read/Reset commands are functionally equivalent, reset-

ting the device to the read mode. Please note that commands are always written at DQ_0 to DQ_7 and DQ_8 to DQ_{15} bits are ignored.

Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits ($DQ_5 = 1$) to Read/Reset mode, the Read/Reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The devices remain enabled for reads until the command register contents are altered.

The devices will automatically power-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the devices reside in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address (BA) and the Autoselect command. Then the manufacture and device codes can be read from the bank, and an actual data of memory cell can be read from the another bank.

Following the command write, a read cycle from address (BA) 00h retrieves the manufacture code of 04h. A read cycle from address (BA) 01h for $\times$16 ((BA) 02h for $\times$8) returns the device code (MBM29DL400TC = 0Ch and MBM29DL400BC = 0Fh for $\times$8 mode; MBM29DL400TC = 220Ch and MBM29DL400BC = 220Fh for $\times$16 mode) . (See "MBM29DL400TC/BC Sector Protection Verify Autoselect Codes" and "Expanded Autoselect Code" Tables in "■DEVICE BUS OPERATION".)

All manufacturer and device codes will exhibit odd parity with DQ_7 defined as the parity bit. Sector state (protection or unprotection) will be informed by address (BA) 02h for $\times$16 ((BA) 04h for $\times$8) . Scanning the sector addresses (A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) $=$ $(0, 1, 0)$ will produce a logical "1" at device output DQ_0 for a protected sector. The programming verification should be performed by verify sector protection on the protected sector. (See "MBM29DL400TC/BC User Bus Operations ($\overline{BYTE}$ = V_{IH}) and ($\overline{BYTE}$ = V_{IL})" Tables in "■DEVICE BUS OPERATION".)

The manufacture and device codes can be allowed reading from selected bank. To read the manufacture and device codes and sector protection status from non-selected bank, it is necessary to write Read/Reset command sequence into the register and then Autoselect command should be written into the bank to be read.

If the software (program code) for Autoselect command is stored into the Frash memory, the device and manufacture codes should be read from the other bank where is not contain the software.

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register, and also to write the Autoselect command during the operation, execute it after writing Read/Reset command sequence.

Byte/Word Programming

The devices are programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

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The system can determine the status of the program operation by using DQ_7 ($\overline{Data}$ Polling) , DQ_6 (Toggle Bit) , or RY/$\overline{BY}$. The $\overline{Data}$ Polling and Toggle Bit must be performed at the memory location which is being programmed.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which time the devices return to the read mode and addresses are no longer latched. (See "Hardware Sequence Flags" Table.) Therefore, the devices require that a valid address to the devices be supplied by the system at this particular instance of time. Hence, $\overline{Data}$ Polling must be performed at the memory location which is being programmed.

If hardware reset occurs during the programming operation, it is impossible to guarantee the data are being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Read/Reset mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

"Embedded Program™ Algorithm" in "■FLOW CHART" illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the devices will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase (Preprogram function) . The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{Data}$ Polling) , DQ_6 (Toggle Bit) , or RY/$\overline{BY}$. The chip erase begins on the rising edge of the last $\overline{CE}$ or $\overline{WE}$, whichever happens first in the command sequence and terminates when the data on DQ_7 is "1" (See Write Operation Status section.) at which time the device returns to read the mode.

Chip Erase Time; Sector Erase Time × All sectors + Chip Program Time (Preprogramming)

"Embedded Erase™ Algorithm" in "■FLOW CHART" illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever happens later, while the command (Data = 30h) is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ which happens first. After time-out of 50 μs from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on "MBM29DL400TC/BC Command Definitions" Table in "■DEVICE BUS OPERATION". This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 50 μs otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 50 μs from the rising edge of last $\overline{CE}$ or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command (s) . If another falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first occurs within the 50 μs time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, Sector Erase Timer.) Resetting the devices once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 13) .

Sector erase does not require the user to program the devices prior to erase. The devices automatically program all memory locations in the sector (s) to be erased prior to electrical erase (Preprogram function) . When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{Data}$ Polling) , DQ_6 (Toggle Bit) , or RY/$\overline{BY}$.

The sector erase begins after the 50 μs time out from the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever happens first for the last sector erase command pulse and terminates when the data on DQ_7 is "1" (See Write Operation Status section.) at which time the devices return to the read mode. $\overline{Data}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)] × Number of Sector Erase

In case of multiple sector erase across bank boundaries, a read from bank (read-while-erase) can not performe.

"Embedded Erase™ Algorithm" in "■FLOW CHART" illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. Writting the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30h) resumes the erase operation. The bank addresses of sector being erasing or suspending should be set when writting the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 20 μs to suspend the erase operation. When the devices have entered the erase-suspended mode, the RY/$\overline{BY}$ output pin will be at Hi-Z and the DQ_7 bit will be at logic "1", and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the devices default to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on DQ_2.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the devices are in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the RY/$\overline{BY}$ output pin, $\overline{Data}$ polling of DQ_7 or by the Toggle Bit I (DQ_6) which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address within bank being erase-suspended.

To resume the operation of Sector Erase, the Resume command (30h) should be written to the bank being erase suspended. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Extended Command

(1) Fast Mode

MBM29DL400TC/BC has Fast Mode function. This mode dispenses with the initial two unclock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. (Do not write erase command in this mode.) The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register. The first cycle must contain the bank address. (Refer to the "Embedded Programming Algorithm for Fast Mode" in "■FLOW CHART" Extended algorithm.) The V_{CC} active current is required even $\overline{CE} = V_{IH}$ during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD) . (Refer to the "Embedded Programming Algorithm for Fast Mode" in "■FLOW CHART" Extended algorithm.)

(3) Extended Sector Protection

In addition to normal sector protection, the MBM29DL400TC/BC has Extended Sector Protection as extended function. This function enable to protect sector by forcing V_{ID} on $\overline{RESET}$ pin and write a commnad sequence. Unlike conventional procedure, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{RESET}$ pin requires V_{ID} for sector protection in this mode. The extended sector protect requires V_{ID} on $\overline{RESET}$ pin. With this condition, the operation is initiated by writing the set-up command (60h) into the command register. Then, the sector addresses pins (A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set to the sector to be protected (recommend to set V_{IL} for the other addresses pins) , and write extended sector protect command (60h) . A sector is typically protected in 150 μs. To verify programming of the protection circuitry, the sector addresses pins (A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set and write a command (40h) . Following the command write, a logical "1" at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical "0", please repeat to write extended sector protect command (60h) again. To terminate the operation, it is necessary to set $\overline{RESET}$ pin to V_{IH}.

Write Operation Status

Detailed in "Hardware Sequence Flags" Table are all the status flags that can determine the status of the bank for the current mode operation. The read operation from the bank where is not operate Embedded Algorithm returns a data of memory cell. These bits offer a method for determining whether a Embedded Algorithm is completed properly. The information on DQ_2 is address sensitive. This means that if an address from an erasing sector is consectively read, then the DQ_2 bit will toggle. However, DQ_2 will not toggle if an address from a non-erasing sector is consectively read. This allows the user to determine which sectors are erasing and which are not.

The status flag is not output from bank (non-busy bank) not executing Embedded Algorithm. For example, there is bank (busy bank) which is now executing Embedded Algorithm. When the read sequence is [1] < busy bank > , [2] < non-busy bank > , [3] < busy bank > , the DQ_6 is toggling in the case of [1] and [3]. In case of [2], the data of memory cell is outputted. In the erase-suspend read mode with the same read sequence, DQ_6 will not be toggled in the [1] and [3].

In the erase suspend read mode, DQ_2 is toggled in the [1] and [3]. In case of [2], the data of memory cell is outputted.

Hardware Sequence Flags

Status			DQ$_7$	DQ$_6$	DQ$_5$	DQ$_3$	DQ$_2$
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle*
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	0	0	1*
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A

* : Successive reads from the erasing or erase-suspend sector will cause DQ$_2$ to toggle. Reading from non-erase suspend sector address will indicate logic "1" at the DQ$_2$ bit.

Notes : 1. DQ$_0$ and DQ$_1$ are reserve pins for future use.
2. DQ$_4$ is Fujitsu internal use only.

DQ$_7$
$\overline{\text{Data}}$ Polling

The MBM29DL400TC/BC devices feature $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the devices will produce the complement of the data last written to DQ$_7$. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ$_7$. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ$_7$ output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ$_7$ output. The flowchart for $\overline{\text{Data}}$ Polling (DQ$_7$) is shown in "$\overline{\text{Data}}$ Polling Algorithm" in "■FLOW CHART".

For programming, the $\overline{\text{Data}}$ Polling is valid after the rising edge of fourth write pulse in the four write pulse sequence.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at sector address within any of the sectors being erased and not a protected sector. Otherwise, the status may not be valid.

If a program address falls within a protected sector, $\overline{\text{Data}}$ Polling on DQ$_7$ is active for approximately 1 µs, then that bank returns to the read mode. After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on DQ$_7$ is active for approximately 100 µs, then the bank returns to read mode.

Once the Embedded Algorithm operation is close to being completed, the MBM29DL400TC/BC data pins (DQ$_7$) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the devices are driving status information on DQ$_7$ at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ$_7$ output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ$_7$ has a valid data, the data outputs on DQ$_6$ to DQ$_0$ may be still invalid. The valid data on DQ$_7$ to DQ$_0$ will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. (See "Hardware Sequence Flags" Table.)

See "$\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram" in "■TIMING DIAGRAM" for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ$_6$
Toggle Bit I

The MBM29DL400TC/BC also feature the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the devices will result in DQ$_6$ toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ$_6$ will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequence. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 1 μs and then stop toggling without the data having changed. In erase, the devices will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 μs and then drop back into read mode, having changed none of the data.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ$_6$ to toggle. In addition, an Erase Suspend/Resume command will cause the DQ$_6$ to toggle.

The system can use DQ$_6$ to determine whether a sector is actively erasing or is erase-suspended. When a bank is actively erasing (that is, the Embedded Erase Algorithm is in progress) , DQ$_6$ toggles. When a bank enters the Erase Suspend mode, DQ$_6$ stops toggling. Successive read cycles during the erase-suspend-program cause DQ$_6$ to toggle.

To operate toggle bit function properly, $\overline{\text{CE}}$ or $\overline{\text{OE}}$ must be high when bank address is changed.

See "AC Waveforms for Toggle Bit I during Embedded Algorithm Operations" in "■TIMING DIAGRAM" for the Toggle Bit I timing specifications and diagrams.

DQ$_5$
Exceeded Timing Limits

DQ$_5$ will indicate if the program or erase time has exceeded the specified limits (internal pulse count) . Under these conditions DQ$_5$ will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the devices under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA) . The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in "MBM29DL400TC/BC User Bus Operations ($\overline{\text{BYTE}}$ = V$_{\text{IH}}$) and ($\overline{\text{BYTE}}$ = V$_{\text{IL}}$)" Tables in "■DEVICE BUS OPERATIONS".

The DQ$_5$ failure condition may also appear if a user tries to program a non blank location without erasing. In this case the devices lock out and never complete the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ$_7$ bit and DQ$_6$ never stops toggling. Once the devices have exceeded timing limits, the DQ$_5$ bit will indicate a "1." Please note that this is not a device failure condition since the devices were incorrectly used. If this occurs, reset the device with command sequence.

DQ$_3$
Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ$_3$ will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ$_3$ may be used to determine if the sector erase timer window is still open. If DQ$_3$ is high ("1") the internally controlled erase cycle has begun. If DQ$_3$ is low ("0") the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ$_3$ prior to and following each subsequent Sector Erase command. If DQ$_3$ were high on the second status check, the command may not have been accepted.

See "Hardware Sequence Flags" Table.

DQ$_2$
Toggle Bit II

This toggle bit II, along with DQ$_6$, can be used to determine whether the devices are in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ$_2$ to toggle during the Embedded Erase Algorithm. If the devices are in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ$_2$ to toggle. When the devices are in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic "1" at the DQ$_2$ bit.

DQ$_6$ is different from DQ$_2$ in that DQ$_6$ toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ$_7$, is summarized as follows :

For example, DQ$_2$ and DQ$_6$ can be used together to determine if the erase-suspend-read mode is in progress. (DQ$_2$ toggles while DQ$_6$ does not.) See also "Hardware Sequence Flags" Table and "DQ$_2$ vs. DQ$_6$" in "■TIMING DIAGRAM".

Furthermore, DQ$_2$ can also be used to determine which sector is being erased. When the device is in the erase mode, DQ$_2$ toggles if this bit is read from an erasing sector.

To operate toggle bit function properly, $\overline{CE}$ or $\overline{OE}$ must be high when bank address is changed.

Mode	DQ$_7$	DQ$_6$	DQ$_2$
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle*
Erase-Suspend Read (Erase-Suspended Sector) *	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle	1*

* : Successive reads from the erasing or erase-suspend sector will cause DQ$_2$ to toggle. Reading from non-erase suspend sector address will indicate logic "1" at the DQ$_2$ bit.

RY/$\overline{BY}$
Ready/Busy

The MBM29DL400TC/BC provide a RY/$\overline{BY}$ open-drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the devices are busy with either a program or erase operation. If the output is high, the devices are ready to accept any read/write or erase operation. If the MBM29DL400TC/BC are placed in an Erase Suspend mode, the RY/$\overline{BY}$ output will be high.

During programming, the RY/$\overline{BY}$ pin is driven low after the rising edge of the fourth write pulse. During an erase operation, the RY/$\overline{BY}$ pin is driven low after the rising edge of the sixth write pulse. The RY/$\overline{BY}$ pin will indicate a ready condition during the $\overline{RESET}$ pulse. Refer to "RY/$\overline{BY}$ Timing Diagram during Program/Erase Operation Timing Diagram" and "$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram" in "■TIMING DIAGRAM" for a detailed timing diagram. The RY/$\overline{BY}$ pin is pulled high in standby mode.

Since this is an open-drain output, RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to V$_{CC}$.

Byte/Word Configuration

The $\overline{\text{BYTE}}$ pin selects the byte (8-bit) mode or word (16-bit) mode for the MBM29DL400TC/BC devices. When this pin is driven high, the devices operate in the word (16-bit) mode. The data is read and programmed at DQ_{15} to DQ_0. When this pin is driven low, the devices operate in byte (8-bit) mode. Under this mode, the DQ_{15}/A_{-1} pin becomes the lowest address bit and DQ_{14} to DQ_8 bits are tri-stated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ_7 to DQ_0 and the DQ_{15} to DQ_8 bits are ignored. Refer to "Timing Diagram for Word Mode Configuration", "$\overline{\text{BYTE}}$ Timing Diagram for Write Operations" and "Timing Diagram for Byte Mode Configuration" in "■TIMING DIAGRAM" for the timing diagram.

Data Protection

The MBM29DL400TC/BC are designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the devices automatically reset the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The devices also incorporate several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 2.3 V (typically 2.4 V) . If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 2.3 V.

If Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector (s) cannot be used.

Write Pulse "Glitch" Protection

Noise pulses of less than 3 ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$, or $\overline{\text{WE}}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{\text{OE}} = V_{IL}$, $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{WE}} = V_{IH}$. To initiate a write cycle $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be a logical zero while $\overline{\text{OE}}$ is a logical one.

Power-Up Write Inhibit

Power-up of the devices with $\overline{\text{WE}} = \overline{\text{CE}} = V_{IL}$ and $\overline{\text{OE}} = V_{IH}$ will not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically reset to the read mode on power-up.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	T_{stg}	−55	+125	°C
Ambient Temperature with Power Applied	T_A	−40	+85	°C
Voltage with Respect to Ground All pins except A9, $\overline{OE}$, and $\overline{RESET}$ *1	V_{IN}, V_{OUT}	−0.5	V_{CC} + 0.5	V
Power Supply Voltage *1	V_{CC}	−0.5	+4.0	V
A9, $\overline{OE}$, and $\overline{RESET}$ *2	V_{IN}	−0.5	+13.0	V

*1: Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

*2: Minimum DC input voltage on A9, $\overline{OE}$ and $\overline{RESET}$ pins is −0.5 V. During voltage transitions, A9, $\overline{OE}$ and $\overline{RESET}$ pins may undershoot V_{SS} to −2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN} - V_{CC}) does not exceed 9.0 V. Maximum DC input voltage on A9, $\overline{OE}$ and $\overline{RESET}$ pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Part No.	Value		Unit
			Min	Max	
Ambient Temperature	T_A	MBM29DL400TC/BC-55	−20	+70	°C
		MBM29DL400TC/BC-70/90	−40	+85	°C
Power Supply Voltage	V_{CC}	MBM29DL400TC/BC-55	+3.0	+3.6	V
		MBM29DL400TC/BC-70/90	+2.7	+3.6	V

Note : Operating ranges define those limits between which the proper device function is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ **MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT**

+0.6 V
−0.5 V
−2.0 V

20 ns 20 ns
20 ns
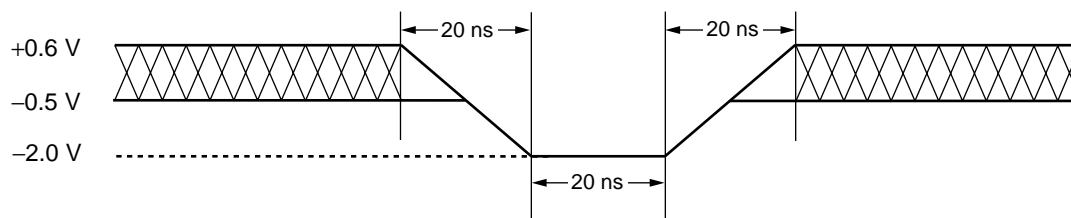
Maximum Undershoot Waveform

V_{CC} + 2.0 V
V_{CC} + 0.5 V
+2.0 V

20 ns
20 ns 20 ns

Maximum Overshoot Waveform 1

+14.0 V
+13.0 V
V_{CC} + 0.5 V

20 ns
20 ns 20 ns
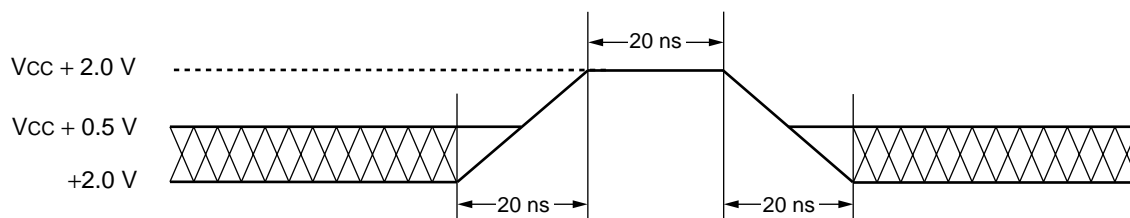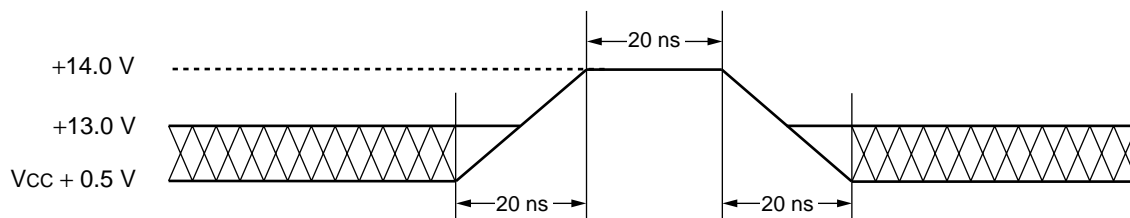
Note : This waveform is applied for A_9, $\overline{OE}$, and $\overline{RESET}$.

Maximum Overshoot Waveform 2

■ DC CHARACTERISTICS

Parameter	Symbol	Conditions		Value		Unit
				Min	Max	
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		−1.0	+1.0	μA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		−1.0	+1.0	μA
A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	I_{LIT}	$V_{CC} = V_{CC}$ Max A_9, $\overline{OE}$, $\overline{RESET} = 12.5$ V		—	+35	μA
V_{CC} Active Current *1	I_{CC1}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 10 MHz	Byte	—	18	mA
			Word		20	
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5 MHz	Byte	—	8	mA
			Word		10	
V_{CC} Active Current *2	I_{CC2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		—	35	mA
V_{CC} Current (Standby)	I_{CC3}	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V		—	5	μA
V_{CC} Current (Standby, Reset)	I_{CC4}	$V_{CC} = V_{CC}$ Max, $\overline{RESET} = V_{SS} \pm 0.3$ V		—	5	μA
V_{CC} Current (Automatic Sleep Mode) *3	I_{CC5}	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{SS} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V $V_{IN} = V_{CC} \pm 0.3$ V or $V_{SS} \pm 0.3$ V		—	5	μA
V_{CC} Active Current *5 (Read-While-Program)	I_{CC6}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	Byte	—	45	mA
			Word	—	45	
V_{CC} Active Current *5 (Read-While-Erase)	I_{CC7}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	Byte	—	45	mA
			Word	—	45	
V_{CC} Active Current (Erase-Suspend-Program)	I_{CC8}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		—	35	mA
Input Low Level	V_{IL}	—		−0.5	0.6	V
Input High Level	V_{IH}	—		2.0	$V_{CC} + 0.3$	V
Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$, $\overline{RESET}$) *4	V_{ID}	—		11.5	12.5	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 4.0$ mA, $V_{CC} = V_{CC}$ Min		—	0.45	V
Output High Voltage Level	V_{OH1}	$I_{OH} = -2.0$ mA, $V_{CC} = V_{CC}$ Min		2.4	—	V
	V_{OH2}	$I_{OH} = -100$ μA		$V_{CC} - 0.4$	—	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	—		2.3	2.5	V

*1: The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2: I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3: Automatic sleep mode enables the low power mode when address remain stable for 150 ns.

*4: Applicable for only V_{CC} applying.

*5: Embedded Algorithm (program or erase) is in progress. (@5 MHz)

■ AC CHARACTERISTICS

• Read Only Operations Characteristics

Parameter	Symbol		Test Setup	Value (Note)						Unit
				-55		-70		-90		
	JEDEC	Standard		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	—	55	—	70	—	90	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	55	—	70	—	90	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE} = V_{IL}$	—	55	—	70	—	90	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	30	—	30	—	35	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	25	—	25	—	30	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	25	—	25	—	30	ns
Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	0	—	0	—	0	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t_{READY}	—	—	20	—	20	—	20	μs
$\overline{CE}$ to $\overline{BYTE}$ Switching Low or High	—	t_{ELFL} t_{ELFH}	—	—	5	—	5	—	5	ns

Note : Test Conditions :
Output Load : 1 TTL gate and 30 pF (MBM29DL400TC/BC-55/-70)
        1 TTL gate and 100 pF (MBM29DL400TC/BC-90)
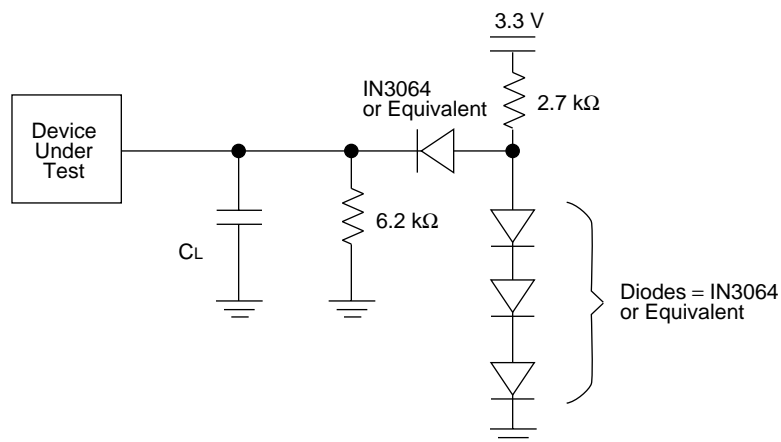Input rise and fall times : 5 ns
Input pulse levels : 0.0 V or 3.0 V
Timing measurement reference level
        Input : 1.5 V
        Output : 1.5 V

Note : C_L = 30 pF including jig capacitance (MBM29DL400TC/BC-55/-70)
        C_L = 100 pF including jig capacitance (MBM29DL400TC/BC-90)

Test Conditions

- **Write/Erase/Program Operations**

Parameter	Symbol		Value									Unit
			-55			-70			-90			
	JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	55	—	—	70	—	—	90	—	—	ns
Address Setup Time	t_{AVWL}	t_{AS}	0	—	—	0	—	—	0	—	—	ns
Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling	—	t_{ASO}	15	—	—	15	—	—	15	—	—	ns
Address Hold Time	t_{WLAX}	t_{AH}	45	—	—	45	—	—	45	—	—	ns
Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling	—	t_{AHT}	0	—	—	0	—	—	0	—	—	ns
Data Setup Time	t_{DVWH}	t_{DS}	30	—	—	35	—	—	45	—	—	ns
Data Hold Time	t_{WHDX}	t_{DH}	0	—	—	0	—	—	0	—	—	ns
Output Enable Hold Time — Read	—	t_{OEH}	0	—	—	0	—	—	0	—	—	ns
Output Enable Hold Time — Toggle and $\overline{Data}$ Polling			10	—	—	10	—	—	10	—	—	ns
$\overline{CE}$ High During Toggle Bit Polling	—	t_{CEPH}	20	—	—	20	—	—	20	—	—	ns
$\overline{OE}$ High During Toggle Bit Polling	—	t_{OEPH}	20	—	—	20	—	—	20	—	—	ns
Read Recover Time Before Write	t_{GHWL}	t_{GHWL}	0	—	—	0	—	—	0	—	—	ns
Read Recover Time Before Write	t_{GHEL}	t_{GHEL}	0	—	—	0	—	—	0	—	—	ns
$\overline{CE}$ Setup Time	t_{ELWL}	t_{CS}	0	—	—	0	—	—	0	—	—	ns
$\overline{WE}$ Setup Time	t_{WLEL}	t_{WS}	0	—	—	0	—	—	0	—	—	ns
$\overline{CE}$ Hold Time	t_{WHEH}	t_{CH}	0	—	—	0	—	—	0	—	—	ns
$\overline{WE}$ Hold Time	t_{EHWH}	t_{WH}	0	—	—	0	—	—	0	—	—	ns
Write Pulse Width	t_{WLWH}	t_{WP}	30	—	—	35	—	—	45	—	—	ns
$\overline{CE}$ Pulse Width	t_{ELEH}	t_{CP}	30	—	—	35	—	—	45	—	—	ns
Write Pulse Width High	t_{WHWL}	t_{WPH}	25	—	—	25	—	—	25	—	—	ns
$\overline{CE}$ Pulse Width High	t_{EHEL}	t_{CPH}	25	—	—	25	—	—	25	—	—	ns
Byte Programming Operation	t_{WHWH1}	t_{WHWH1}	—	8	—	—	8	—	—	8	—	µs
Sector Erase Operation *1	t_{WHWH2}	t_{WHWH2}	—	1	—	—	1	—	—	1	—	s
V_{CC} Setup Time	—	t_{VCS}	50	—	—	50	—	—	50	—	—	µs
Rise Time to V_{ID} *2	—	t_{VIDR}	500	—	—	500	—	—	500	—	—	ns
Voltage Transition Time *2	—	t_{VLHT}	4	—	—	4	—	—	4	—	—	µs
Write Pulse Width *2	—	t_{WPP}	100	—	—	100	—	—	100	—	—	µs
$\overline{OE}$ Setup Time to $\overline{WE}$ Active *2	—	t_{OESP}	4	—	—	4	—	—	4	—	—	µs
$\overline{CE}$ Setup Time to $\overline{WE}$ Active *2	—	t_{CSP}	4	—	—	4	—	—	4	—	—	µs
Recover Time From RY/$\overline{BY}$	—	t_{RB}	0	—	—	0	—	—	0	—	—	ns
$\overline{RESET}$ Pulse Width	—	t_{RP}	500	—	—	500	—	—	500	—	—	ns
$\overline{RESET}$ Hold Time Before Read	—	t_{RH}	200	—	—	200	—	—	200	—	—	ns

(Continued)

(Continued)

Parameter	Symbol		Value									Unit
			-55			-70			-90			
	JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$\overline{BYTE}$ Switching Low to Output High-Z	—	t_{FLQZ}	—	—	30	—	—	30	—	—	35	ns
$\overline{BYTE}$ Switching High to Output Active	—	t_{FHQV}	30	—	—	30	—	—	35	—	—	ns
Program/Erase Valid to RY/$\overline{BY}$ Delay	—	t_{BUSY}	—	—	90	—	—	90	—	—	90	ns
Delay Time from Embedded Output Enable	—	t_{EOE}	—	—	30	—	—	30	—	—	35	ns

*1: This does not include the preprogramming time.

*2: This timing is for Sector Protection operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limit			Unit	Remarks
	Min	**Typ**	**Max**		
Sector Erase Time	—	1	10	s	Excludes programming time prior to erasure
Word Programming Time	—	16	360	μs	Excludes system-level overhead
Byte Programming Time	—	8	300	μs	
Chip Programming Time	—	4.2	12.5	s	Excludes system-level overhead
Program/Erase Cycle	100,000	—	—	cycle	—

■ INPUT/OUTPUT PIN CAPACITANCE

1. TSOP (I) PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	**Max**	
Input Capacitance	C_{IN}	$V_{IN} = 0$	6.0	7.5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	8.5	12.0	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	8.0	10.0	pF

Notes : • Test conditions $T_A = 25\ °C$, f = 1.0 MHz
 • DQ_{15}/A_{-1} pin capacitance is stipulated by output capacitance.

2. FBGA PIN CAPACITANCE
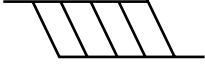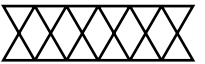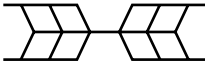
Parameter	Symbol	Test Setup	Value		Unit
			Typ	**Max**	
Input Capacitance	C_{IN}	$V_{IN} = 0$	6.0	7.5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	8.5	12.0	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	8.0	10.0	pF

Notes : • Test conditions $T_A = 25\ °C$, f = 1.0 MHz
 • DQ_{15}/A_{-1} pin capacitance is stipulated by output capacitance.

■ TIMING DIAGRAM

• **Key to Switching Waveforms**

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Change from H to L
	May Change from L to H	Will Change from L to H
	"H" or "L": Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State
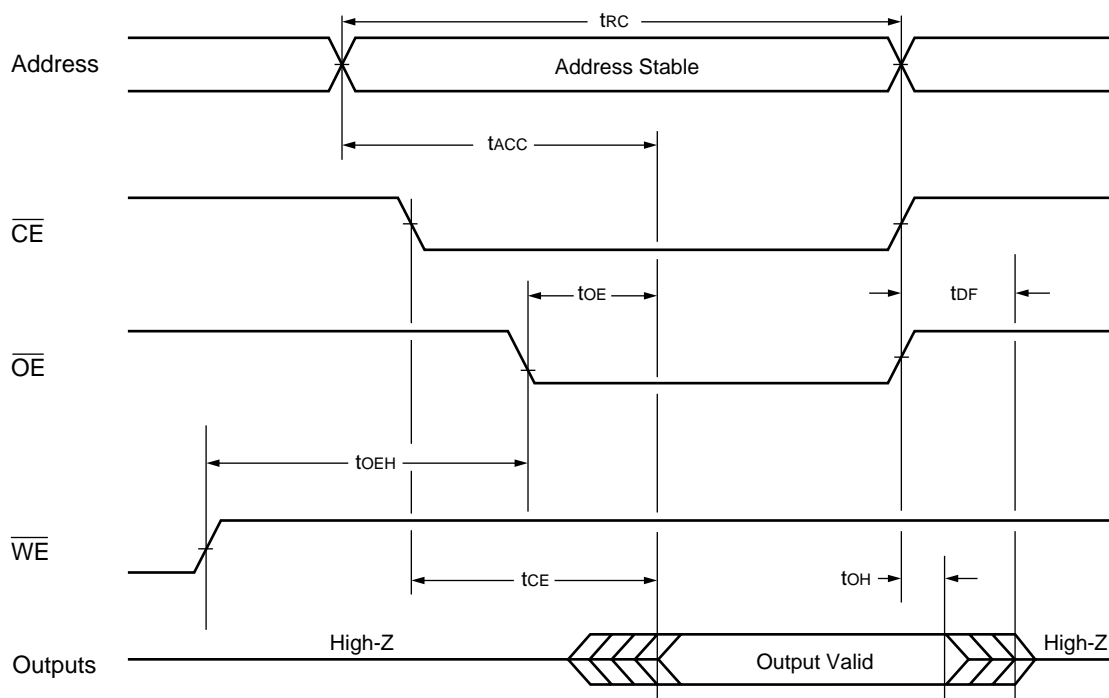
Read Operation Timing Diagram
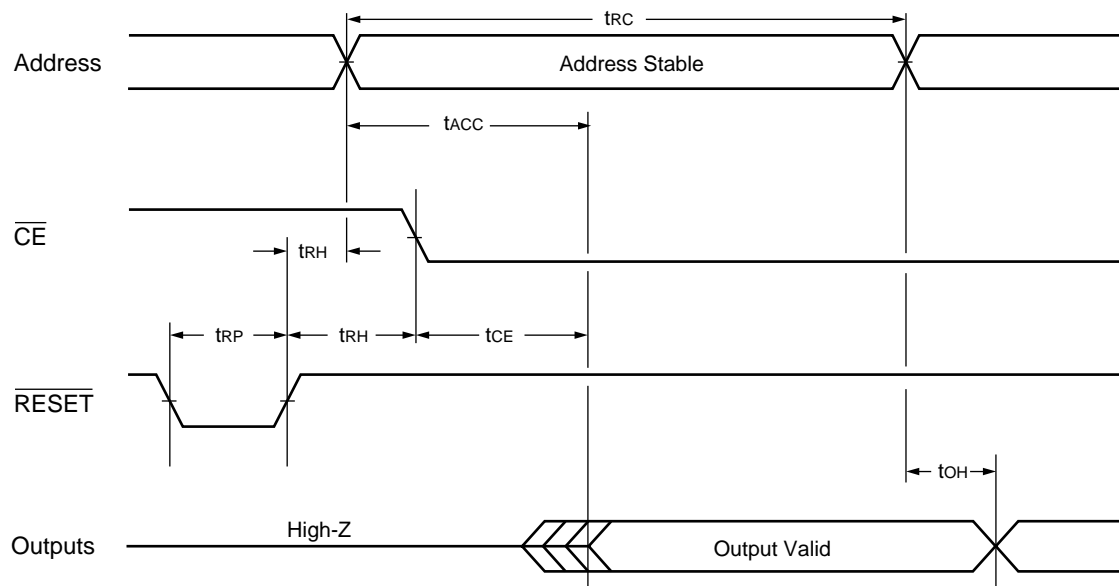
Hardware Reset/Read Operation Timing Diagram
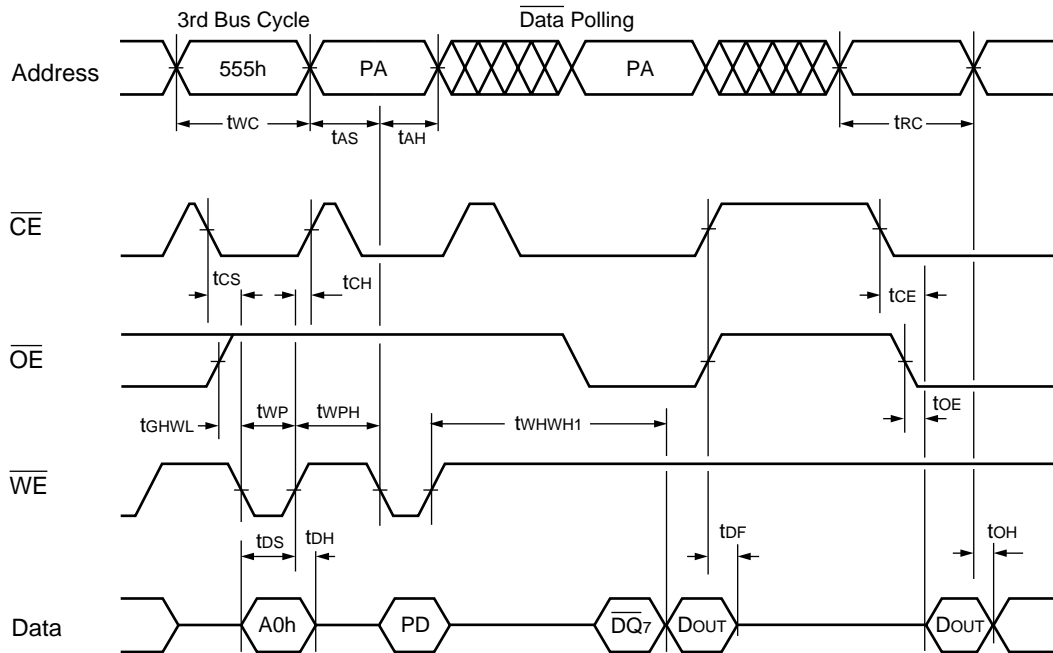
Notes : • PA is address of the memory location to be programmed.
- PD is data to be programmed at word address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram
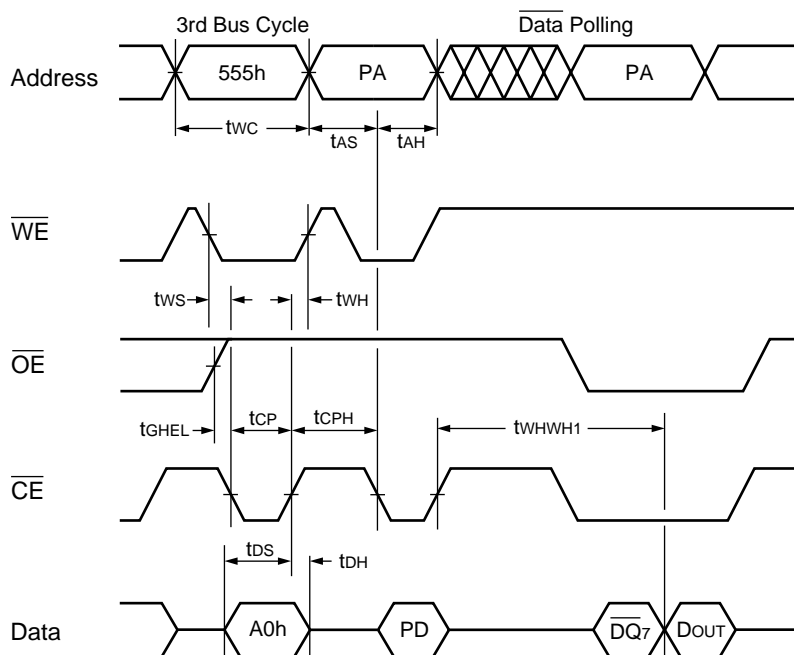
Notes : • PA is address of the memory location to be programmed.
  • PD is data to be programmed at word address.
  • $\overline{DQ_7}$ is the output of the complement of the data written to the device.
  • D$_{OUT}$ is the output of the data written to the device.
  • Figure indicates last two bus cycles out of four bus cycle sequence.
  • These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

Alternate $\overline{CE}$ Controlled Program Operation Timing Diagram
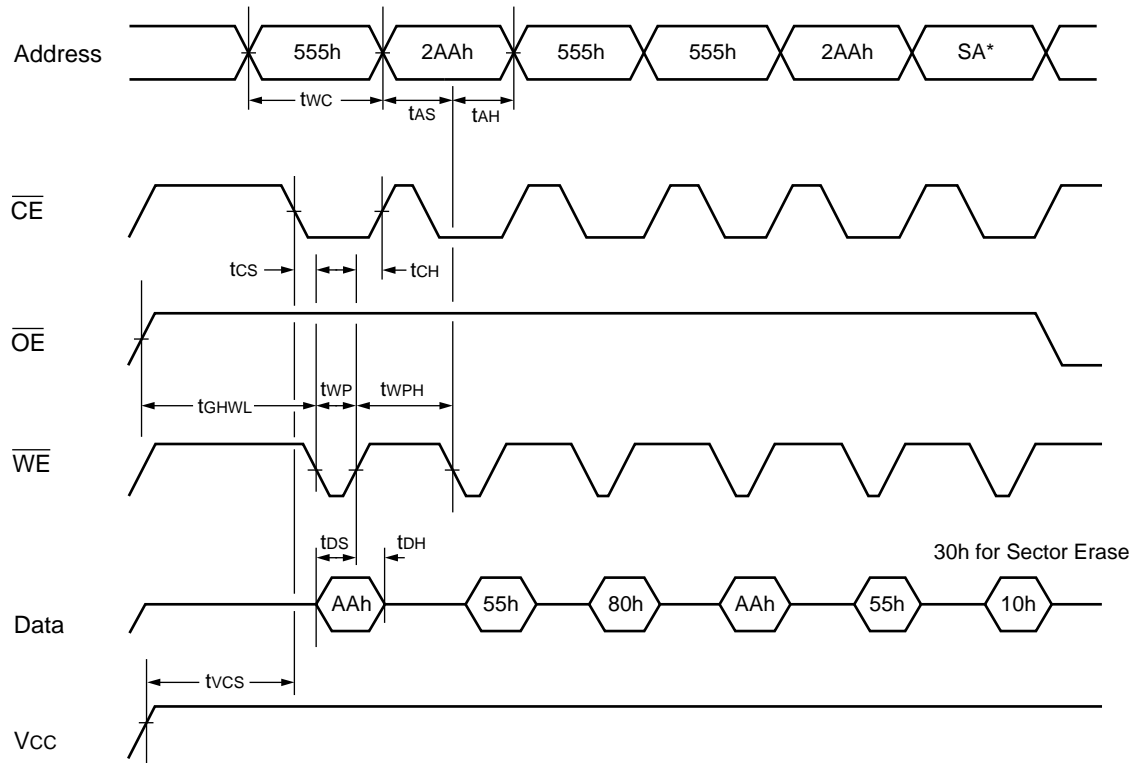
* : SA is the sector address for Sector Erase. Address = 555h (Word) for Chip Erase.

Note : These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

Chip/Sector Erase Operation Timing Diagram
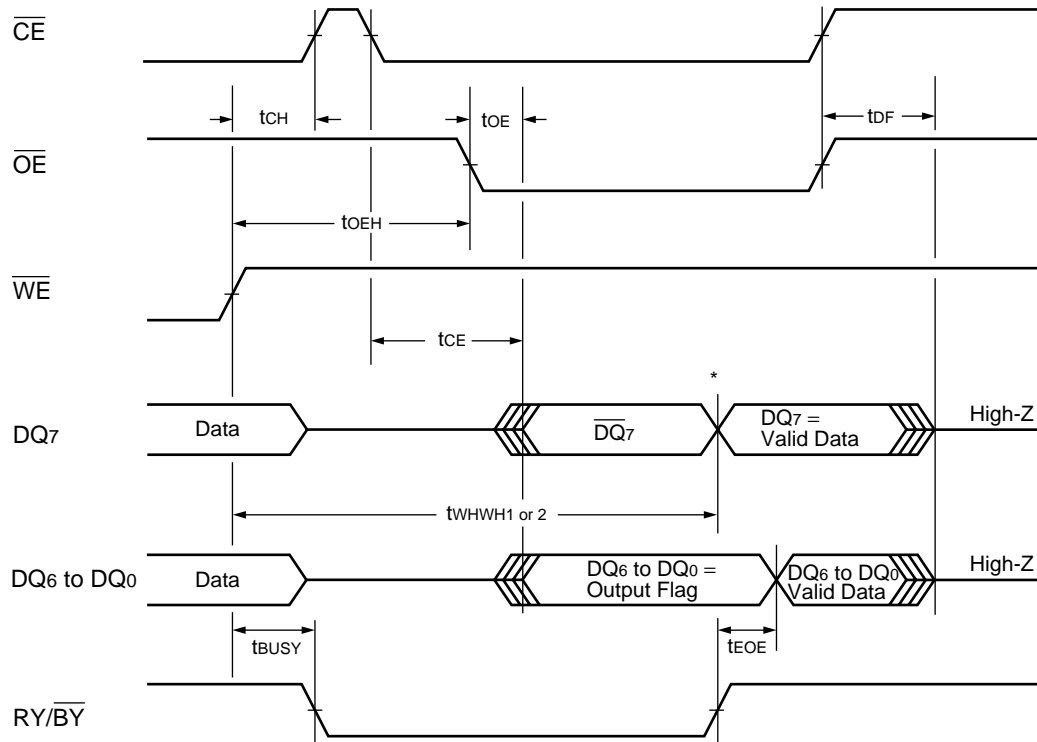
* : DQ7 = Valid Data (The device has completed the Embedded operation) .

$\overline{\text{Data}}$ **Polling during Embedded Algorithm Operation Timing Diagram**
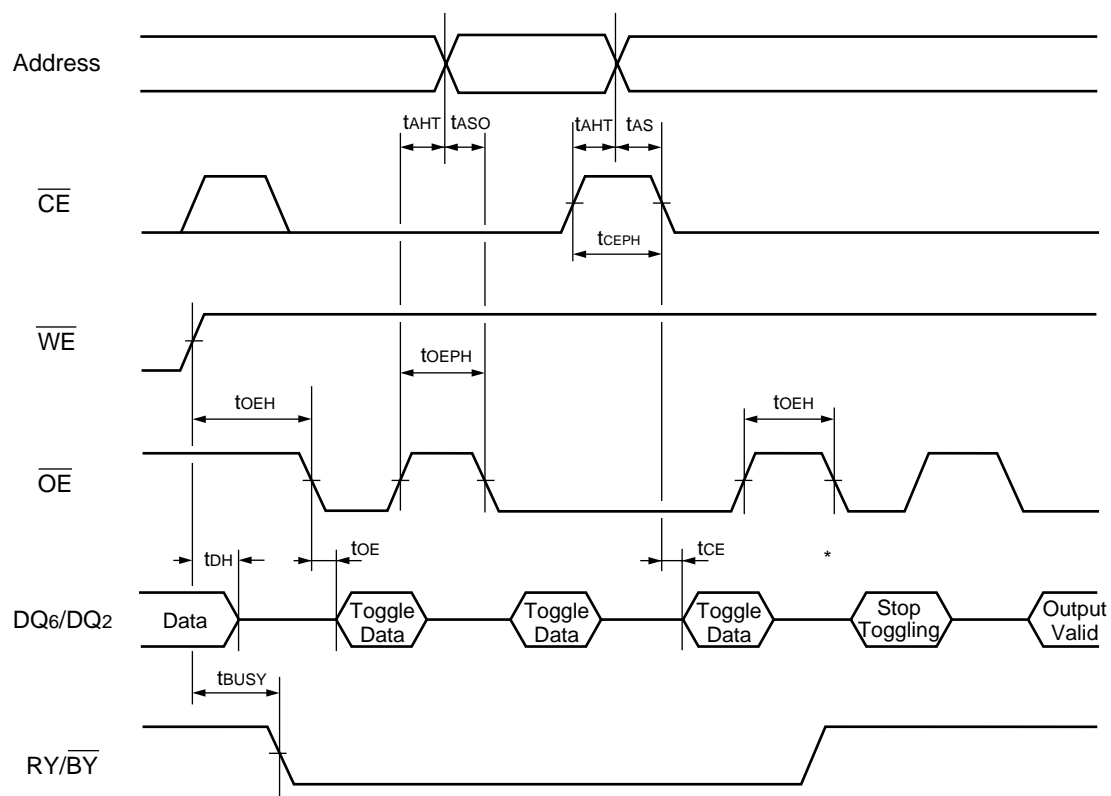
* : DQ$_6$ stops toggling (The device has completed the Embedded operation) .

AC Waveforms for Toggle Bit I during Embedded Algorithm Operations

Read | Command | Read | Command | Read | Read

Address: BA1 | BA2 (555h) | BA1 | BA2 (PA) | BA1 | BA2 (PA)

$\overline{CE}$

$\overline{OE}$

$\overline{WE}$

DQ: Valid Output | Valid Intput (A0h) | Valid Output | Valid Intput (PD) | Valid Output | Status
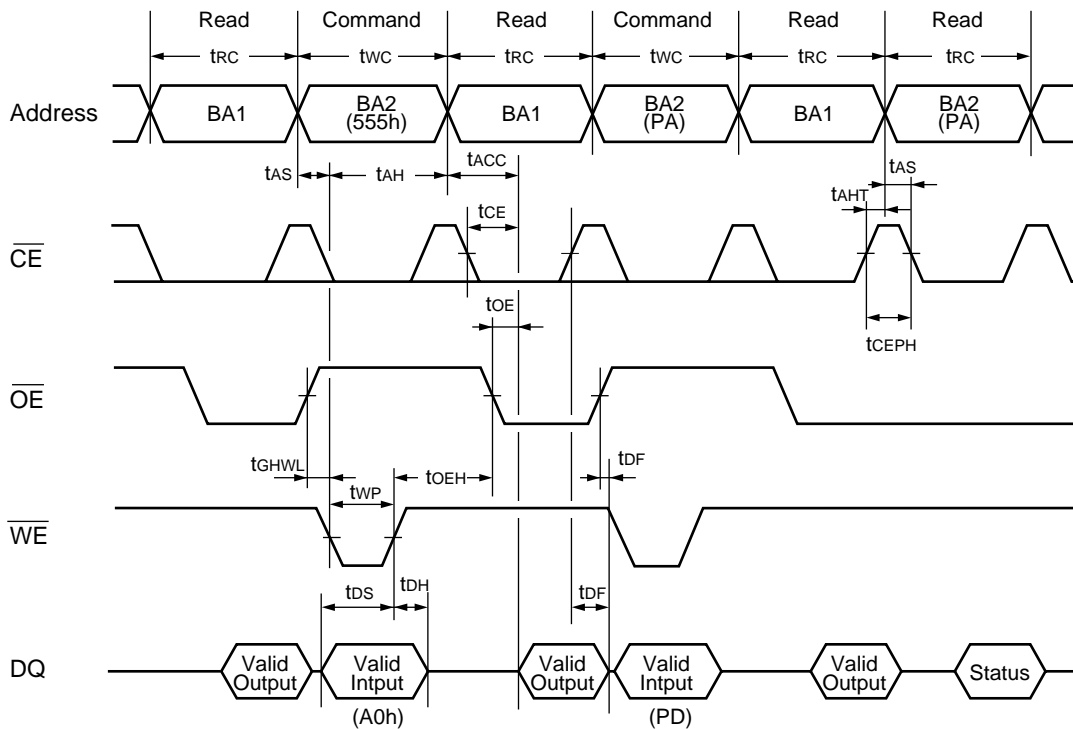
Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1 : Address Corresponding to Bank 1.
BA2 : Address Corresponding to Bank 2.

Bank-to-Bank Read/Write Timing Diagram

Enter Embedded Erasing | Erase Suspend | Enter Erase Suspend Program | Erase Resume

$\overline{WE}$: Erase | Erase Suspend Read | Erase Suspend Program | Erase Suspend Read | Erase | Erase Complete

DQ6

DQ2

Toggle DQ2 and DQ6 with $\overline{OE}$ or $\overline{CE}$
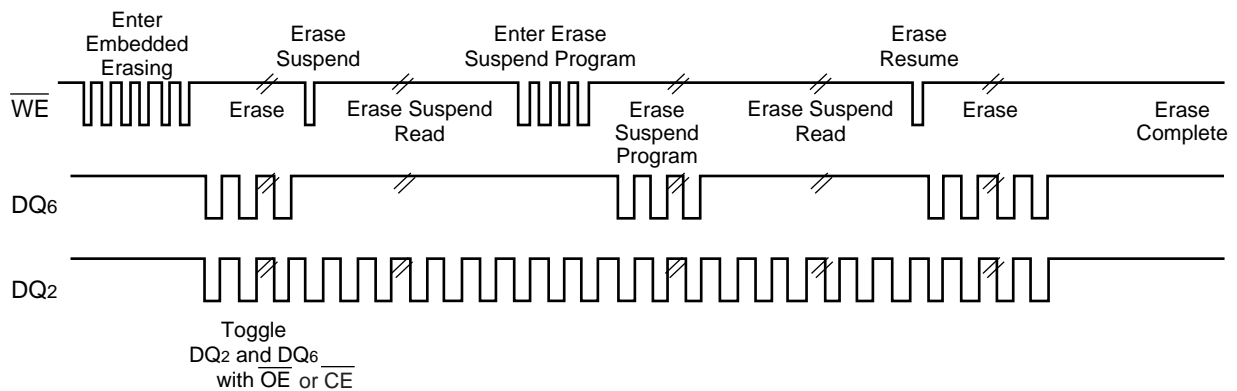
Note : DQ2 is read from the erase-suspended sector.

DQ2 vs. DQ6
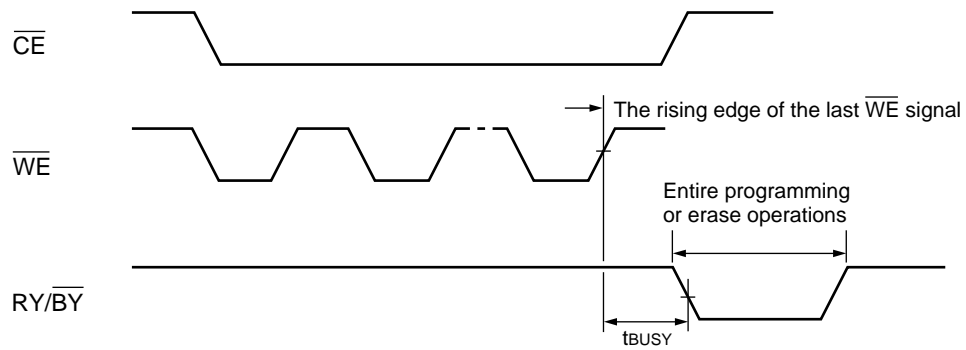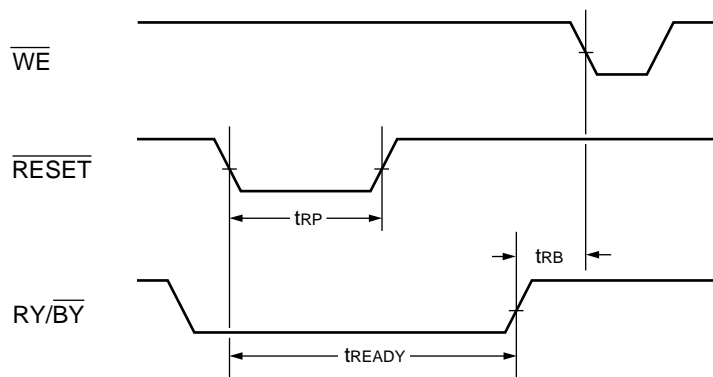
CE

WE

The rising edge of the last WE signal

Entire programming
or erase operations

RY/BY

tBUSY

RY/BY Timing Diagram during Program/Erase Operation Timing Diagram

WE

RESET

tRP

tRB

RY/BY

tREADY

RESET, RY/BY Timing Diagram

CE

BYTE

DQ14 to DQ0

t_{CE}

t_{ELFH}

t_{FHQV}

Data Output
(DQ7 to DQ0)

Data Output
(DQ14 to DQ0)

DQ15/A-1

A-1

DQ15

Timing Diagram for Word Mode Configuration

CE or WE

Falling edge of last write signal

BYTE

Input
Valid

t_{AS}

t_{AH}

BYTE Timing Diagram for Write Operations

CE

BYTE

DQ14 to DQ0

t_{ELFL}

Data Output
(DQ14 to DQ0)

Data Output
(DQ7 to DQ0)

t_{ACC}

DQ15/A-1

DQ15

A-1

t_{FLQZ}

Timing Diagram for Byte Mode Configuration

41
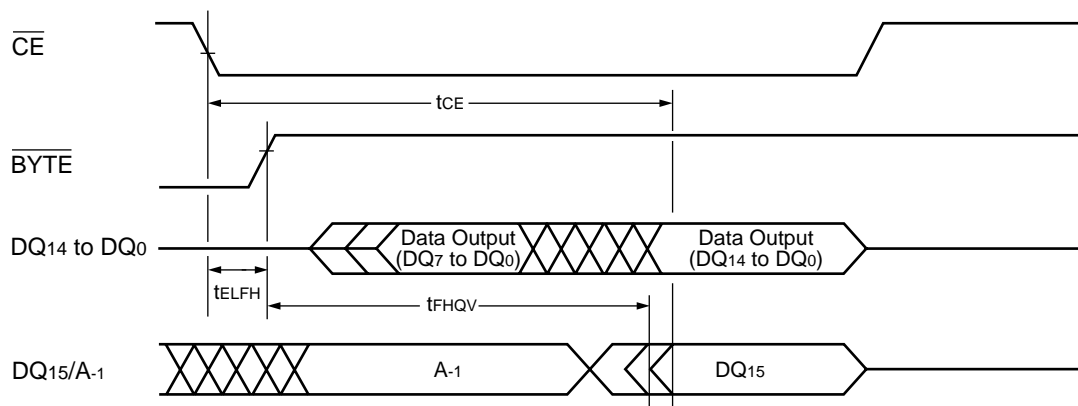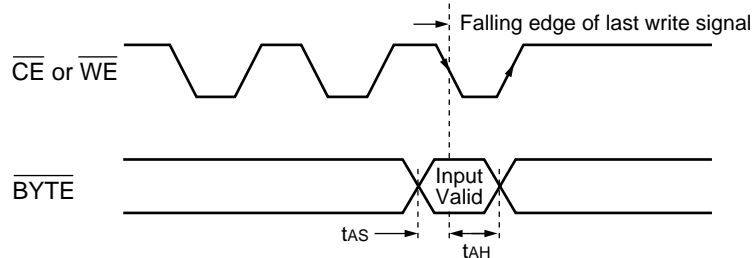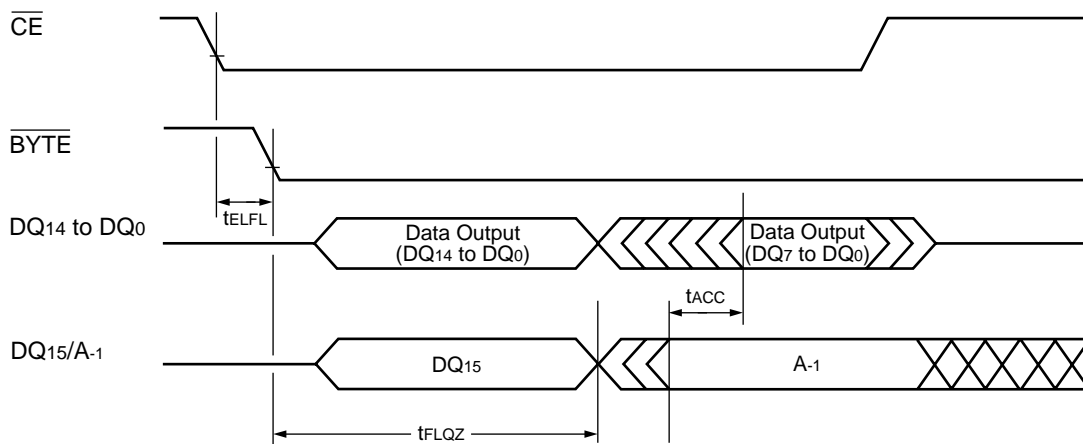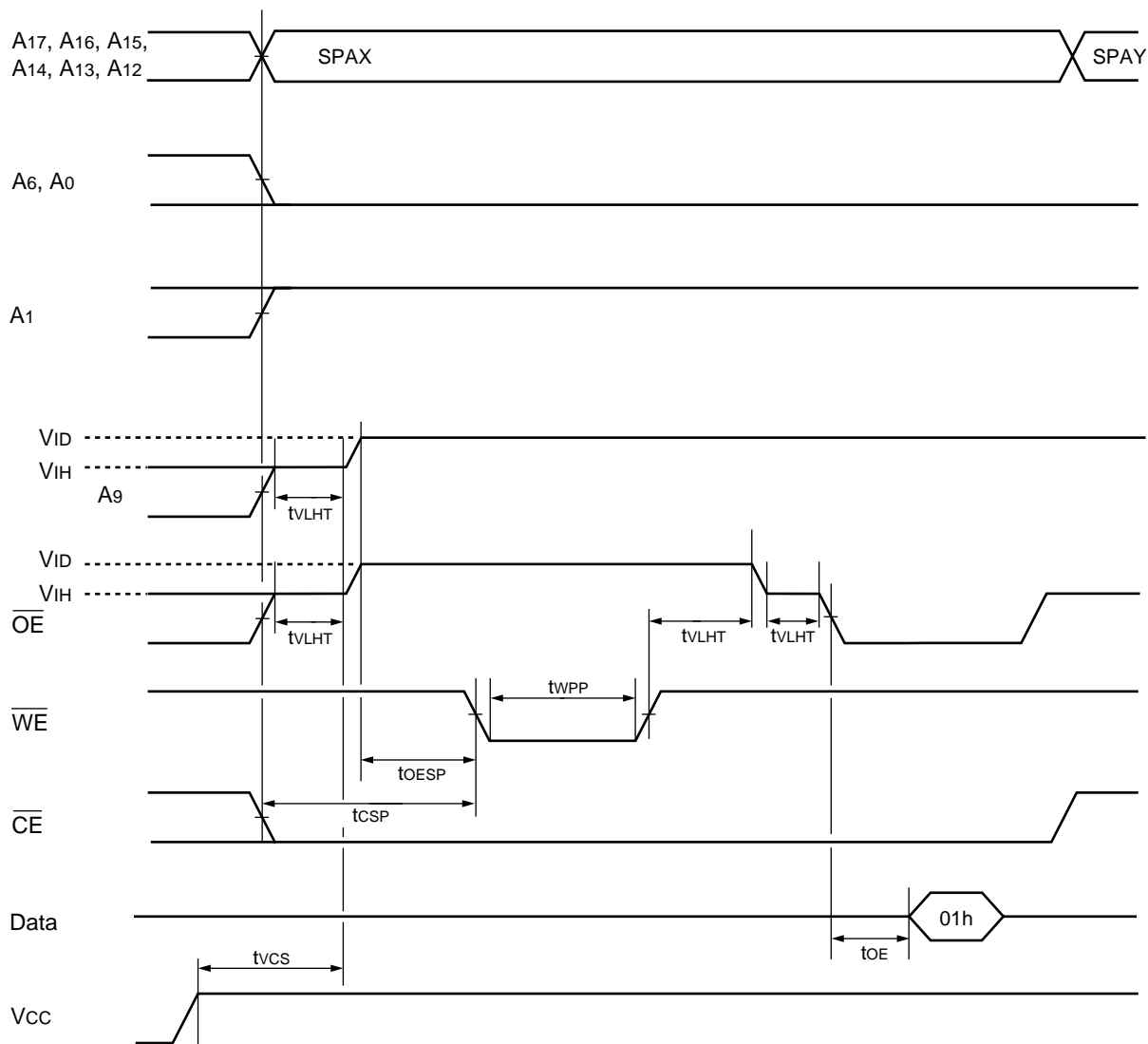
SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected

Note : A-1 is VIL on byte mode.
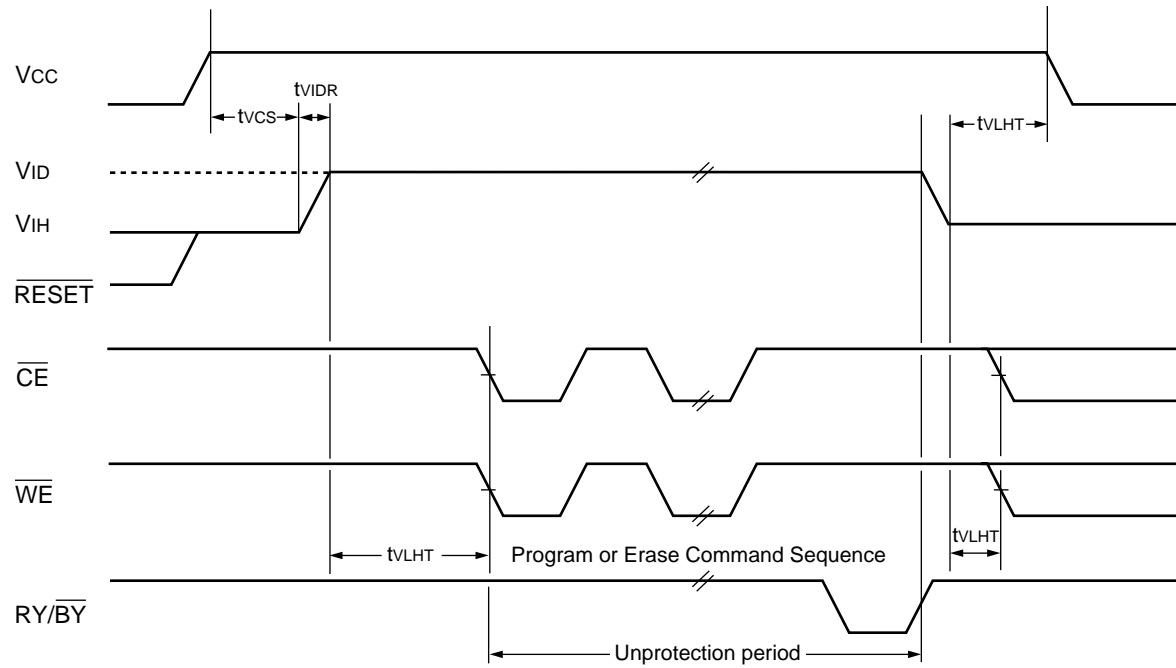
Sector Protection Timing Diagram

Temporary Sector Unprotection Timing Diagram

VCC

tVCS

RESET

tVLHT

tVIDR   tWC   tWC

Address   SPAX   SPAX   SPAY

A6, A0

A1

CE

OE   TIME-OUT

tWP

WE

Data   60h   60h   40h   01h   60h

tOE
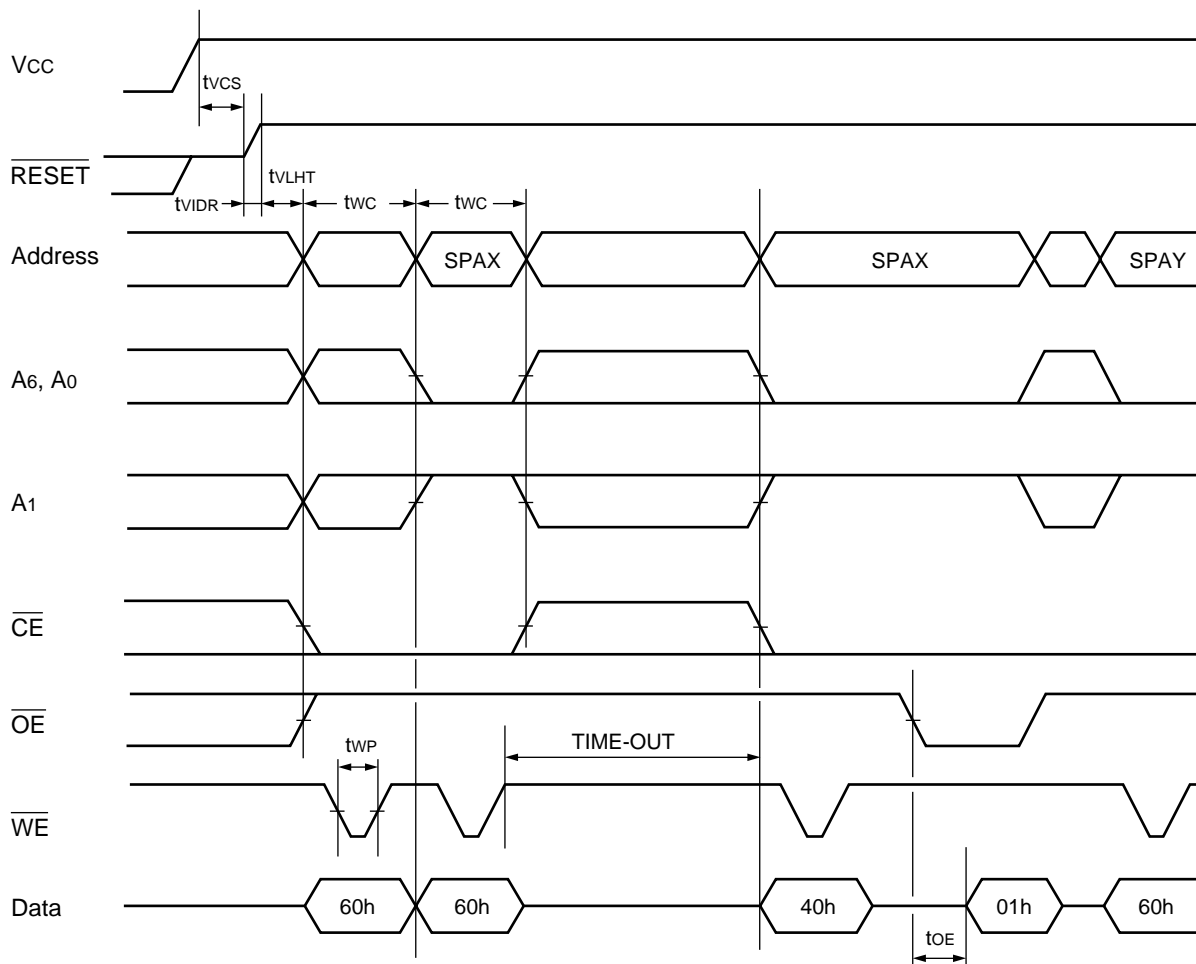
SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected
TIME-OUT : Time-Out window = 150 μs (Min)

Extended Sector Protection Timing Diagram

■ FLOW CHART

EMBEDDED ALGORITHM
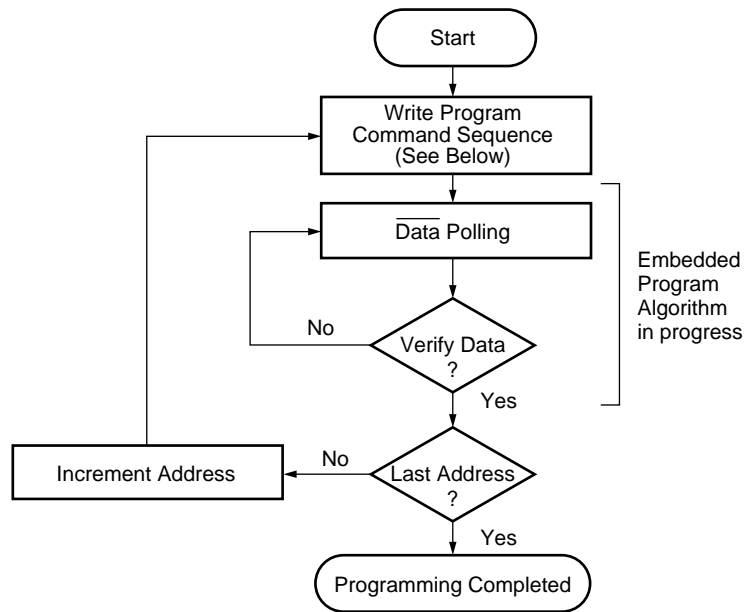
Start

Write Program
Command Sequence
(See Below)

Data Polling

Verify Data
?
No → (back to Data Polling)
Yes

Embedded
Program
Algorithm
in progress

Last Address
?
No → Increment Address → (back to Write Program Command Sequence)
Yes

Programming Completed

Program Command Sequence (Address/Command):

555h/AAh

2AAh/55h

555h/A0h

Program Address/Program Data
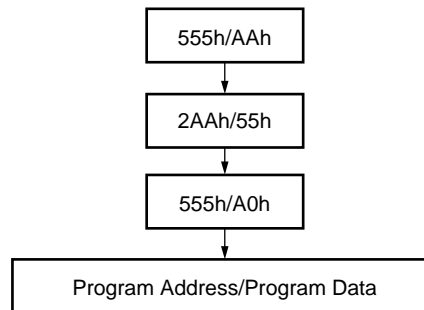
Note : The sequence is applied for ×16 mode.
The addresses differ from ×8 mode.

Embedded Program™ Algorithm

EMBEDDED ALGORITHM

```
                            ┌─────────────┐
                            │    Start    │
                            └──────┬──────┘
                                   │
                         ┌─────────▼─────────┐
                         │   Write Erase     │
                         │ Command Sequence  │
                         │   (See Below)     │
                         └─────────┬─────────┘
                                   │
                         ┌─────────▼─────────┐          ┐
                  ┌─────►│   Data Polling    │          │
                  │      └─────────┬─────────┘          │
                  │                │                    │  Embedded
                  │            ╱───▼───╲                │  Erase
              No  │          ╱ Data = FFh ╲             │  Algorithm
                  └─────────┤      ?       │            │  in progress
                             ╲           ╱              │
                              ╲────┬────╱  Yes          │
                                   │                    ┘
                         ┌─────────▼─────────┐
                         │ Erasure Completed │
                         └───────────────────┘
```

Chip Erase Command Sequence (Address/Command):

```
        ┌─────────────┐
        │  555h/AAh   │
        └──────┬──────┘
        ┌──────▼──────┐
        │  2AAh/55h   │
        └──────┬──────┘
        ┌──────▼──────┐
        │  555h/80h   │
        └──────┬──────┘
        ┌──────▼──────┐
        │  555h/AAh   │
        └──────┬──────┘
        ┌──────▼──────┐
        │  2AAh/55h   │
        └──────┬──────┘
        ┌──────▼──────┐
        │  555h/10h   │
        └─────────────┘
```
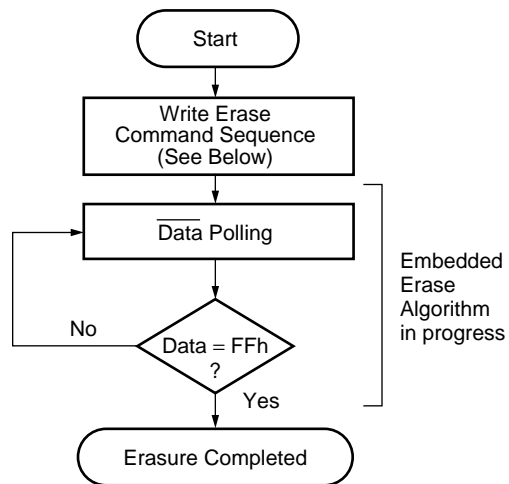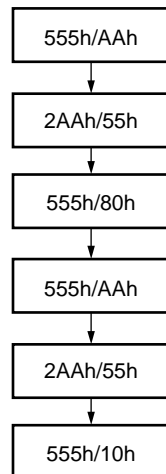
Individual Sector/Multiple Sector Erase Command Sequence (Address/Command):

```
        ┌─────────────┐
        │  555h/AAh   │
        └──────┬──────┘
        ┌──────▼──────┐
        │  2AAh/55h   │
        └──────┬──────┘
        ┌──────▼──────┐
        │  555h/80h   │
        └──────┬──────┘
        ┌──────▼──────┐
        │  555h/AAh   │
        └──────┬──────┘
        ┌──────▼──────┐
        │  2AAh/55h   │
        └──────┬──────┘
        ┌──────▼──────┐
        │Sector Address│
        │    /30h     │
        └──────┬──────┘
        ┌──────▼──────┐
        │Sector Address│        ┐
        │    /30h     │        │  Additional sector
        └──────┬──────┘        ├  erase commands
        ┌──────▼──────┐        │  are optional.
        │Sector Address│        ┘
        │    /30h     │
        └─────────────┘
```
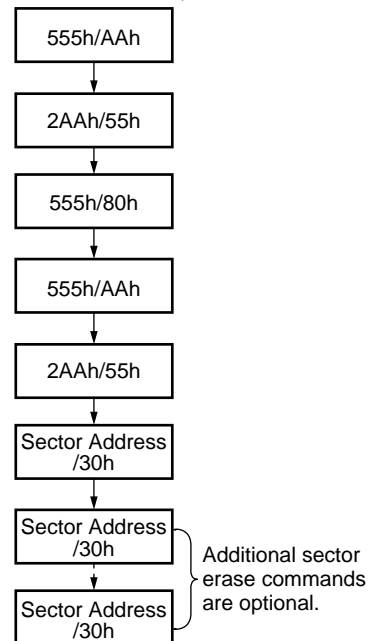
Note : The sequence is applied for ×16 mode.
The addresses differ from ×8 mode.

Embedded Erase™ Algorithm
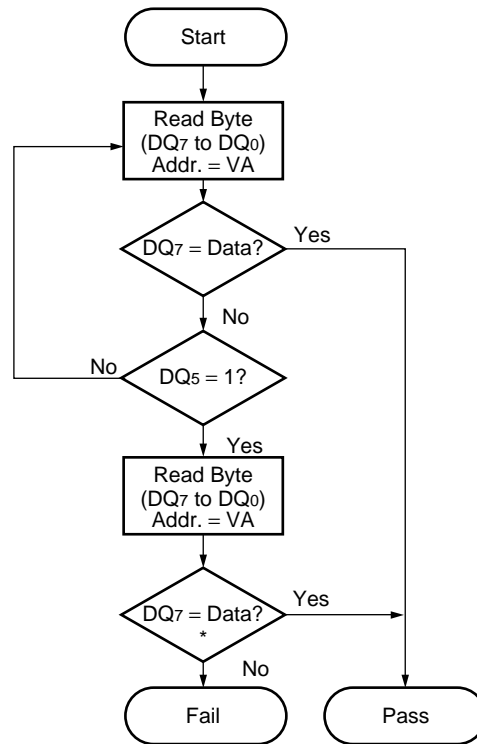
VA = Address for programming
  = Any of the sector addresses within the sector being erased during sector erase or multiple erases operation.
  = Any of the sector addresses within the sector not being protected during sector erase or multiple sector erases operation.

Start

Read Byte
(DQ7 to DQ0)
Addr. = VA

DQ7 = Data? — Yes

No

DQ5 = 1? — No

Yes

Read Byte
(DQ7 to DQ0)
Addr. = VA

DQ7 = Data?
* — Yes

No

Fail   Pass

* : DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

Data Polling Algorithm

Start

Read DQ7 to DQ0
Addr. = VA
*1

Read DQ7 to DQ0
Addr. = VA
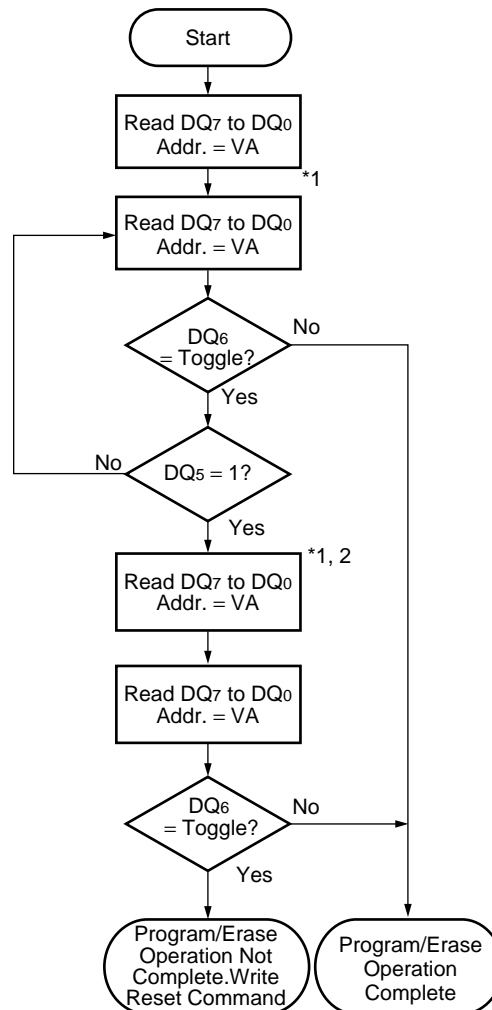
VA = Bank address being executed
Embedded Algorithm.

DQ6
= Toggle?   No

Yes

No   DQ5 = 1?

Yes

Read DQ7 to DQ0
Addr. = VA   *1, 2

Read DQ7 to DQ0
Addr. = VA

DQ6
= Toggle?   No

Yes

Program/Erase
Operation Not
Complete.Write
Reset Command

Program/Erase
Operation
Complete

*1 : Read toggle bit twice to determine whether it is toggling.

*2 : Recheck toggle bit because it may stop toggling as DQ5 changes to "1".

Toggle Bit Algorithm

48

Start

Setup Sector Addr.
(A17, A16, A15, A14, A13, A12)

PLSCNT = 1

$\overline{OE}$ = VID, A9 = VID
$\overline{CE}$ = VIL, $\overline{RESET}$ = VIH
A6 = A0 = VIL, A1 = VIH

Activate $\overline{WE}$ Pulse

Time out 100 μs

$\overline{WE}$ = VIH, $\overline{CE}$ = $\overline{OE}$ = VIL
(A9 should remain VID)

Read from Sector
(Addr. = SPA, A1 = VIH) *
A6 = A0 = VIL

Increment PLSCNT

PLSCNT = 25?

No

Data = 01h?

No

Yes

Yes

Protect Another Sector?

Yes

No

Remove VID from A9
Write Reset Command

Device Failed

Remove VID from A9
Write Reset Command

Sector Protection
Completed

* : A-1 is VIL on byte mode.

Sector Protection Algorithm

49

Start

$\overline{RESET} = V_{ID}$
*1

Perform Erase or
Program Operations

$\overline{RESET} = V_{IH}$

Temporary Sector
Unprotection Completed
*2

*1 : All protected sectors are unprotected.

*2 : All previously protected sectors are protected once again.

Temporary Sector Unprotection Algorithm

```
                              ┌──────────────┐
                              │    Start     │
                              └──────┬───────┘
                              ┌──────┴───────┐
                              │ RESET = VID  │
                              └──────┬───────┘
                              ┌──────┴───────┐
                              │ Wait to 4 µs │
                              └──────┬───────┘
┌──────────────────┐      No   ◇ Extended Sector ◇
│ Device is Operating in │◄────── ◇ Protection Entry? ◇
│ Temporary Sector       │        └──────┬───────┘
│ Unprotection Mode      │           Yes │
└──────────────────┘      ┌──────────────┴────────────┐
                          │ To Setup Sector Protection │
                          │     Write XXXh/60h         │
                          └──────────────┬────────────┘
                          ┌──────────────┴────────────┐
                          │       PLSCNT = 1           │◄────────────┐
                          └──────────────┬────────────┘             │
                          ┌──────────────┴────────────┐             │
                          │      To Protect Sector     │             │
                          │ Write 60h to Sector Address│             │
                          │  (A6 = A0 = VIL, A1 = VIH) │             │
                          └──────────────┬────────────┘             │
                          ┌──────────────┴────────────┐             │
                          │      Time out 150 µs       │             │
                          └──────────────┬────────────┘             │
                          ┌──────────────┴────────────┐             │
                          │ To Verify Sector Protection│             │
                          │ Write 40h to Sector Address│             │
                          │  (A6 = A0 = VIL, A1 = VIH) │             │
                          └──────────────┬────────────┘             │
                          ┌──────────────┴────────────┐             │
                          │   Read from Sector Address │  ┌──────────────────────┐
                          │ (A0 = VIL, A1 = VIH, A6 = VIL)│ Setup Next Sector Address│
                          └──────────────┬────────────┘  └──────────────────────┘
        ◇ PLSCNT = 25? ◇ ◄──No── ◇    Data = 01h?    ◇ ──Yes──┐
              │                          │ Yes                  │
          Yes │              ◇ Protect Other Sector? ◇ ──Yes───┘
┌─────────────────────┐          │ No
│ Remove VID from RESET│  ┌─────────────────────┐
│ Write Reset Command  │  │ Remove VID from RESET│
└─────────┬───────────┘  │ Write Reset Command  │
┌─────────┴───────────┐  └─────────┬───────────┘
│   Device Failed     │  ┌─────────┴───────────┐
└─────────────────────┘  │  Sector Protection  │
                         │     Completed       │
                         └─────────────────────┘
```
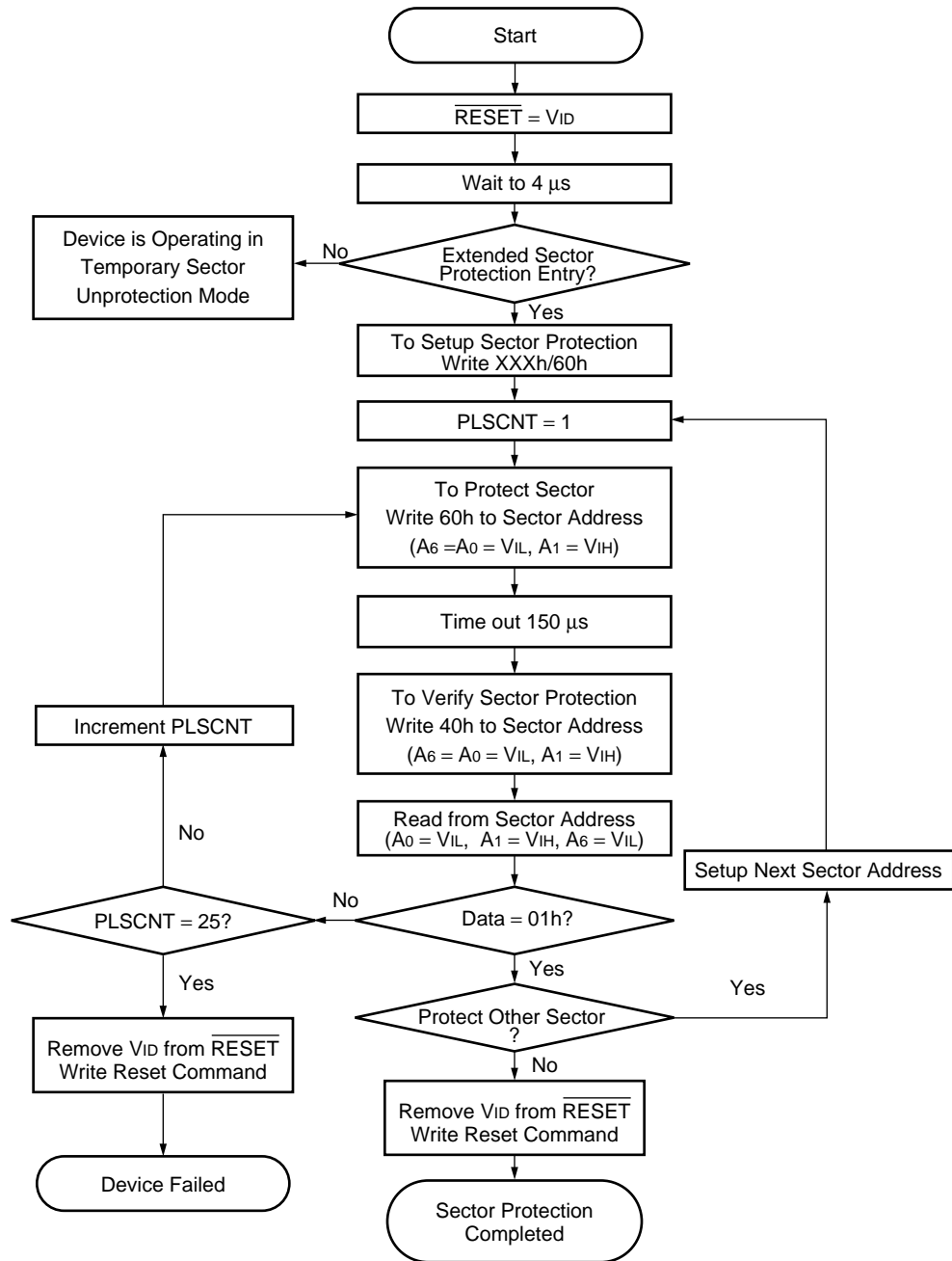
Extended Sector Protection Algorithm

FAST MODE ALGORITHM

```
                           ┌─────────┐
                           │  Start  │
                           └────┬────┘
                                │
                        ┌───────▼───────┐            ┐
                        │   555h/AAh    │            │
                        └───────┬───────┘            │
                                │                    │
                        ┌───────▼───────┐            │
                        │   2AAh/55h    │            ├── Set Fast Mode
                        └───────┬───────┘            │
                                │                    │
                        ┌───────▼───────┐            │
                        │   555h/20h    │            ┘
                        └───────┬───────┘
                                │
                        ┌───────▼───────┐            ┐
         ┌─────────────►│   XXXh/A0h    │            │
         │              └───────┬───────┘            │
         │                      │                    │
         │      ┌───────────────▼───────────────┐    │
         │      │  Program Address/Program Data  │    │
         │      └───────────────┬───────────────┘    │
         │                      │                    │
         │              ┌───────▼───────┐            ├── In Fast Program
         │              │  Data Polling │◄──┐        │
         │              └───────┬───────┘   │        │
         │                      │           │        │
         │                 ◄────▼────►  No   │        │
         │                 │Verify Data?├────┘        │
         │                 ◄────┬────►             │
         │                      │ Yes                │
         │                 ◄────▼────►                │
  ┌──────┴────────┐   No   │Last Address?│            │
  │Increment Addr │◄───────◄─────┬──────►            │
  └───────────────┘              │ Yes               │
                        ┌────────▼─────────┐         │
                        │Programming Completed│       ┘
                        └────────┬─────────┘
                                 │
                        ┌────────▼─────────┐          ┐
                        │  (BA)XXXh/90h    │          │
                        └────────┬─────────┘          ├── Reset Fast Mode
                                 │                    │
                        ┌────────▼─────────┐          │
                        │    XXXh/F0h      │          ┘
                        └──────────────────┘
```
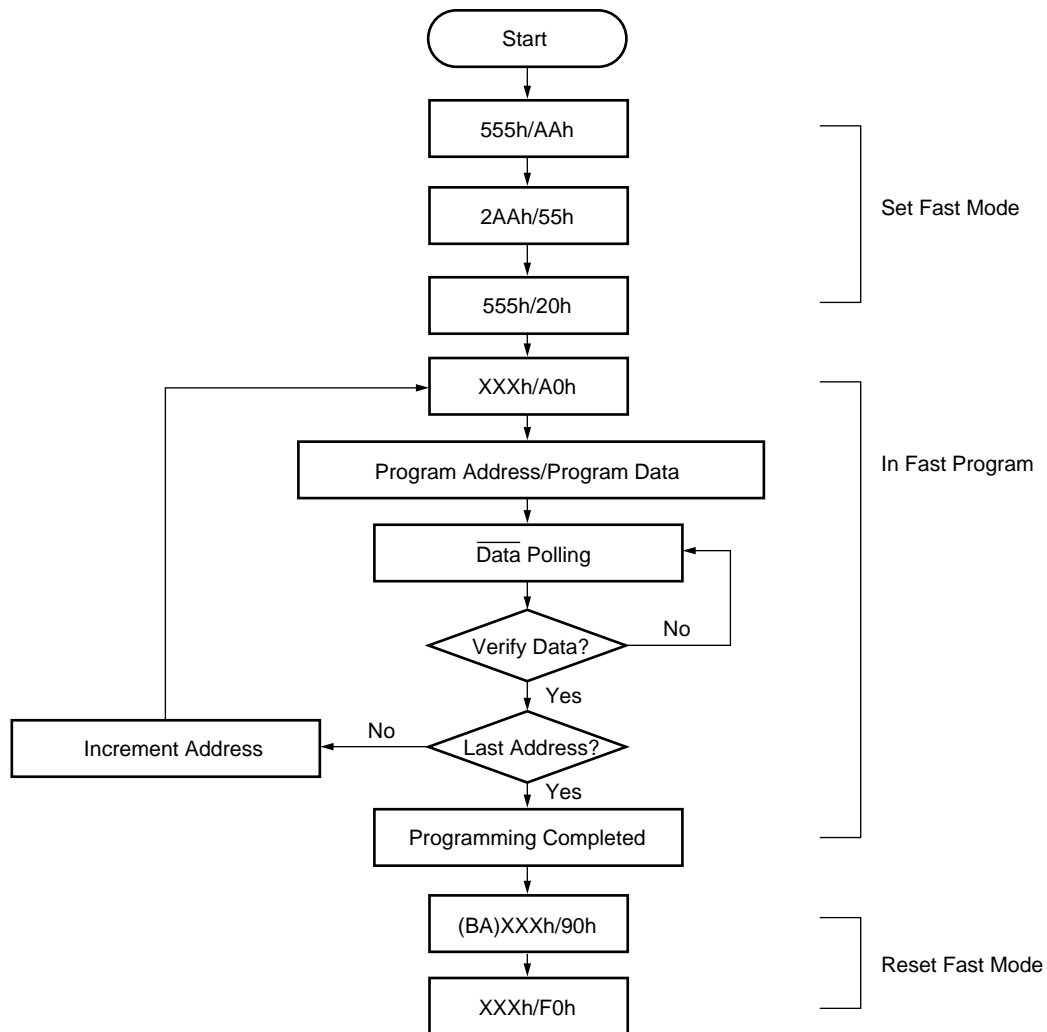
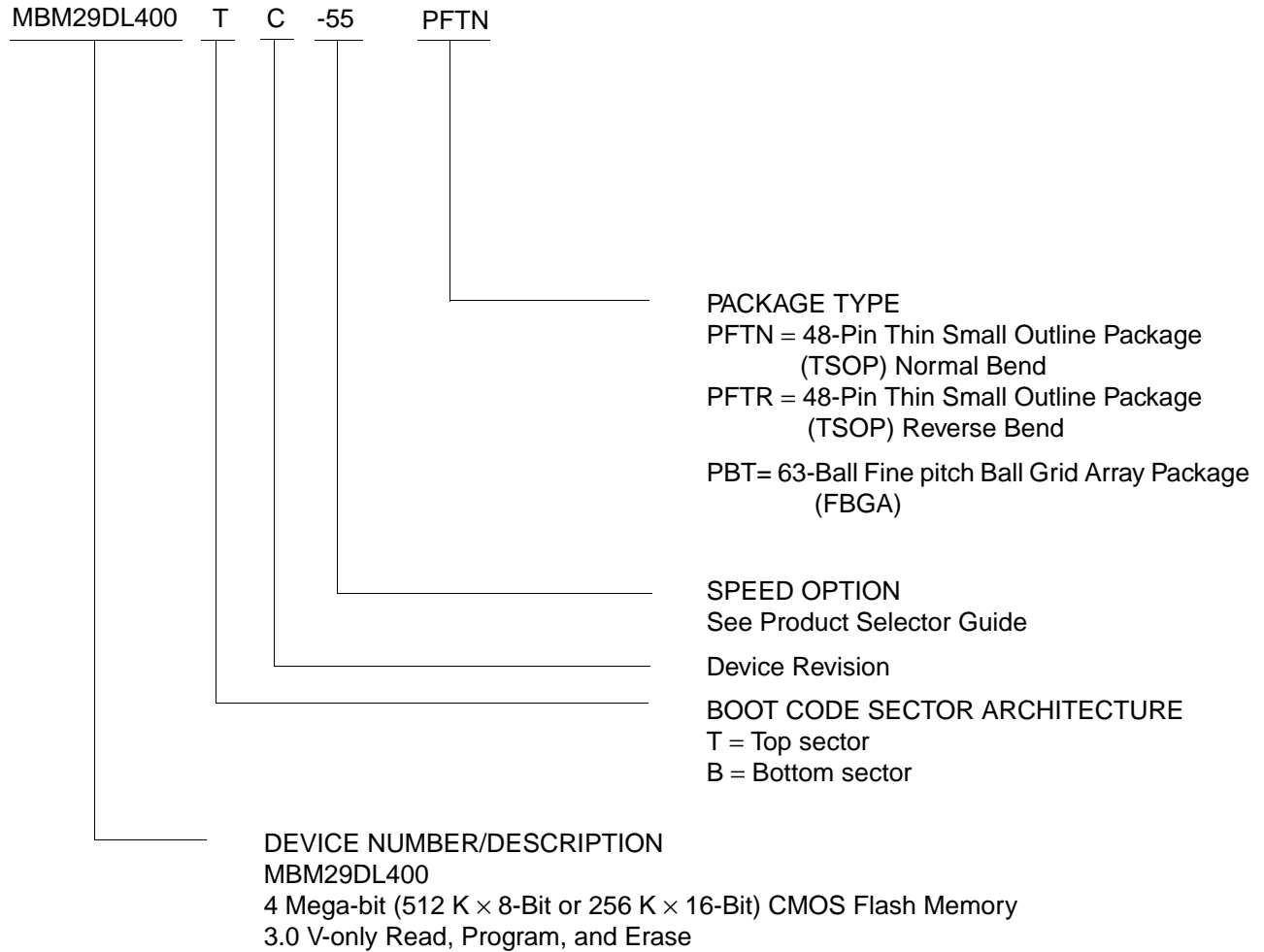Note : The sequence is applied for ×16 mode.
The addresses differ from ×8 mode.

Valid Combinations
Valid Combinations list configurations planned to be supported in volume for this device.
Consult the local Fujitsu sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Embedded Programming Algorithm for Fast Mode

■ ORDERING INFORMATION

Standard Products

Fujitsu standard products are available in several packages. The order number is formed by a combination of :

MBM29DL400   T   C   -55   PFTN

PACKAGE TYPE
PFTN = 48-Pin Thin Small Outline Package
(TSOP) Normal Bend
PFTR = 48-Pin Thin Small Outline Package
(TSOP) Reverse Bend

PBT= 63-Ball Fine pitch Ball Grid Array Package
(FBGA)

SPEED OPTION
See Product Selector Guide

Device Revision

BOOT CODE SECTOR ARCHITECTURE
T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION
MBM29DL400
4 Mega-bit (512 K × 8-Bit or 256 K × 16-Bit) CMOS Flash Memory
3.0 V-only Read, Program, and Erase

Valid Combinations		
MBM29DL400 TC/BC	55	TN
	70	TR
	90	PBT

■ **PACKAGE DIMENSIONS**

48-pin plastic TSOP (I)
(FPT-48P-M19)

Note 1: *:Values do not include resin protrusion.
Resin protrusion and gate protrusion are +0.15(.006)Max(each side).
Note 2: Pins width and pins thickness include plating thickness.

LEAD No.

① INDEX ㊽

㉔ ㉕

Details of "A" part

0.25(.010)

0~8°

0.60±0.15
(.024±.006)

20.00±0.20
(.787±.008)

* 18.40±0.20
(.724±.008)

"A"

⬭ 0.10(.004)

* 12.00±0.20
(.472±.008)

$1.10 ^{+0.10}_{-0.05}$
$\left(.043 ^{+.004}_{-.002}\right)$
(Mounting height)

0.10±0.05
(.004±.002)
(Stand off height)

0.50(.020)
TYP

$0.17 ^{+0.03}_{-0.08}$
$\left(.007 ^{+.001}_{-.003}\right)$

0.22±0.05
(.009±.002)

⊕ 0.10(.004) Ⓜ
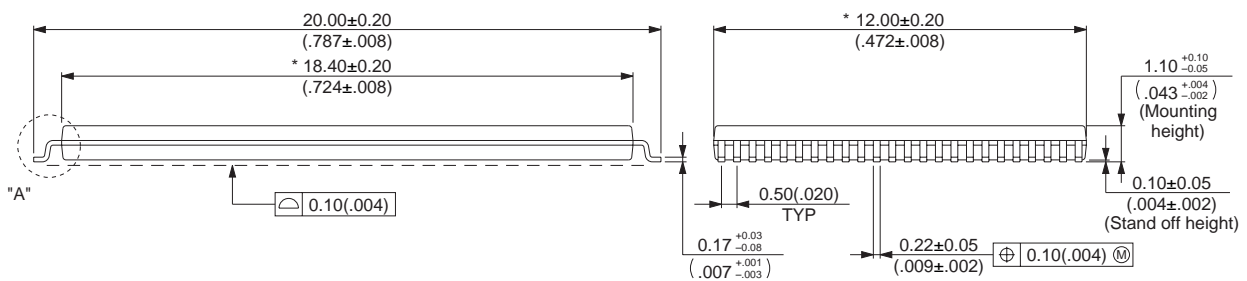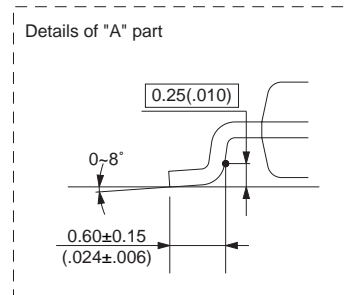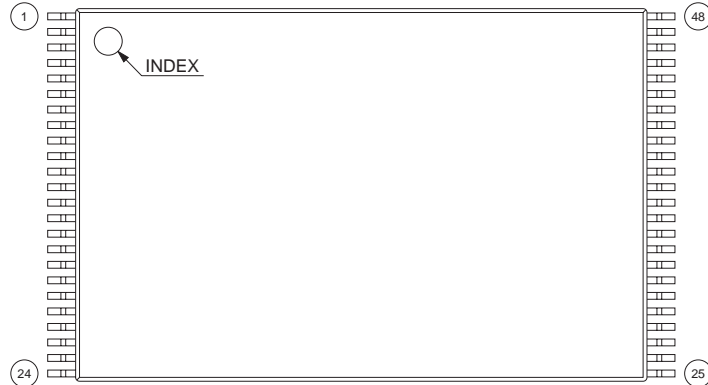
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Dimensions in mm (inches)

(Continued)

48-pin plastic TSOP (I)
(FPT-48P-M20)

Note 1: *:Values do not include resin protrusion.
Resin protrusion and gate protrusion are +0.15(.006)Max(each side).
Note 2: Pins width and pins thickness include plating thickness.

LEAD No.

INDEX

Details of "A" part

0.60±0.15
(.024±.006)

0~8°

0.25(.010)

0.17 +0.03 −0.08
(.007 +.001 −.003)

0.22±0.05
(.009±.002)

0.10(.004) Ⓜ

0.50(.020)
TYP

0.10±0.05
(.004±.002)
(Stand off height)

0.10(.004)

"A"

* 18.40±0.20
(.724±.008)

20.00±0.20
(.787±.008)

1.10 +0.10 −0.05
(.043 +.004 −.002)
(Mounting height)

* 12.00±0.20(.472±.008)
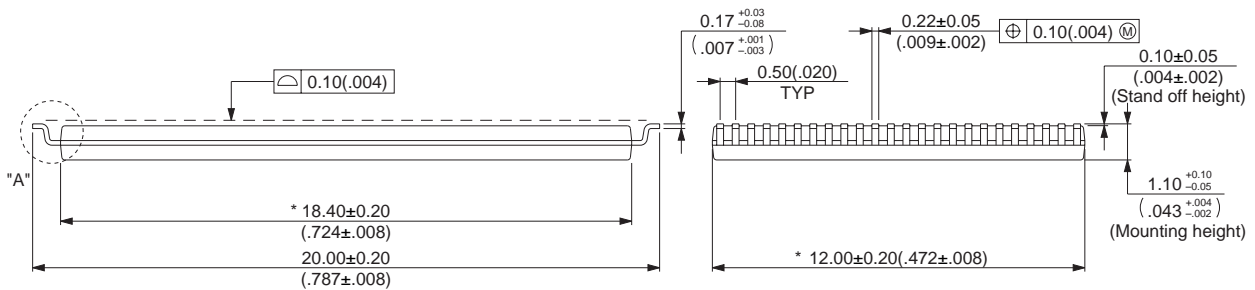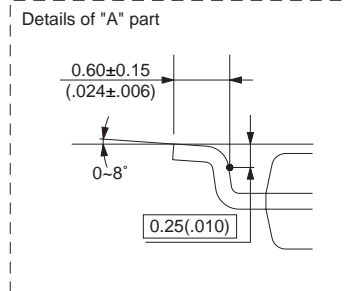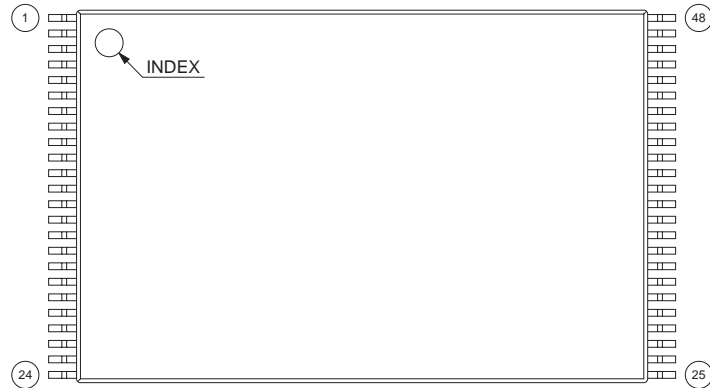
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Dimensions in mm (inches)

(Continued)

MBM29DL400TC/BC-55/70/90

(Continued)

48-pin plastic FBGA
(BGA-48P-M11)

8.00±0.20(.315±.008)

INDEX

6.00±0.20
(.236±.008)

C0.25(.010)

1.05 $^{+0.15}_{-0.10}$ (.041 $^{+.006}_{-.004}$)
(Mounting height)

0.38±0.10(.015±.004)
(Stand off)

(5.60(.220))

0.80(.031)TYP

(4.00(.157))

6
5
4
3
2
1

H G F E D C B A

48-ø0.45±0.10
(48-ø.018±.004) ⊕ ø0.08(.003) Ⓜ

0.10(.004)
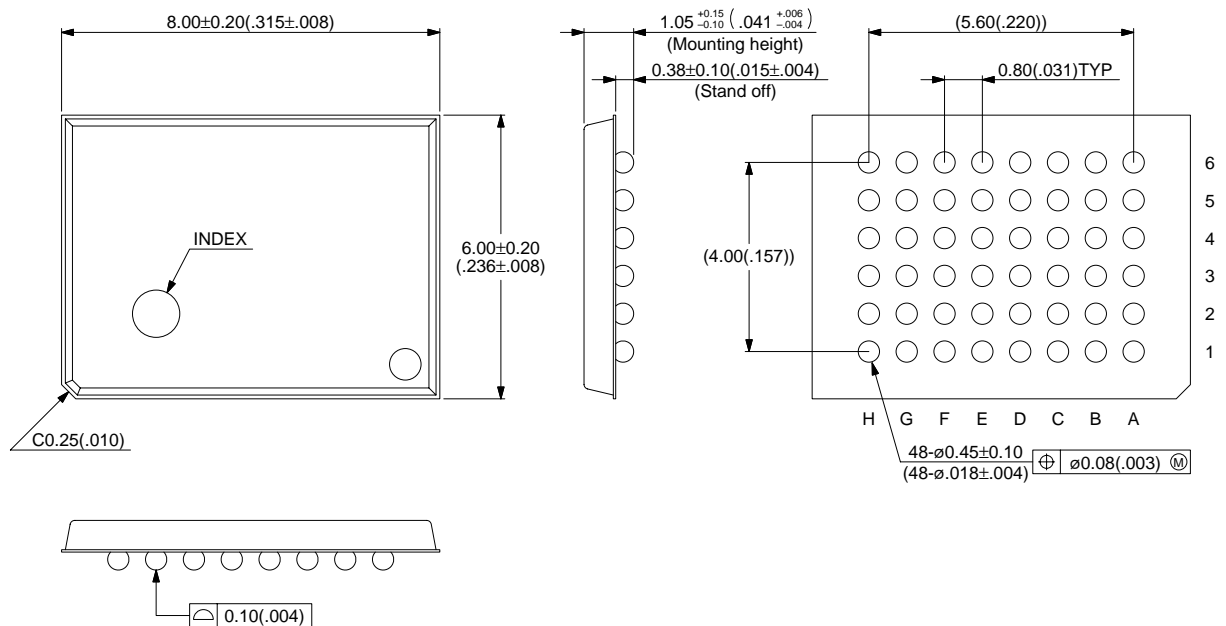
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Dimensions in mm (inches)

56

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