NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PARTS
ISL97671A or ISL97672B

ISL97673

6-Channel SMBus or PWM Dimming LED Driver with Phase Shift Control

ISL97673

The ISL97673 is a 6-Channel 45V dual dimming capable LED driver that can be used with either SMBus/I^{2}C or PWM signal for dimming control. The ISL97673 drives 6 channels of LED to support 78 LEDs from 4.5V to 26V or 48 LEDs from a boost supply of 2.7V to 26V and a separate 5V bias on the ISL97673 VIN pin

The ISL97673 compensates for non-uniformity of the forward voltage drops in the LED strings with its 6 voltage controlled-current source channels. Its headroom control monitors the highest LED forward voltage string for output regulation, to minimize the voltage headroom and power loss in a typical multi-string operation.

The ISL97673 features optional channel phase shift control to minimize the input, output ripple characteristics and load transients as well as spreading the light output to help reduce the video and audio interference from the backlight driver operation. The phase shift can be programmed with equal phase angle or adjustable in 7-bit resolution.

The ISL97673 has a full range of dimming capabilities that include SMBus/I^{2}C controlled PWM dimming or DC dimming. Another key feature of the ISL97673 is that it allows very linear PWM dimming from 0.4% to 100% of up to 30kHz. Current matching of 0.4% to 100% dimming achieves ±1% tolerance from 100Hz to 5kHz dimming and ±3% tolerance from 5kHz to 30kHz dimming.

Features

- 6 Channels
- 4.5V to 26.5V Input
- 45V Output Max
- Up to 40mA LED Current per channel
- Extensive Dimming Control
  - PWM/DPST Dimming, I^{2}C 8-bit with equal phase shift, and 0.007% Direct PWM dimming at 200Hz
- Optional Master Fault Protection
- PWM Dimming Linearity 0.4%~100% <30kHz
- 600kHz/1.2MHz selectable switching frequency
- Dynamic Headroom Control
- Protections with Flag Indication
  - String Open/Short Circuit, V_{OUT} Short Circuit, Overvoltage and Over-Temperature Protections
  - Optional Master Fault Protection
- Current Matching ±0.7%
- 20 Ld 4mmx3mm QFN Package

Applications

- Notebook Displays WLED or RGB LED Backlighting
- LCD Monitor LED Backlighting
- Automotive Displays LED Backlighting

Typical Application Circuit

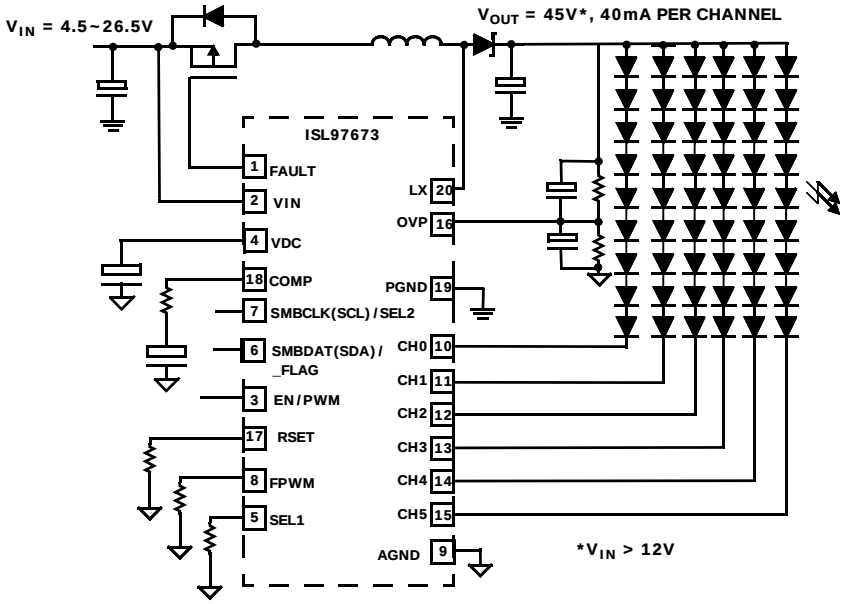


FIGURE 1. ISL97673 TYPICAL APPLICATION DIAGRAM

Block Diagram

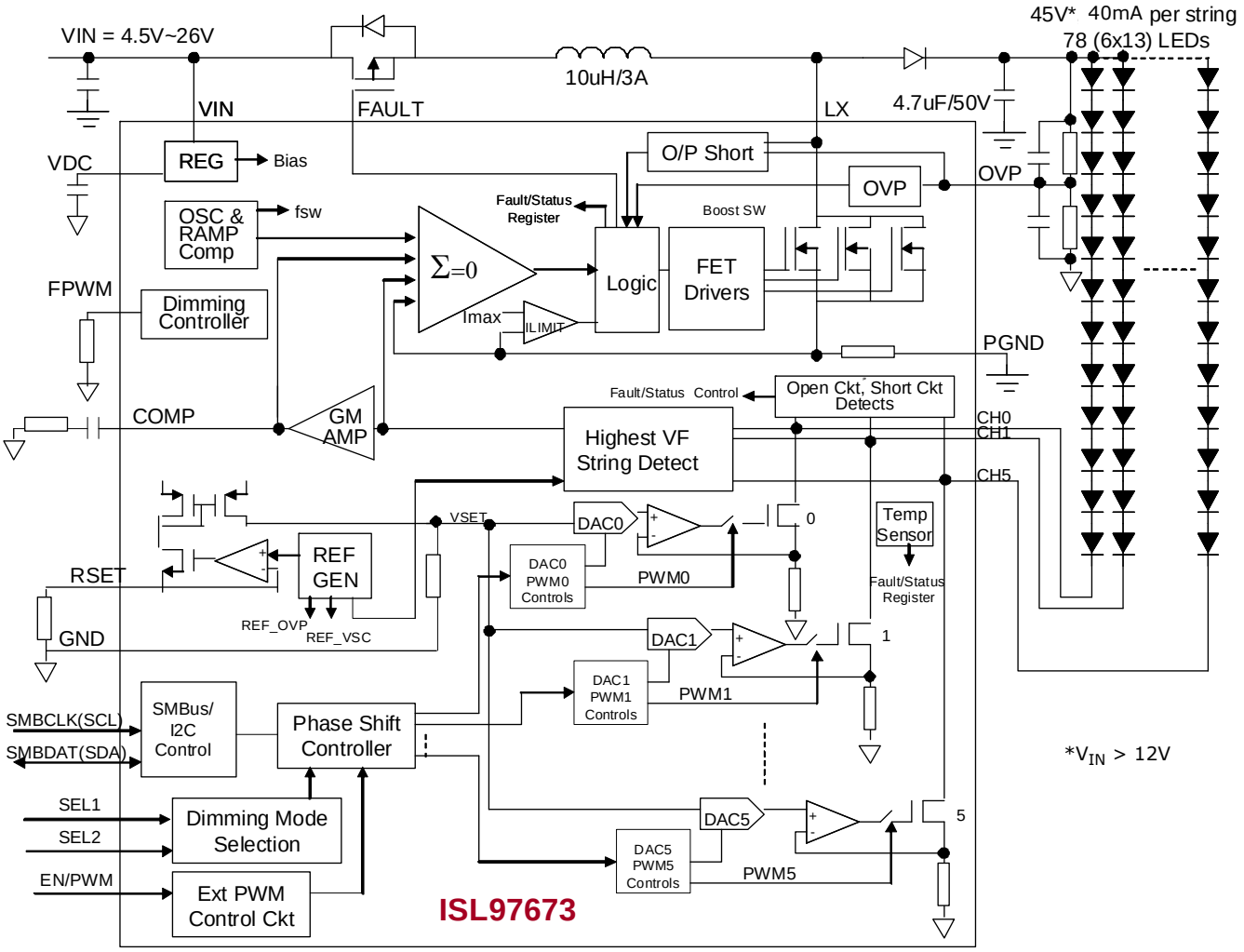


FIGURE 2. ISL97673 BLOCK DIAGRAM

Ordering Information

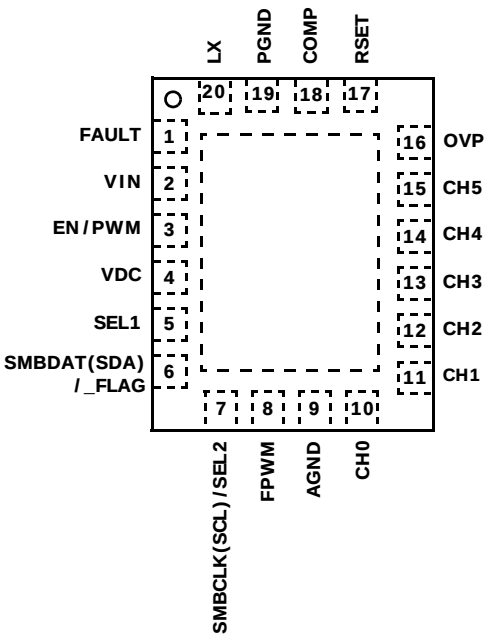
PART NUMBER (Notes 1, 2)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL97673IRZ	7673	20 Ld 4x3 QFN	L20.3x4
ISL97673IRZ-EVAL	Evaluation Board		

NOTES:

1. Add "-T" or "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL97673. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL97673
(20 LD QFN)
TOP VIEW



Pin Descriptions (I = Input, O = Output, S = Supply)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
FAULT	1	O	Fault disconnect switch
VIN	2	S	Input voltage for the device and LED power
EN/PWM	3	I	Dual Functions: Enable pin and PWM brightness control pin or DPST control input. The device needs 4ms for initial power-up Enable, then this pin can be applied with a PWM signal with off time no longer than 28ms.
VDC	4	S	De-couple capacitor for internally generated supply rail.
SEL1	5	I	Mode select pin 1
SMBDAT(SDA)/_FLAG	6	I/O	When SEL1 is high, this pin is configured as the SMBus/I^2C serial data input/output. When SEL1 is low or floating, this pin is configured as the fault flag output and will be pulled low when a fault condition occurs. An external pull-up is required.
SMBCLK(SCL)/SEL2	7	I	When SEL1 is high, this pin is configured as the SMBus/I^2C serial clock input. When SEL1 is low or floating, this pins is configured as mode select pin 2, and operates in conjunction with SEL1 to determine the operating mode. See Table 1 for details.
FPWM	8	I	PWM Dimming Frequency Set Pin with RFPWM
AGND	9	S	Analog Ground for precision circuits
CH0, CH1, CH2, CH3, CH4, CH5	10, 11, 12, 13, 14, 15	I	Input 0, Input 1, Input 2, Input 3, Input 4, Input 5 to current source, FB, and monitoring
OVP	16	I	Overvoltage protection input
RSET	17	I	Resistor connection for setting LED current, (see Equation 2 for calculating the ILEDpeak)
COMP	18	O	Boost compensation pin
PGND	19	S	Power ground
LX	20	O	Input to boost switch

Table of Contents

Absolute Maximum Ratings (T_A = +25°C)

VIN, EN/PWM. . . . . -0.3V to 28V
FAULT . . . . . VIN - 8.5V to VIN + 0.3V
VDC, COMP, RSET, FPWM, OVP. . . . . -0.3V to 5.5V
SMBCLK(SCL), SMBDAT(SDA) . . . . . -0.3V to 5.5V
CH0 - CH5, LX . . . . . -0.3V to 45V
PGND, AGND . . . . . -0.3V to +0.3V
Above voltage ratings are all with respect to AGND pin
ESD Rating
Human Body Model (Tested per JESD22-A114E) 3kV
Machine Model (Tested per JESD22-A115-A). 300V
Charged Device Model 1kV

Thermal Information

	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Thermal Resistance (Typical)		
20 Ld QFN Package (Notes 4, 5, 7)	40	2.5

	PSI_{JT} (°C/W)
Thermal Characterization (Typical)	
20 Ld QFN Package (Note 6)	1

Maximum Continuous Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . .-40°C to +85°C

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. PSI_{JT} is the PSI junction-to-top thermal characterization parameter. If the package top temperature can be measured with this rating then the die junction temperature can be estimated more accurately than the θ_{JC} and θ_{JC} thermal resistance ratings
7. Refer to JESD51-7 high effective thermal conductivity board layout for proper via and plane designs.

Electrical Specifications

All specifications below are tested at T_A = +25°C; V_{IN} = 12V, EN/PWM = 5V, R_{SET} = 20.1kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
GENERAL						
V_{IN} (Note 9)	Backlight Supply Voltage	≤11 LEDs per channel (3.2V/20mA type)	**4.5**		**26.5**	V
I_{VIN_STBY}	VIN Shutdown Current				**10**	µA
V_{OUT}	Output Voltage	4.5V < V_{IN} ≤ 26V, F_{SW} = 600kHz			**45**	V
		8.55V < V_{IN} ≤ 26V, F_{SW} = 1.2MHz			**45**	V
		4.5V < V_{IN} ≤ 8.55V, F_{SW} = 1.2MHz			**V_{IN} / 0.19**	V
V_{UVLO}	Undervoltage Lock-out Threshold		**2.6**		**3.3**	V
V_{UVLO_HYS}	Undervoltage Lock-out Hysteresis			275		mV
REGULATOR						
V_{DC}	LDO Output Voltage	V_{IN} > 6V	**4.55**	4.8	**5**	V
I_{VDC_STBY}	Standby Current	EN/PWMI = 0V			**5**	µA
I_{VDC}	Active Current	EN/PWMI = 5V		5		mA
V_{LDO}	VDC LDO Droop Voltage	V_{IN} > 5.5V, 20mA		20	**200**	mV
EN_{Low}	Guaranteed Range for EN Input Low Voltage				**0.5**	V
EN_{Hi}	Guaranteed Range for EN Input High Voltage		**1.8**			V
t_{ENLow}	EN/PWMI Low Time Before Shut-down			30.5		ms

Electrical Specifications All specifications below are tested at T_A = +25°C; V_{IN} = 12V, EN/PWM = 5V, R_{SET} = 20.1kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
BOOST						
SW_{ILimit}	Boost FET Current Limit		**1.5**	2.0	2.7	A
$r_{DS(ON)}$	Internal Boost Switch ON-resistance	T_A = +25°C		235	300	mΩ
SS	Soft-start	100% LED Duty Cycle		7		ms
Eff_peak	Peak Efficiency	V_{IN} = 12V, 72 LEDs, 20mA each, L = 10µH with DCR 101mΩ, T_A = +25°C		92.9		%
		V_{IN} = 12V, 60 LEDs, 20mA each, L = 10µH with DCR 101mΩ, T_A = +25°C		90.8		%
$\Delta I_{OUT}/\Delta V_{IN}$	Line Regulation			0.1		%
D_{MAX}	Boost Maximum Duty Cycle	FSW = 1, 600kHz	**90**			%
		FSW = 0, 1.2MHz	**81**			
D_{MIN}	Boost Minimum Duty Cycle	FSW = 1, 600kHz			9.5	%
		FSW = 0, 1.2MHz			17	
f_{OSC_hi}	Lx Frequency High	FSW = 1, 600kHz	**475**	600	**640**	kHz
f_{OSC_lo}	Lx Frequency Low	FSW = 0, 1.2MHz	**0.97**	1.14	**1.31**	MHz
ILX_leakage	Lx Leakage Current	LX = 45V, EN = 0			**10**	µA
FAULT DETECTION						
V_{SC}	Short Circuit Threshold Accuracy	Reg0x08, SC[1:0] = 01	**3.15**	3.6	**4.3**	V
		Reg0x08, SC[1:0] = 10	**4.2**	4.8	**5.4**	V
		Reg0x08, SC[1:0] = 11	**5.2**	5.85	**6.6**	V
Temp_shtdwn	Temperature Shutdown Threshold			150		°C
Temp_Hyst	Temperature Shutdown Hysteresis			23		°C
V_{OVPlo}	Overvoltage Limit on OVP Pin		**1.19**		**1.25**	V
OVP_{fault}	OVP Short Detection Fault Level			400		mV
CURRENT SOURCES						
I_{MATCH}	DC Channel-to-Channel Current Matching	R_{SET} = 20.1kΩ, Reg0x00 = 0xFF (I_{OUT} = 20mA)		±0.7	**±1.0**	%
I_{ACC}	Current Accuracy		**-1.5**		**+1.5**	%
$V_{headroom}$	Dominant Channel Current Source Headroom at FBx Pin	I_{LED} = 20mA T_A = +25°C		500		mV
V_{RSET}	Voltage at RSET Pin	R_{SET} = 20.1kΩ	**1.2**	1.22	**1.24**	mV
I_{LEDmax}	Maximum LED Current per Channel	V_{IN} = 12V, V_{OUT} = 45V, Fsw=1.2MHz, T_A = +25°C		40		mA
PWM GENERATOR						
VIL	Guaranteed Range for PWMI Input Low Voltage				**0.8**	V
VIH	Guaranteed Range for PWMI Input High Voltage		**1.5**		**VDD**	V
FPWM	PWMI Input Frequency Range		**200**		**30,000**	Hz
PWMACC	PWM Input Accuracy			8		bits

Electrical Specifications All specifications below are tested at T_A = +25°C; V_{IN} = 12V, EN/PWM = 5V, R_{SET} = 20.1kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
FPWM	PWM Dimming Frequency Range	RFPWM = 660kΩ	90	100	110	Hz
tDIRECTPWM	Direct PWM Minimum On Time	Direct PWM Mode	**250**		**350**	ns
FAULT PIN						
I_{FAULT}	Fault Pull-down Current	V_{IN} = 12V	**12**	21	**30**	µA
V_{FAULT}	Fault Clamp Voltage with Respect to V_{IN}	V_{IN} = 12V, V_{IN} - V_{FAULT}	**6**	7	**8.3**	V
LXStart_thres	Lx Start-up Threshold		**1.3**	1.4	**1.5**	V
IlxStart-up	Lx Start-up Current		**1**	3.5	**5**	mA
SMBus/I²C INTERFACE LOGIC LEVEL						
V_{IL}	Guaranteed Range for Data, Clock Input Low Voltage				**0.8**	V
VIH	Guaranteed Range for Data, Clock Input High Voltage		**1.5**		**VDD**	V
V_{OL}	SMBus/I²C Output Data Line Logic Low Voltage	I_{PULLUP} = 4mA			**0.17**	V
I_{LEAK}	Input Leakage On SMBData/SMBClk	Measured at 4.8V	**-10**		**10**	µA
SMBus/I²C TIMING SPECIFICATIONS (Note 10)						
tEN-SMB/I²C	Minimum Time Between EN high and SMBus/I²C Enabled	1µF capacitor on VDC	**2**			ms
PWS	Pulse Width Suppression on SMBCLK/SMBDAT		0.15		0.45	µs
f_{SMB}	SMBus Clock Frequency				400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition		1.3			µs
$t_{HD:STA}$	Hold Time After (Repeated) START Condition. After this Period, the First Clock is Generated		0.6			µs
$t_{SU:STA}$	Repeated Start Condition Setup Time		0.6			µs
$t_{SU:STO}$	Stop Condition Setup Time		0.6			µs
$t_{HD:DAT}$	Data Hold Time		300			ns
$t_{SU:DAT}$	Data Setup Time		100			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
t_F	Clock/data Fall Time				300	ns
t_R	Clock/data Rise Time				300	ns

NOTES:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Independent from the numbers of LEDs, at minimum V_{IN} of 4.5V, maximum V_{OUT} is limited to 35V. And at maximum V_{IN} of 26.5V, minimum V_{OUT} is limited 28V.
10. Limits established by characterization and are not production tested.

Typical Performance Curves

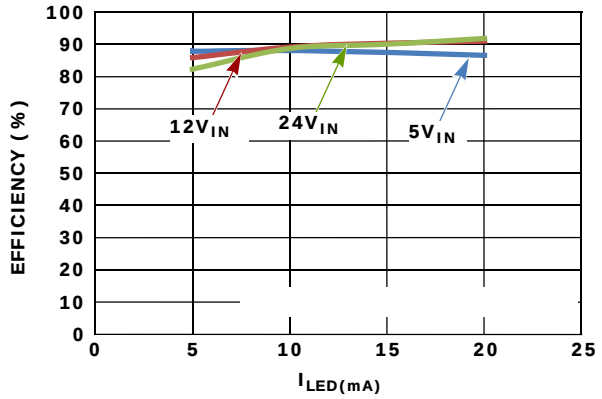


FIGURE 3. EFFICIENCY vs up to 20mA LED CURRENT (100% LED DUTY CYCLE) vs V_{IN}

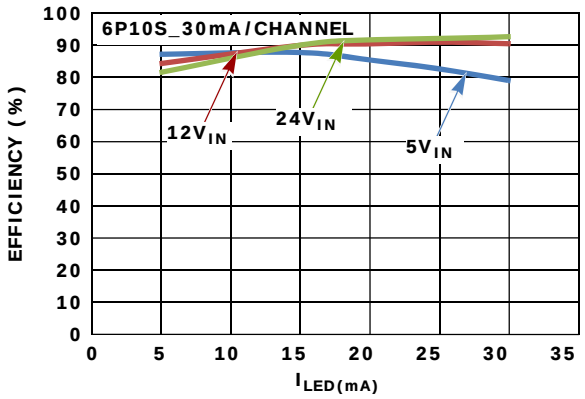


FIGURE 4. EFFICIENCY vs up to 30mA LED CURRENT (100% LED DUTY CYCLE) vs V_{IN}

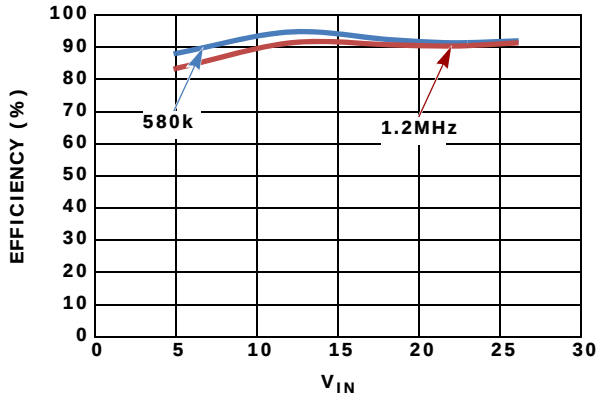


FIGURE 5. EFFICIENCY vs V_{IN} vs SWITCHING FREQUENCY AT 20mA (100% LED DUTY CYCLE)

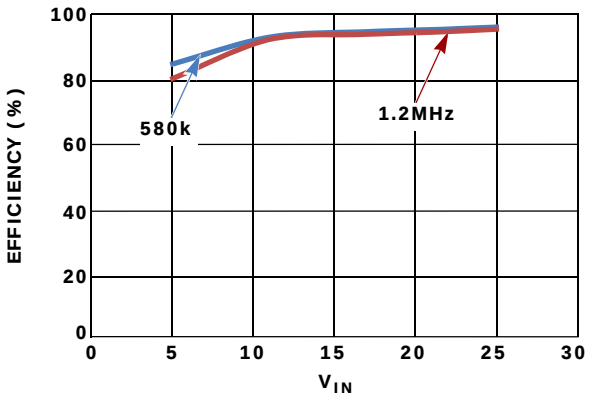


FIGURE 6. EFFICIENCY vs V_{IN} vs SWITCHING FREQUENCY AT 30mA (100% LED DUTY CYCLE)

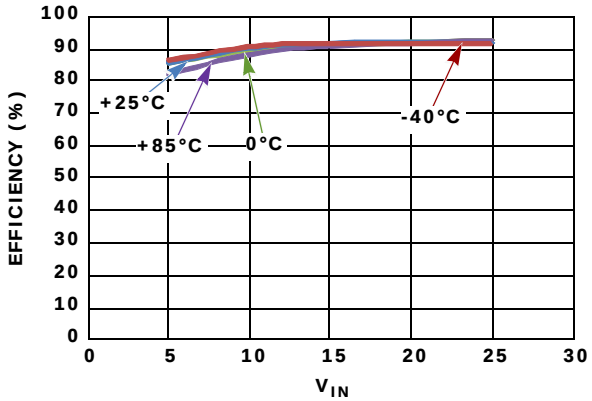


FIGURE 7. EFFICIENCY vs V_{IN} vs TEMPERATURE AT 20mA (100% LED DUTY CYCLE)

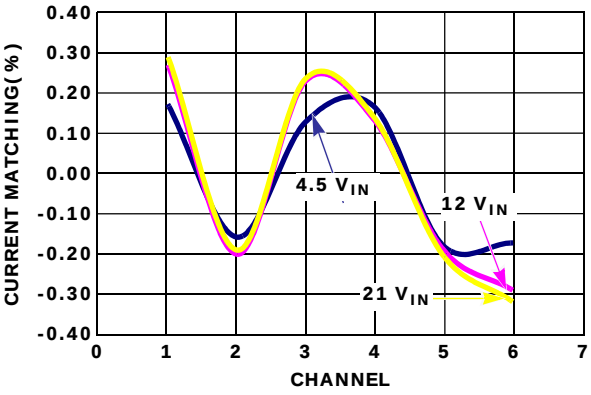


FIGURE 8. CHANNEL-TO-CHANNEL CURRENT MATCHING

Typical Performance Curves (Continued)

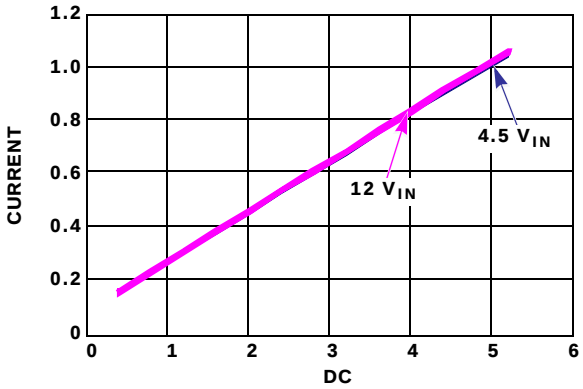


FIGURE 9. CURRENT LINEARITY vs LOW LEVEL PWM DIMMING DUTY CYCLE vs V_{IN}

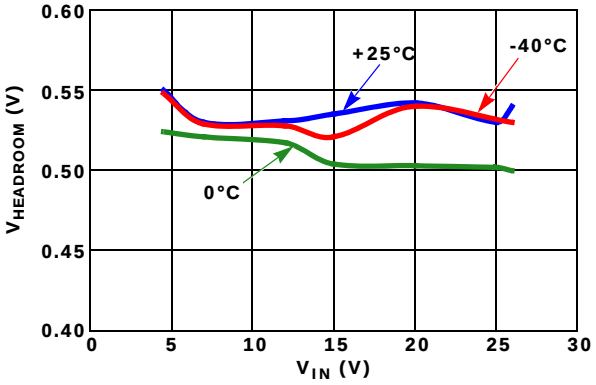


FIGURE 10. $V_{HEADROOM}$ vs V_{IN} AT 20mA

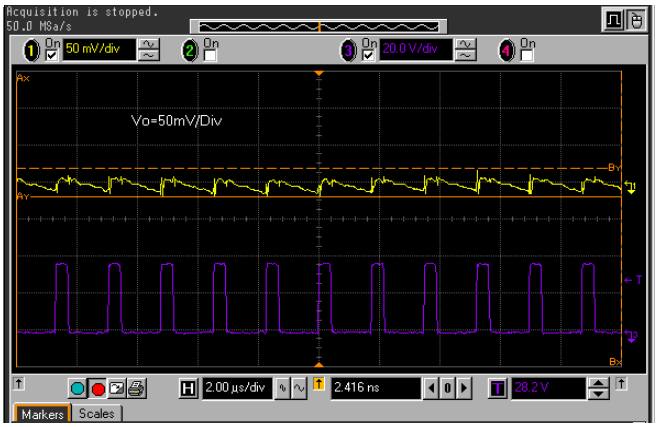


FIGURE 11. V_{OUT} RIPPLE VOLTAGE, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

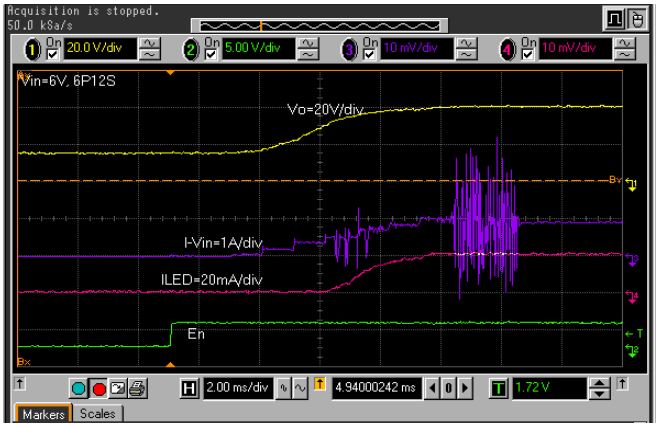


FIGURE 12. IN-RUSH and LED CURRENT AT V_{IN} = 6V FOR 6P12S AT 20mA/CHANNEL

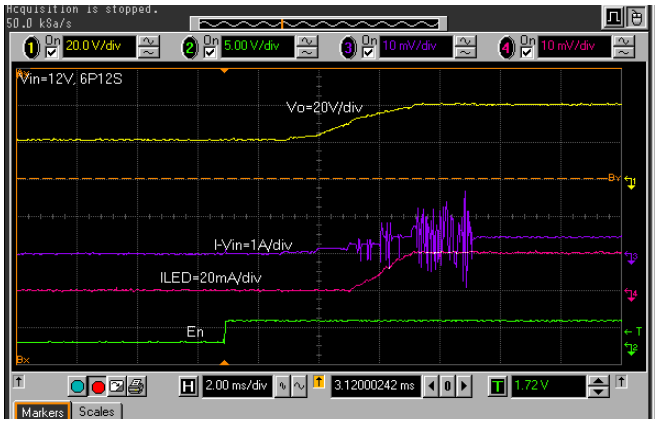


FIGURE 13. IN-RUSH AND LED CURRENT AT V_{IN} = 12V FOR 6P12S AT 20mA/CHANNEL

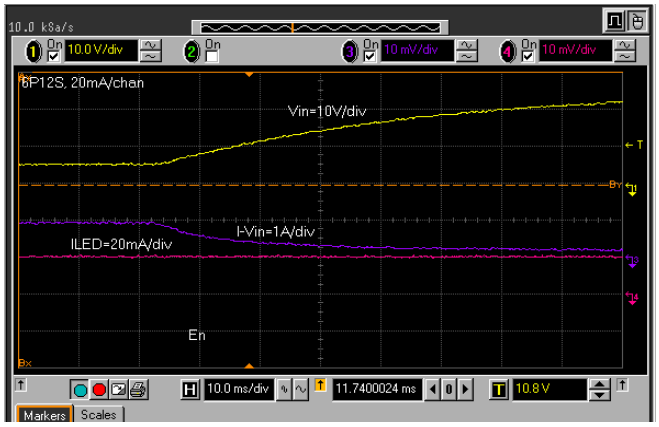


FIGURE 14. LINE REGULATION WITH V_{IN} CHANGE FROM 6V TO 26V, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

Typical Performance Curves (Continued)

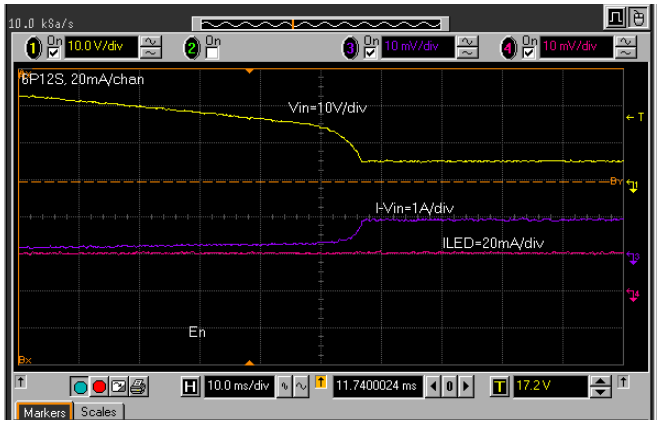


FIGURE 15. LINE REGULATION WITH V_{IN} CHANGE FROM 26V TO 6V FOR 6P12S AT 20mA/CHANNEL

FIGURE 16. LOAD REGULATION WITH I_{LED} CHANGE FROM 0% TO 100% PWM DIMMING, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

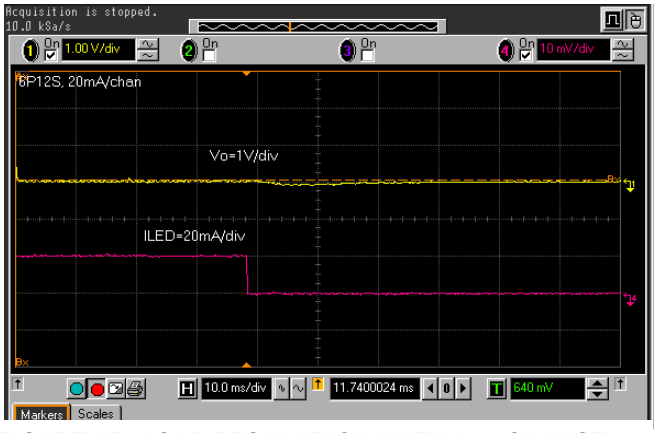


FIGURE 17. LOAD REGULATION WITH I_{LED} CHANGE FROM 100% TO 0% PWM DIMMING, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

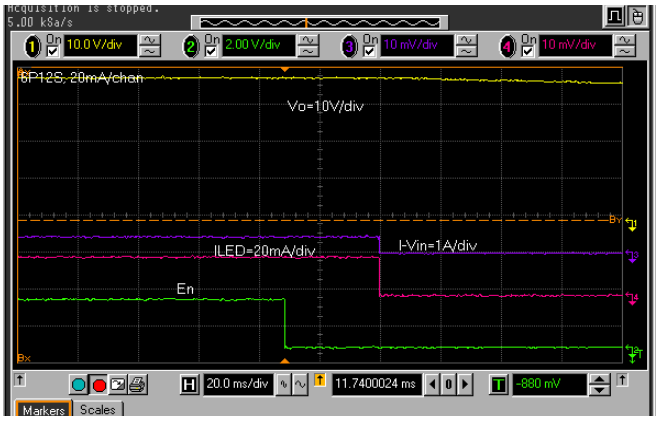


FIGURE 18. ISL97671 SHUTS DOWN AND STOPS SWITCHING ~ 30ms AFTER EN GOES LOW

Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED stack with the highest forward voltage drop to run at the programmed current. The ISL97673 employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. Such architecture achieves a fast transient response that is essential for the notebook backlight application where the power can be a series of drained batteries or instantly change to an AC/DC adapter without rendering a noticeable visual nuisance. The number of LEDs that can be driven by ISL97673 depend on the type of LED chosen in the application. The ISL97673 are capable of boosting up to 45V and typically driving 13 LEDs in series for each of the 6 channels, enabling a total of 104 pieces of the 3.2V/20mA type of LEDs.

Enable and PWM

The ISL97673 has EN/PWM pin that serves dual purposes; it is used as an Enable signal and can be used as a PWM input signal for dimming. If a PWM signal is applied to this pin, the first pulse of minimum 4ms will be used as an Enable signal. If there is no signal for longer than 28ms, the device will enter shutdown.

OVP and V_{OUT} Requirement

The Overvoltage Protection (OVP) pin has a function of setting the overvoltage trip level as well as limiting the V_{OUT} regulation range.

The ISL97673 OVP threshold is set by R_{UPPER} and R_{LOWER} as shown in Equation 1:

$$V_{OUT\_OVP} = 1.21V \times (R_{UPPER} + R_{LOWER})/R_{LOWER} \quad \text{(EQ. 1)}$$

V_{OUT} can only regulate between 64% and 100% of the V_{OUT_OVP} such that:

Allowable V_{OUT} = 64% to 100% of V_{OUT_OVP}

For example, if 10 LEDs are used with the worst case V_{OUT} of 35V. If R_1 and R_2 are chosen such that the OVP level is set at 40V, then the V_{OUT} is allowed to operate between 25.6V and 40V. If the requirement is changed to a 6 LEDs 21V V_{OUT} application, then the OVP level must be reduced and users should follow V_{OUT} = (64% ~100%) OVP requirement. Otherwise, the headroom control will be disturbed such that the channel voltage can be much higher than expected and sometimes it can prevent the driver from operating properly.

The ratio of the OVP capacitors should be the inverse of the OVP resistors. For example, if R_{UPPER}/R_{LOWER} = 33/1, then C_{UPPER}/C_{LOWER} = 1/33 with C_{UPPER} = 100pF and C_{LOWER} = 3.3nF.

Current Matching and Current Accuracy

Each channel of the LED current is regulated by the current source circuit, as shown in Figure 19.

The LED peak current is set by translating the R_{SET} current to the output with a scaling factor of $410.5/R_{SET}$. The source terminals of the current source MOSFETs are designed to run at 500mV to optimize power loss versus accuracy requirements. The sources of errors of the channel-to-channel current matching come from the op amps offset, internal layout, reference, and current source resistors. These parameters are optimized for current matching and absolute current accuracy. However, the absolute accuracy is additionally determined by the external R_{SET}. A 1% tolerance resistor is recommended.

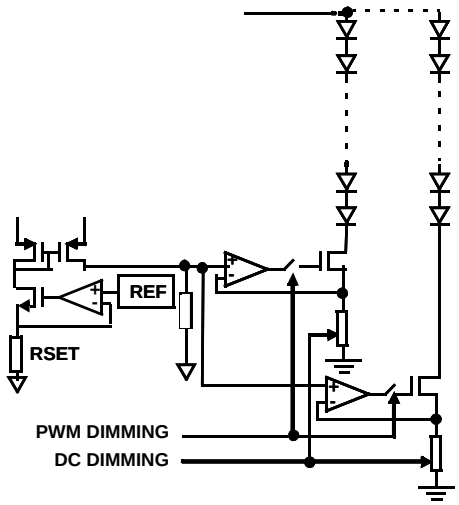


FIGURE 19. SIMPLIFIED CURRENT SOURCE CIRCUIT

Dynamic Headroom Control

The ISL97673 features a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string or effectively the lowest voltage from any of the CH0-CH5 pins digitally. When the lowest channel voltage is lower than the short circuit threshold, V_{SC}, such voltage will be used as the feedback signal for the boost regulator. The boost makes the output to the correct level such that the lowest channel is at the target headroom voltage. Since all LED stacks are connected to the same output voltage, the other channel pins will have a higher voltage, but the regulated current source circuit on each channel will ensure that each channel has the same current. The output voltage will regulate cycle-by-cycle and it is always referenced to the highest forward voltage string in the architecture.

Operating Modes

The ISL97673 has extensive operating modes such as SMBus controlled PWM or DC dimmings, PWM dimming with phase shift control and more. Depending on the pin 5 (SEL1) condition, pins 6 and 7 correspond to different operating modes as shown in Table 1.

TABLE 1.

SEL1	SEL2	OPERATING MODE
High	N/A	Selectable by SMBus/I^{2}C Interface
Float	High	PWMI, Fixed-Delay Phase Shift PWM
Float	Float	PWMI, Equal-Phase Phase Shift PWM
Float	Low	PWMI, No-Delay PWM
Low	High	Not Used
Low	Float	DC Current Adjustment
Low	Low	Direct PWM

- When SEL1 is high, Pins 6 and 7 Correspond to SMBDAT and SMBCLK Accordingly. The dimming duty cycle is controlled by the SMBus/I^{2}C communications and the dimming frequency is set by RFPWM.
- When SEL1 is floating and SEL2 is high, the channels will be in phase shift mode with fixed delay. The dimming signal is derived from the applied PWMI signal and the dimming frequency is set by RFPWM.
- When SEL1 is floating and SEL2 is floating, the channels will be in phase shift mode with equal phase. The dimming signal is derived from the applied PWMI signal and the dimming frequency is set by RFPWM.
- When SEL1 is floating and SEL2 is low, the channels phase shift mode is disabled. The dimming signal is derived from the applied PWMI signal and the dimming frequency is set by RFPWM.
- When SEL1 is low and SEL2 is high, this combination is not used thus the operation will not change.
- When SEL1 is low and SEL2 is floating, it is in DC dimming mode such that the output current is averaged in DC and is proportional to the applied PWMI signal duty cycle.
- When SEL1 is low and SEL2 is low, it is in direct PWM mode such that the dimming follows directly from the applied PWMI signal.

Dimming Controls

The ISL97673 allow two ways of controlling the LED current, and therefore, the brightness. They are:

1. DC current adjustment
2. PWM chopping of the LED current defined in Step 1.

There are various ways to achieve DC or PWM current control, which will be described in the following.

MAXIMUM DC CURRENT SETTING

The initial brightness should be set by choosing an appropriate value for R_{SET}. This should be chosen to fix the maximum possible LED current:

$$I_{LEDmax} = \frac{(410.5)}{R_{SET}} \quad \text{(EQ. 2)}$$

DC CURRENT ADJUSTMENT

Once R_{SET} is fixed, the LED DC current can be adjusted through Register 0x07 (BRTDC) as Equation 3:

$$I_{LED} = 1.58x(BRTDC/R_{SET}) \quad \text{(EQ. 3)}$$

BRTDC can be programmed from 0 to 255 in decimal and defaults to 255 (0xFF). If left at the default value, LED current will be fixed at I_{LEDmax}. BRTDC can be adjusted dynamically on the fly during operation and a "0" value disconnects all channels.

For example, if the maximum required LED current ($I_{LED(max)}$) is 20mA, rearranging Equation 2 yields Equation 4:

$$R_{SET} = 410.5/0.02 = 20.52k\Omega \quad \text{(EQ. 4)}$$

If BRTDC is set to 200 then:

$$I_{LED} = 1.58 \bullet 200/20100 = 15.7mA \quad \text{(EQ. 5)}$$

PWM CONTROL

The ISL97673 provides two different PWM dimming methods, as described in the following. Each of these methods results in PWM chopping of the current in the LEDs for all 6 channels to provide an average LED current. During the On periods, the LED current will be defined by the value of R_{SET} and BRTDC, as described in Equations 2 and 3. The source of the PWM signal can be described as follows:

1. **SMBus/I^{2}C generated** 256 level duty cycle programmed through the SMBus/I^{2}C.
2. **External** signal from PWM.

The default PWM dimming is in SMBus/I^{2}C mode. In both methods, the average LED current of each channel is controlled by I_{LED} and the PWM duty cycle in percent as:

$$I_{LED(ave)} = I_{LED} \times PWM \quad \text{(EQ. 6)}$$

Method 1 (SMBus/I^{2}C controlled PWM)

To use this mode, users need to set Register 0x01 to 0x05 with EN/PWM in logic high.

The average LED current of each channel is controlled by the SMBus/I^{2}C setting as:

$$I_{LED(ave)} = I_{LED} \times (BRT/255) \quad \text{(EQ. 7)}$$

where BRT is the PWM brightness level programmed in the Register 0x00. BRT ranges from 0 to 255 in decimal and defaults to 255 (0xFF). BRT = 0 disconnects all channels.

Method 2 (External applied PWM)

To use this mode users need to set Register 0x01 to 0x03

The average LED current of each channel can also be controlled by an external PWM signal as Equation 8:

$$I_{LILED(ave)} = I_{LED} \times PWM \quad \text{(EQ. 8)}$$

PWM Dimming Frequency Adjustment (Applicable to SMBus/ I²C controlled PWM and DPST Modes)

Except for the external PWM dimming mode, the dimming frequencies of any other modes are set by an external resistor at the FPWM pin as Equation 9:

$$F_{PWM} = \frac{6.66 \times 10^7}{RFPWM} \quad \text{(EQ. 9)}$$

where F_{PWM} is the desirable PWM dimming frequency and R_{FPWM} is the setting resistor.

The PWM dimming frequency can be set or applied up to 30kHz with duty cycle from 0.4% to 100%.

PHASE SHIFT CONTROL

The ISL97673 is capable of delaying the phase of each current source to minimize load transients. By default, phase shifting is disabled as shown in Figure 20 where the channels PWM currents are switching uniformly. The duty cycles can be controlled by the data in PWM Brightness Control Register via the SMBus/I²C interface, an external PWM signal with the frequency set by the RFPWM, or by an external PWM signal with the frequency set by the incoming signal.

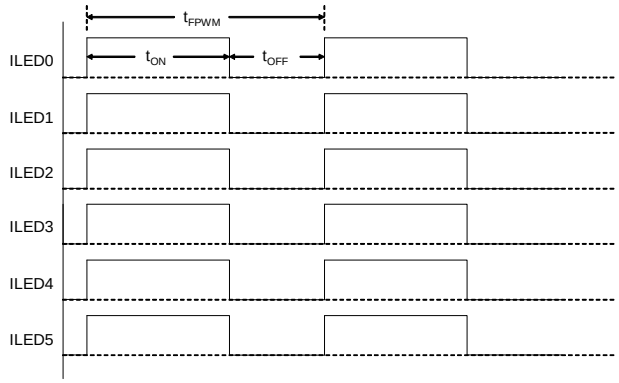


FIGURE 20. NO DELAY (DEFAULT PHASE SHIFT DISABLED)

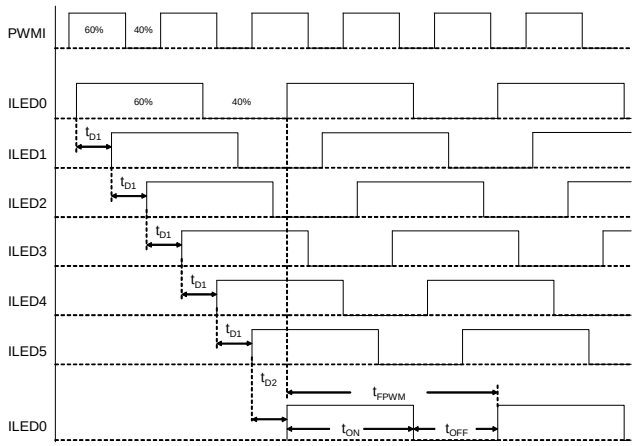


FIGURE 21. 6 EQUAL PHASE CHANNELS PHASE SHIFT ILLUSTRATION

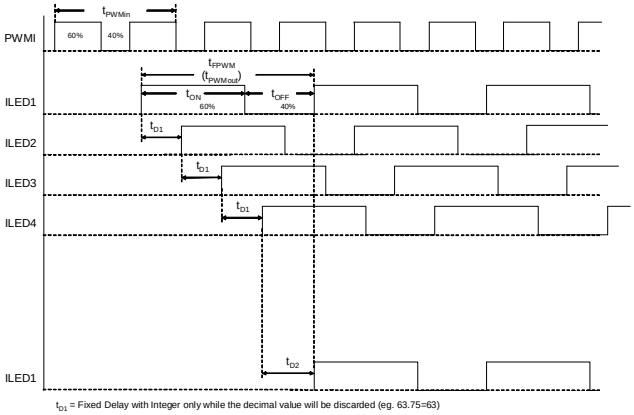


FIGURE 22. 4 EQUAL PHASE CHANNELS PHASE SHIFT ILLUSTRATION

When EqualPhase = 1, the phase shift evenly spreads the channels switching across the PWM cycle, depending on how many channels are enabled, as shown in Figures 21 and 22. Equal phase means there are fixed delays between channels and such delay can be calculated as Equations 10 and 11:

$$t_{D1} = \frac{t_{FPWM}}{255} x\left(\frac{255}{N}\right) \quad \text{(EQ.10)}$$

$$t_{D2} = \frac{t_{FPWM}}{255} x\left(255 - (N-1)\left(\frac{255}{N}\right)\right) \quad \text{(EQ.11)}$$

where (255/N) is rounded down to the nearest integer. For example, if N = 6, (255/N) = 42, that leads to:

$t_{D1} = t_{FPWM}$ x 42/255

$t_{D2} = t_{FPWM}$ x 45/255

where t_{FPWM} is the sum of t_{ON} and t_{OFF}. N is the number of LED channels. The ISL97673 will detect the numbers of operating channels automatically.

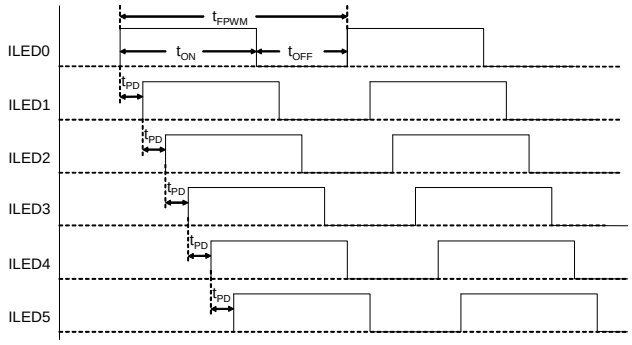


FIGURE 23. PHASE SHIFT WITH 7-BIT PROGRAMMABLE DELAY

The ISL97673 allows the user to program the amount of phase shift degree in 7-bit resolution, as shown in Figure 24. To enable programmable phase shifting, the user must write to the Phase Shift Control register with EqualPhase = 0 and the desirable phase shift value of PhaseShift[6:0]. The delay between CH5 and the repeated CH0 is the rest of the PWM cycle.

Switching Frequency

There are 2 levels of switching frequencies enable for the boost regulator's control of the LX pin: 600kHz or 1.2MHz. Each can be programmed in the Configuration Register 0x08 bit 2. The default switching frequency is at 600kHz.

5V Low Dropout Regulator

A 5V LDO regulator is present at the VDC pin to develop the necessary low voltage supply, which is used by the chips internal control circuitry. Because VDC is an LDO pin, it requires a bypass capacitor of 1µF or more for the regulation. Low input voltage also allows only lower output voltage applications only with the maximum boost ratio defined in "Components Selections" on page 24. The VDC pin can be used as a coarse reference with a few mA sourcing capability.

In-rush Control and Soft-start

The ISL97673 has separately built in independent in-rush control and soft-start functions. The in-rush control function is built around the short circuit protection FET, and is only available in applications, which include this device. At start-up, the fault protection FET is turned on slowly due to a 15µA pull-down current output from the FAULT pin. This discharges the fault FET's gate-source capacitance, turning on the FET in a controlled fashion. As this happens, the output capacitor is charged slowly through the weakly turned on FET before it becomes fully enhanced. This results in a low in-rush current. This current can be further reduced by adding a capacitor (in the 1nF to 5nF range) across the gate-source terminals of the FET.

Once the chip detects that the fault protection FET is turned on hard, it is assumed that in-rush has completed. At this point, the boost regulator will begin to switch and the current in the inductor will ramp-up. The current in the boost power switch is monitored and the switching is terminated in any cycle where the current exceeds the current limit. The ISL97673 includes a soft-start feature where this current limit starts at a low value (275mA). This is stepped up to the final 2.2A current limit in 7 further steps of 275mA. These steps will happen over at least 8ms, and will be extended at low LED PWM frequencies if the LED duty cycle is low. This allows the output capacitor to be charged to the required value at a low current limit and prevents high input current for systems that have only a low to medium output current requirement.

For systems with no master fault protection FET, the inrush current will flow towards C_{OUT} when VIN is applied and it is determined by the ramp rate of VIN and the values of C_{OUT} and L.

Fault Protection and Monitoring

The ISL97673 features extensive protection functions to cover all the perceivable failure conditions. The failure mode of a LED can be either open circuit or as a short. The behavior of an open circuited LED can additionally take the form of either infinite resistance or, for some LEDs, a zener diode, which is integrated into the device in parallel with the now opened LED.

For basic LEDs (which do not have built-in zener diodes), an open circuit failure of an LED will only result in the loss of one channel of LEDs without affecting other channels. Similarly, a short circuit condition on a channel that results in that channel being turned off does not affect other channels unless a similar fault is occurring. LED faults are reported via the SMBus/I^2C interface to Register 0x02 (Fault/Status register). The controller is able to determine which channels have failed via Register 0x09 (Output Masking register). The controller can also choose to use Register 0x09 to disable faulty channels at start-up, resulting in only further faulty channels being reported by Register 0x02.

Due to the lag in boost response to any load change at its output, certain transient events (such as LED current steps or significant step changes in LED duty cycle) can transiently look like LED fault modes. The ISL97673 uses feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED stacks to fault out. See Table 2 for more details.

A fault condition that results in high input current due to a short on V_{OUT} will result in a shutdown of all output channels. The control device logic will remain functional such that the Fault/Status Register can be interrogated by the system. The root cause of the failure will be loaded to the volatile Fault/Status Register so that the host processor can interrogate the data for failure monitoring.

Short Circuit Protection (SCP)

The short circuit detection circuit monitors the voltage on each channel and disables faulty channels which are detected above the programmed short circuit threshold.

There are three selectable levels of short circuit threshold (3.6V, 4.8V, and 5.85V) that can be programmed through the Configuration Register 0x08. When an LED becomes shorted, the action taken is described in Table 2. The default short circuit threshold is 5.85V. The detection of this failure mode can be disabled via Register 0x08.

Open Circuit Protection (OCP)

When one of the LEDs becomes open circuit, it can behave as either an infinite resistance or a gradually increasing finite resistance. The ISL97673 monitors the current in each channel such that any string which reaches the intended output current is considered "good". Should the current subsequently fall below the target, the channel will be considered an "open circuit". Furthermore, should the boost output of the ISL97673 reaches the OVP limit or should the lower over-temperature threshold be reached, all channels which are not "good" will immediately be considered as "open circuit". Detection of an "open circuit" channel will result in a time-out before disabling of the affected channel. This time-out is run when the device is above the lower over-temperature threshold in an attempt to prevent the upper over-temperature trip point from being reached.

Some users employ some special types of LEDs that have zener diode structure in parallel with the LED for ESD enhancement, thus enabling open circuit operation. When this type of LED goes open circuit, the effect is as if the LED forward voltage has increased, but no light is emitted. Any affected string will not be disabled, unless the failure results in the boost OVP limit being reached, allowing all other LEDs in the string to remain functional. Care should be taken in this case that the boost OVP limit and SCP limit are set properly, so as to make sure that multiple failures on one string do not cause all other good channels to be faulted out. This is due to the increased forward voltage of the faulty channel making all other channel look as if they have LED shorts. See Table 2 for details for responses to fault conditions.

Overvoltage Protection (OVP)

The integrated OVP circuit monitors the output voltage and keeps the voltage at a safe level. The OVP threshold is set as:

$$OVP = 1.21V \times (R_{UPPER} + R_{LOWER})/R_{LOWER} \quad \text{(EQ.12)}$$

These resistors should be large to minimize the power loss. For example, a 1MkΩ R_{UPPER} and 30kΩ R_{LOWER} sets OVP to 41.2V. Large OVP resistors also allow C_{OUT} discharges slowly during the PWM Off time. Parallel capacitors should also be placed across the OVP resistors such that $R_{UPPER}/R_{LOWER} = C_{LOWER}/C_{UPPER}$. Using a C_{UPPER} value of at least 30pF is recommended. These capacitors reduce the AC impedance of the OVP node, which is important when using high value resistors.

Undervoltage Lockout

If the input voltage falls below the UVLO level of 2.45V, the device will stop switching and be reset. Operation will restart only if the device is re-enabled through the SMBus/I^2C interface once the input voltage is back in the operating range. In non-SMBus/I^2C applications, the part will automatically restart once the input voltage clears the UVLO threshold with the part already enabled.

Input Overcurrent Protection

During normal switching operation, the current through the internal boost power FET is monitored. If the current exceeds the current limit, the internal switch will be turned off. This monitoring happens on a cycle by cycle basis in a self protecting way.

Additionally, the ISL97673 monitors the voltage at the LX and OVP pins. At startup, a fixed current is injected out of the LX pins and into the output capacitor. The device will not start up unless the voltage at LX exceeds 1.2V. The OVP pin is also monitored such that if it rises above and subsequently falls below 20% of the target OVP level, the input protection FET will be switched off.

Over-Temperature Protection (OTP)

The ISL97673 includes two over-temperature thresholds. The lower threshold is set to +130°C. When this threshold is reached, any channel which is outputting current at a level below the regulation target will be treated as "open circuit" and disabled after a time-out period. The intention of the lower threshold is to allow bad channels to be isolated and disabled before they cause enough power dissipation (as a result of other channels having large voltages across them) to hit the upper temperature threshold.

The upper threshold is set to +150°C. Each time this is reached, the boost will stop switching and the output current sources will be switched off. Hitting of the upper threshold will also set the thermal fault bit of the Fault/Status register 0x02. Unless disabled via the EN pin, the device stays in an active state throughout, allowing an external processor to interrogate the fault condition.

For the extensive fault protection conditions, please refer to Figure 24 and Table 2 for details.

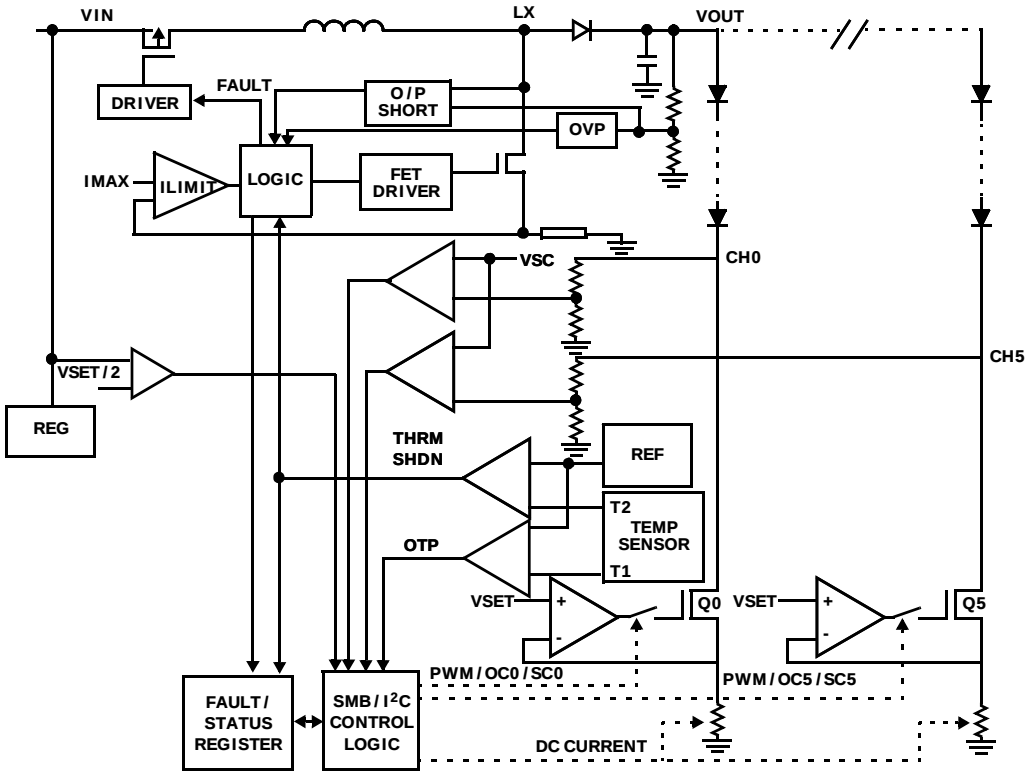


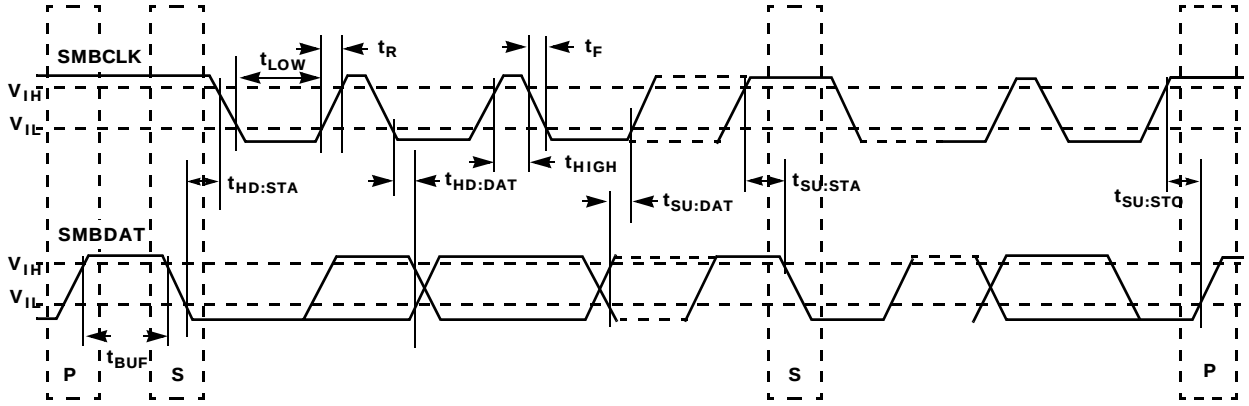
FIGURE 24. SIMPLIFIED FAULT PROTECTIONS

TABLE 2. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
1	CH0 Short Circuit	Upper Over-Temperature Protection limit (OTP) not triggered and CH0 < 4V	CH0 ON and burns power.	CH1 through CH5 Normal	Highest VF of CH1 through CH5
2	CH0 Short Circuit	Upper OTP triggered but VCH0 < 4V	All channels go off until chip cooled and then comes back on with current reduced to 76%. Subsequent OTP triggers will reduce I_{OUT} further.	Same as CH0	Highest VF of CH1 through CH5
3	CH0 Short Circuit	Upper OTP not triggered but CH0 > 4V	CH1 disabled after 6 PWM cycle time-out.	CH1 through CH5 Normal	Highest VF of CH1 through CH5
4	CH0 Open Circuit with infinite resistance	Upper OTP not triggered and CH0 < 4V	V_{OUT} will ramp to OVP. CH1 will time-out after 6 PWM cycles and switch off. V_{OUT} will drop to normal level.	CH1 through CH5 Normal	Highest VF of CH1 through CH5
5	CH0 LED Open Circuit but has paralleled Zener	Upper OTP not triggered and CH0 < 4V	CH1 remains ON and has highest VF, thus V_{OUT} increases.	CH1 through CH5 ON, Q1 through Q5 burn power	VF of CH0

TABLE 2. PROTECTIONS TABLE (Continued)

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
6	CH0 LED Open Circuit but has paralleled Zener	Upper OTP triggered but CH0 < 4V	All channels go off until chip cooled and then comes back on with current reduced to 76%. Subsequent OTP triggers will reduce I_{OUT} further	Same as CH0	VF of CH0
7	CH0 LED Open Circuit but has paralleled Zener	Upper OTP not triggered but CHx > 4V	CH0 remains ON and has highest VF, thus V_{OUT} increases.	V_{OUT} increases, then CH-X switches OFF after 6 PWM cycles. This is an unwanted shut off and can be prevented by setting OVP at an appropriate level.	VF of CH0
8	Channel-to-Channel ΔVF too high	Lower OTP triggered but CHx < 4V	Any channel at below the target current will fault out after 6 PWM cycles. Remaining channels driven with normal current.		Highest VF of CH0 through CH5
9	Channel-to-Channel ΔVF too high	Upper OTP triggered but CHx < 4V	All channels go off until chip cooled and then comes back on with current reduced to 76%. Subsequent OTP triggers will reduce I_{OUT} further		Highest VF of CH0 through CH5
10	Output LED stack voltage too high	V_{OUT} > VOVP	Any channel that is below the target current will time-out after 6 PWM cycles, and V_{OUT} will return to the normal regulation voltage required for other channels.		Highest VF of CH0 through CH5
11	V_{OUT}/LX shorted to GND at start-up or V_{OUT} shorted in operation	LX current and timing are monitored. OVP pins monitored for excursions below 20% of OVP threshold.	The chip is permanently shutdown 31mS after power-up if V_{OUT}/Lx is shorted to GND.		



NOTES:

SMBus/I²C Description

S = start condition

P = stop condition

A = acknowledge

$\overline{A}$ = not acknowledge

R/$\overline{W}$ = read enable at high; write enable at low

FIGURE 25. SMBus/I²C INTERFACE

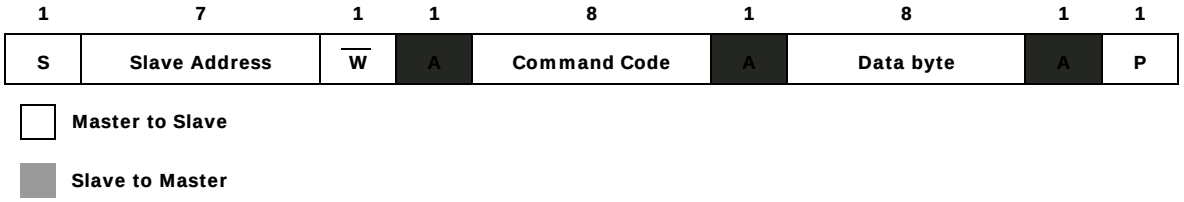


FIGURE 26. WRITE BYTE PROTOCOL

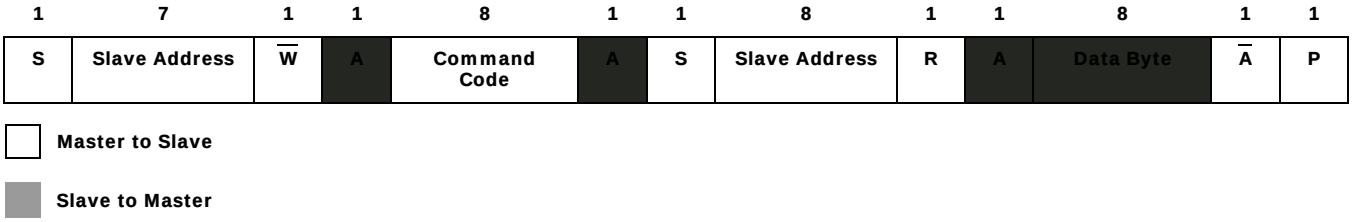


FIGURE 27. READ BYTE PROTOCOL

Write Byte

The Write Byte protocol is only three bytes long. The first byte starts with the slave address followed by the "command code," which translates to the "register index" being written. The third byte contains the data byte that must be written into the register selected by the "command code". A shaded label is used on cycles during which the slaved backlight controller "owns" or "drives" the Data line. All other cycles are driven by the "host master."

Read Byte

As shown in the Figure 27, the four byte long Read Byte protocol starts out with the slave address followed by the "command code" which translates to the "register index." Subsequently, the bus direction turns around with the re-broadcast of the slave address with bit 0 indicating a read ("R") cycle. The fourth byte contains the data being returned by the backlight controller. That byte value in the data byte reflects the value of the register being queried at the "command code" index. Note the bus directions, which are highlighted by the shaded label that is used on cycles during which the slaved backlight controller "owns" or "drives" the Data line. All other cycles are driven by the "host master."

Slave Device Address

The slave address contains 7 MSB plus one LSB as R/W bit, but these 8 bits are usually called Slave Address bytes. As shown in Figure 28, the high nibble of the Slave Address byte is 0x5 or 0101b to denote the "backlight controller class." Bit 3 in the lower nibble of the Slave Address byte is 1. Bit 0 is always the R/W bit, as specified by the SMBus/I^{2}C protocol. Note: In this document, the device address will always be expressed as a full 8-bit address instead of the shorter 7-bit address typically used in other backlight controller specifications to avoid confusion. Therefore, if the device is in the write mode where bit 0 is 0, the slave address byte is 0x58 or 01011000b. If the device is in the read mode where bit 0 is 1, the slave address byte is 0x59 or 01011001b.

The backlight controller may sense the state of the pins at POR or during normal operation. The pins will not change state while the device is in operation.

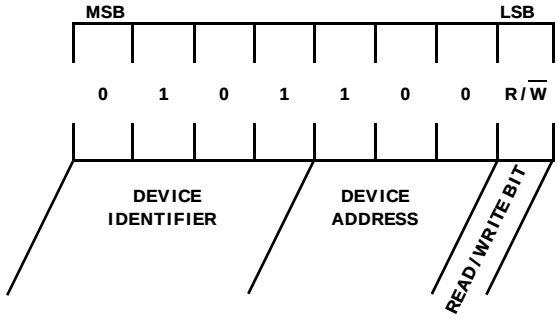


FIGURE 28. SLAVE ADDRESS BYTE DEFINITION

SMBus/I^{2}C Register Definitions

The backlight controller registers are Byte wide and accessible via the SMBus/I^{2}C Read/Write Byte protocols. Their bit assignments are provided in the following sections with reserved bits containing a default value of "0".

TABLE 3A. REGISTER LISTING

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DEFAULT VALUE	SMBus/I²C PROTOCOL
0x00	PWM Brightness Control Register	BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0	0xFF	Read and Write
0x01	Device Control Register	Reserved	Reserved	Reserved	Reserved	Reserved	PWM_MD	PWM_SEL	BL_CTL	0x00	Read and Write
0x02	Fault/Status Register	Reserved	Reserved	2_CH_SD	1_CH_SD	BL_STAT	OV_CURR	THRM_SHDN	FAULT	0x00	Read Only
0x03	Si Revision Register	1	1	0	0	1	REV2	REV1	REV0	0xC8	Read Only
0x07	DC Brightness Control Register	BRTDC7	BRTDC6	BRTDC5	BRTDC4	BRTDC3	BRTDC2	BRTDC1	BRTDC0	0xFF	Read and Write
0x08	Configuration Register	Reserved	DirectPWM	PWMtoDC	BstSlew Rate1	BstSlew Rate0	FSW	VSC1	VSC0	0x1F	Read and Write
0x09	Output Channel Register	Reserved	Reserved	CH5	CH4	CH3	CH2	CH1	CH0	0x3F	Read and Write
0x0A	Phase Shift Deg	Equal Phase	Phase Shift6	Phase Shift5	Phase Shift4	Phase Shift3	Phase Shift2	Phase Shift1	Phase Shift0	0x00	Read and Write

TABLE 3B. DATA BIT DESCRIPTIONS

ADDRESS	REGISTER	DATA BIT DESCRIPTIONS
0x00	PWM Brightness Control Register	BRT[7..0] = 256 steps of DPWM duty cycle brightness control
0x01	Device Control Register	PWM_MD = PWM mode select bit (1 = absolute brightness, 0 = % change), default = 0 PWM_SEL = Brightness control select bit (1 = control by PWMI, 0 = control by SMBus/I²C), default = 0 BL_CTL = BL On/Off (1 = On, 0 = Off), default = 0
0x02	Fault/Status Register	2_CH_SD = Two LED output channels are shutdown (1 = shutdown, 0 = OK) 1_CH_SD = One LED output channel is shutdown (1 = shutdown, 0 = OK) BL_STAT = BL status (1 = BL On, 0 = BL Off) OV_CURR = Input overcurrent (1 = Overcurrent condition, 0 = Current OK) THRM_SHDN = Thermal Shutdown (1 = Thermal fault, 0 = Thermal OK) FAULT = Fault occurred (Logic "OR" of all of the fault conditions)
0x03	Si Revision Register	REV[2..0] = Silicon rev (Rev 0 through Rev 7 allowed for silicon spins)
0x07	DC Brightness Control Register	BRTDC[7..0] = 256 steps of DC brightness control
0x08	Configuration Register	DirectPWM = Forces the PWM input signal to directly control the current sources. PWM-to-DC = Switches current sources on and varies DC level rather than PWMing. BstSlewRate = Controls strength of FET driver. 00 - 25% drive strength, 01 - 50% drive strength, 10 - 75% drive strength, 11 - 100% drive strength. FSW = Switching frequencies selection, FSW = 0 = 1.2MHz. FSW = 1 = 600kHz VSC[1..0] = Short circuit thresholds selection, 0 = disabled, 1 = 3.6V, 2 = 4.8V, 3 = 5.8V
0x09	Output Channel Select and Fault Readout Register	CH[5..0] = Output Channel Read and Write. In Write, 1 = Channel Enabled, 0 = Channel Disabled. In Read, 1 = Channel OK, 0 = Channel Shutdown or Disabled
0x0A	Phase Shift Degree	EqualPhase = Controls phase shift mode - When 0, phase shift is defined by PhaseShift<6:0>. When 1, phase shift is 360/N (where N is the number of channels enabled). PS[6..0] = 7-bit Phase shift setting - phase shift between each channel is PhaseShift<6:0>/(255*PWMFreq). In direct PWM modes, phase shift between each channel is PhaseShift<6:0>/12.8MHz. Note that user must not specify a value that gives >360° shift between first and last channels.

PWM Brightness Control Register (0x00)

The Brightness control resolution has 256 steps of PWM duty cycle adjustment. The bit assignment is shown in Figure 29. All of the bits in this Brightness Control Register can be read or write. Step 0 corresponds to the minimum step where the current is less than 10µA. Steps 1 to 255 represent the linear steps between 0.39% and 100% duty cycle with approximately 0.39% duty cycle adjustment per step.

- An SMBus/I^{2}C Write Byte cycle to Register 0x00 sets the PWM brightness level only if the backlight controller is in SMBus/I^{2}C mode (see Table 3A Operating Modes selected by Device Control Register Bits 1 and 2).
- An SMBus/I^{2}C Read Byte cycle to Register 0x00 returns the programmed PWM brightness level.
- An SMBus/I^{2}C setting of 0xFF for Register 0x00 sets the backlight controller to the maximum brightness.
- An SMBus/I^{2}C setting of 0x00 for Register 0x00 sets the backlight controller to the minimum brightness output.
- Default value for Register 0x00 is 0xFF.

REGISTER 0x00	PWM BRIGHTNESS CONTROL REGISTER

BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
BRT[7..0]	= 256 steps of PWM brightness levels

FIGURE 29. DESCRIPTIONS OF BRIGHTNESS CONTROL REGISTER

Device Control Register (0x01)

REGISTER 0x01	DEVICE CONTROL REGISTER

RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PWM_MD	PWM_SEL	BL_CTL
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

PWM_MD	PWM_SEL	BL_CTL	MODE
X	X	0	Backlight Off
0	0	1	SMBus/I^{2}C and PWM dimming (DPST)
0	1	1	PWMI controlled PWM dimming
1	0	1	SMBus/I^{2}C controlled PWM dimming
1	1	1	Backlight On but stays with previous mode selection

FIGURE 30. DESCRIPTIONS OF DEVICE CONTROL REGISTER

This register has two bits that control either SMBus/I^{2}C controlled or external PWM controlled PWM dimming and a single bit that controls the BL ON/OFF state. The remaining bits are reserved. The bit assignment is shown in Figure 30. All other bits in the Device Control Register will read as low unless otherwise written.

- All defined control bits return their current, latched value when read.

A value of 1 written to BL_CTL turns on the BL in 4ms or less after the write cycle completes. The BL is

- deemed to be on when Bit 3 BL_STAT of Register 0x02 is 1 and Register 0x09 is not 0.
- A value of 0 written to BL_CTL immediately turns off the BL. The BL is deemed to be off when Bit 3 BL_STAT of Register 0x02 is 0 and Register 0x09 is 0.
- When SMBus/I^{2}C mode with DPST is selected, Register 0x00 reflects the last value written to it from SMBus/I^{2}C.
- The default value for Register 0x01 is 0x00.

Fault/Status Register (0x02)

This register has 6 status bits that allow monitoring of the backlight controller's operating state. Bit 0 is a logical "OR" of all fault codes to simplify error detection. Not all of the bits in this register are fault related (Bit 3 is a simple BL status indicator). The remaining bits are reserved and return a "0" when read. All of the bits in this register are read-only, with the exception of Bit 0, which can be cleared by writing to it.

- A Read Byte cycle to Register 0x02 indicates the current BL on/off status in BL_STAT (1 if the BL is on, 0 if the BL is off).
- A Read Byte cycles to Register 0x2 also returns FAULT as the logical OR of THRM_SHDN, OV_CURR, 2_CH_SD, and 1_CH_SD should these events occur.
- 1_CH_SD returns a 1 if one or more channels have faulted out.
- 2_CH_SD returns a 1 if two or more channels have faulted out.
- A fault will not be reported in the event that the BL is commanded on and then immediately off by the system.
- When FAULT is set to 1, it will remain at 1 even if the signal which sets it goes away. FAULT will be cleared when the BL_CTL bit of the Device Control Register is toggled or when written low. At that time, if the fault condition is still present or reoccurs, FAULT will be set to 1 again. BL_STAT will not cause FAULT to be set.
- The default value for Register 0x02 is 0x00.

Si Revision Register (0x03)

The Si Revision register has 3 bits that allows up to 8 silicon revisions each. In order to keep the number of silicon revisions low, the revision field will not be updated unless the part will make it out to the user's factory. Thus, if during the first silicon engineering development process, 2 silicon spins were needed, the revision remains as 0. All of the bits in this register are read-only.

- The default value for Register 0x03 is 0xC8.

The initial value of REV shall be 0. Subsequent values of REV will increment by 1.

REGISTER 0x02	FAULT/STATUS REGISTER

RESERVED	RESERVED	2_CH_SD	1_CH_SD	BL_STAT	OV_CURR	THRM_SHDN	FAULT
Bit 7 (R)	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

BIT	BIT ASSIGNMENT	BIT FIELD DEFINITIONS
Bit 5	2_CH_SD	= Two LED output channels are shutdown (1 = shutdown, 0 = OK)
Bit 4	1_CH_SD	= One LED output channel is shutdown (1 = shutdown, 0 = OK)
Bit 3	BL_STAT	= BL Status (1 = BL On, 0 = BL Off)
Bit 2	OV_CURR	= Input Overcurrent (1 = Overcurrent condition, 0 = Current OK)
Bit 1	THRM_SHDN	= Thermal Shutdown (1 = Thermal Fault, 0 = Thermal OK)
Bit 0	FAULT	= Fault occurred (Logic "OR" of all of the fault conditions)

FIGURE 31. DESCRIPTIONS OF FAULT/STATUS REGISTER

REGISTER 0x03	ID REGISTER

LED PANEL	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0
Bit 7 = 1	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
MFG[3..0]	= Manufacturer ID. See "Si Revision Register (0x03)" on page 21. data 0 to 8 in decimal correspond to other vendors data 9 in decimal represents Intersil ID data 10 to 14 in decimal are reserved data 15 in decimal Manufacturer ID is not implemented
REV[2..0]	= Silicon rev (Rev 0 through Rev 7 allowed for silicon spins)

FIGURE 32. DESCRIPTIONS OF ID REGISTER

DC Brightness Control Register (0x07)

REGISTER 0x07	DC BRIGHTNESS CONTROL REGISTER

BRTDC7	BRTDC6	BRTDC5	BRTDC4	BRTDC3	BRTDC2	BRTDC1	BRTDC0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
BRTDC[7..0]	= 256 steps of DC brightness levels

FIGURE 33. DESCRIPTIONS OF DC BRIGHTNESS CONTROL REGISTER

The DC Brightness Control Register 0x07 allows users to have additional dimming flexibility by:

1. Effectively achieving 16-bits of dimming control when DC dimming is combined with PWM dimming.
2. Achieving visual or audio noise free 8-bit DC dimming over potentially noisy PWM dimming.

The bit assignment is shown in Figure 33. All of the bits in this Register can be read or write. Steps 0 to 255 represent the linear steps of current adjustment in DC on the fly. It can also be considered as the peak current factory calibration feature to account for various LED production batch variations, but external EEPROM settings storing and restoring are required.

- An SMBus/I^{2}C Write Byte cycle to Register 0x07 sets the brightness level in DC only.
- An SMBus/I^{2}C Read Byte cycle to Register 0x07 returns the current DC brightness level.
- Default value for Register 0x07 is 0xFF.

Configuration Register (0x08)

The Configuration Register provides many extra functions that users can explore in order to optimize the driver performance at a given application.

A Direct PWM bit allows Direct PWM where the output current follows the same input PWM signal.

A PWM-to-DC bit allows users to provide convert PWM input into average DC LED current output with the level that is proportional to the input PWM duty cycle.

A BstSlewRate bit allows users to control the boost FET slew rate (the rates of turn-on and turn-off). The slew rate can be selected to four relative strengths when driving the internal boost FET. The purpose of this function is to allow users to experiment the slew rate with respect to EMI effect in the system. In general, the slower the slew rate is, the lower the EMI interference to the surrounding circuits; however, the switching loss of the boost FET is also increased.

The FSW bit allows users to set the boost conversion switching frequency between 1.2MHz and 600kHz.

The Vsc bits allow users to set 3 levels of channel short-circuit thresholds or disable it.

The bit assignment is shown in Figure 34. The default value for Register 0x08 is 0x1F.

Output Channel Select and Fault Readout Register (0x09)

This register can be read or write; the bit position corresponds to the channel. For example, Bit 0 corresponds to CH0 and Bit 4 corresponds to CH4 and so on. Writing data to this register, it enables the channels of interest. When reading data from this register, any disabled channel and any faulted out channel will read as 0. This allows the user to determine which channel is faulty and optionally not enabling it in order to allow the rest of the system to continue to function. Additionally, a faulted out channel can be disabled and re-enabled in order to allow a retry for any faulty channel without having to power-down the other channels.

The bit assignment is shown in Figure 35. The default for Register 0x09 is 0x3F.

REGISTER 0x08	CONFIGURATION REGISTER

RESERVED	DIRECT PWM	PWM-TO-DC	BSTSLEWRATE1	BSTSLEWRATE0	FSW	VSC1	VSC0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
DirectPWM	Forces the PWMI signal to directly control the current sources. Note that there is some synchronous delay between PWMI and current sources.
PWM-to-DC	Switches current sources on and varies DC level rather than PWMing.
BstSlewRate[1:0]	Controls strength of FET driver. 00 - 25% drive strength, 01 to 50% drive strength, 10 -75% drive strength, 11 to 100% drive strength.
FSW	2 levels of Switching Frequencies (0 = 1,200kHz, 1 = 600kHz)
VSC[1..0]	3 levels of Short-Circuit Thresholds (0 = disabled, 1 = 3.6V, 2 = 4.8V, 3 = 5.8V)

FIGURE 34. DESCRIPTIONS OF CONFIGURATION REGISTER

REGISTER 0x09	OUTPUT CHANNEL REGISTER

Reserved	Reserved	CH5	CH4	CH3	CH2	CH1	CH0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
CH[5..0]	CH5 = Channel 5, CH4 = Channel 4 and so on

FIGURE 35. DESCRIPTIONS OF OUTPUT CHANNEL REGISTER

REGISTER 0x0A	PHASE SHIFT CONTROL REGISTER

EQUAL PHASE	PHASE-SHIFT6	PHASE-SHIFT5	PHASE-SHIFT4	PHASE-SHIFT3	PHASE-SHIFT2	PHASE-SHIFT1	PHASE-SHIFT0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
EqualPhase	Controls phase shift mode - When 0, phase shift is defined by PhaseShift<6:0>. When 1, phase shift is 360/N (where N is the number of channels enabled).
PhaseShift[6..0]	7-bit Phase shift setting - phase shift between each channel is PhaseShift<6:0>/(255*PWMFreq) In direct PWM modes, phase shift between each channel is PhaseShift<6:0>/12.8MHz Note that user must not specify a value that gives >360° shift between first and last channels.

FIGURE 36. DESCRIPTIONS OF PHASE SHIFT CONTROL REGISTER

Phase Shift Control Register (0x0A)

The Phase Shift Control register is used to set phase delay between each channels. When bit 7 is set high, the phase delay is set by the number of channels enabled and the PWM frequency. The delay time is defined by the Equation 13:

$$t_{DELAY} = (t_{FPWM}/N) \quad \text{(EQ. 13)}$$

where N is the number of channels enabled, and t_{FPWM} is the period of the PWM cycle. When bit 7 is set low, the phase delay is set by bits 6 to 0 and the PWM frequency. The delay time is defined by Equation 14:

$$t_{DELAY} = (PS<6,0> x t_{FPWM}/(255)) \quad \text{(EQ. 14)}$$

where PS is an integer from 0 to 127, and t_{FPWM} is the period of the PWM cycle. By default, all the register bits are set low, which sets zero delay between each channel. Note that the user should not program the register to give more than one period of the PWM cycle delay between the first and last enabled channels.

Components Selections

According to the inductor Voltage-Second Balance principle, the change of inductor current during the switching regulator On time is equal to the change of inductor current during the switching regulator Off time. Since the voltage across an inductor is:

$$V_L = L \times \Delta I_L/\Delta t \quad \text{(EQ. 15)}$$

and ΔI_L @ On = ΔI_L @ Off, therefore:

$$(V_I - 0)/L \times D \times t_S = (V_O - V_D - V_I)/L \times (1-D) \times t_S \quad \text{(EQ. 16)}$$

where D is the switching duty cycle defined by the turn-on time over the switching period. V_D is Schottky diode forward voltage that can be neglected for approximation. Rearranging the terms without accounting for V_D gives the boost ratio and duty cycle respectively as:

$$V_O/V_I = 1/(1-D) \quad \text{(EQ. 17)}$$

$$D = (V_O - V_I)/V_O \quad \text{(EQ. 18)}$$

Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. This reduces interaction between the regulator and input supply, thereby improving system stability. The high switching frequency of the loop causes almost all ripple current to flow in the input capacitor, which must be rated accordingly.

A capacitor with low internal series resistance should be chosen to minimize heating effects and improve system efficiency, such as X5R or X7R ceramic capacitors, which offer small size and a lower value of temperature and voltage coefficient compared to other ceramic capacitors.

In Boost mode, input current flows continuously into the inductor; AC ripple component is only proportional to the rate of the inductor charging, thus, smaller value input capacitors may be used. It is recommended that an input capacitor of at least 10µF be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.

Inductor

The selection of the inductor should be based on its maximum current (I_{SAT}) characteristics, power dissipation (DCR), EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters, including ripple current, current limit, efficiency, transient performance and stability.

The inductor's maximum current capability must be adequate enough to handle the peak current at the worst case condition. If an inductor core is chosen with too low

a current rating, saturation in the core will cause the effective inductor value to fall, leading to an increase in peak to average current level, poor efficiency and overheating in the core. The series resistance, DCR, within the inductor causes conduction loss and heat dissipation. A shielded inductor is usually more suitable for EMI susceptible applications, such as LED backlighting.

The peak current can be derived from the voltage across the inductor during the Off period, as expressed in Equation 19:

$$IL_{pk} = (V_O \times I_O)/(85\% \times V_I) + 1/2[V_I \times (V_O - V_I)/(L \times V_O \times f_{SW})] \quad \text{(EQ. 19)}$$

The choice of 85% is just an average term for the efficiency approximation. The first term is the average current, which is inversely proportional to the input voltage. The second term is the inductor current change, which is inversely proportional to L and f_{SW}. As a result, for a given switching frequency and minimum input voltage on which the system operates, the inductor I_{SAT} must be chosen carefully. At a given inductor size, usually the larger the inductance, the higher the series resistance because of the extra winding of the coil. Thus, the higher the inductance, the lower the peak current capability. The ISL97673 current limit should also have to be taken into account.

Output Capacitors

The output capacitor acts to smooth the output voltage and supplies load current directly during the conduction phase of the power switch. Output ripple voltage consists of the discharge of the output capacitor for I_{LPEAK} during FET On and the voltage drop due to flowing through the ESR of the output capacitor. The ripple voltage can be shown as Equation 20:

$$\Delta V_{CO} = (I_O/C_O \times D/f_S) + ((I_O \times ESR) \quad \text{(EQ. 20)}$$

The conservation of charge principle in Equation 20 also brings up the fact that during the boost switch Off period, the output capacitor is charged with the inductor ripple current minus a relatively small output current in boost topology. As a result, the user needs to select an output capacitor with low ESR and enough input ripple current capability.

The choice of X7R over Y5V ceramic capacitor is highly recommend because X7R capacitor is less sensitive to capacitance change over voltage but the Y5V capacitor exhibits very high capacitance coefficient such that its absolute capacitance can be reduced to 10~20% to the rated capacitance at maximum voltage.

Output Ripple

ΔV_{Co}, can be reduced by increasing Co or f_{SW}, or using small ESR capacitors. In general, Ceramic capacitors are the best choice for output capacitors in small to medium sized LCD backlight applications due to their cost, form factor, and low ESR.

A larger output capacitor will also ease the driver response during PWM dimming Off period due to the longer sample and hold effect of the output drooping. The driver does not need to boost harder in the next On period that minimizes transient current. The output capacitor is also needed for compensation, and, in general one to two 4.7µF/50V ceramic capacitors are suitable for netbook to notebook display backlight applications.

Schottky Diode

A high-speed rectifier diode is necessary to prevent excessive voltage overshoot, especially in the boost configuration. Low forward voltage and reverse leakage current will minimize losses, making Schottky diodes the preferred choice. Although the Schottky diode turns on only during the boost switch Off period, it carries the same peak current as the inductor, and therefore, a suitable current rated Schottky diode must be used.

Applications

High Current Applications

Each channel of the ISL97673 can support up to 30mA. For applications that need higher current, multiple channels can be grouped to achieve the desirable current. For example, the cathode of the last LED can be connected to CH0 to CH2, this configuration can be treated as a single string with 90mA current driving capability.

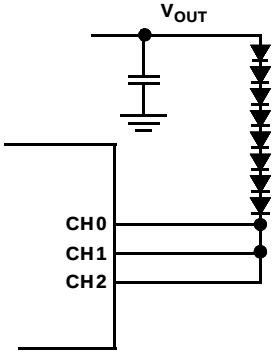


FIGURE 37. GROUPING MULTIPLE CHANNELS FOR HIGH CURRENT APPLICATIONS

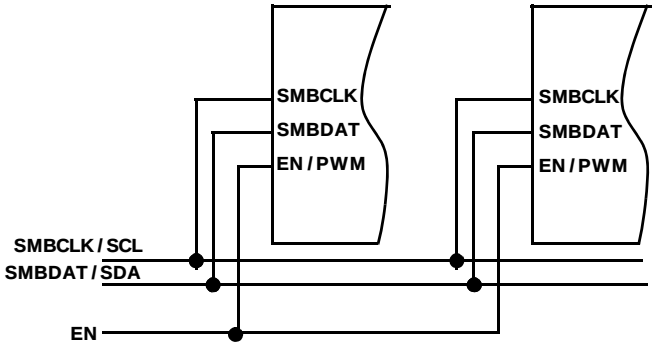


FIGURE 38. MULTIPLE DRIVERS OPERATION

Multiple Drivers Operation

For large LCD panels where more than 6 channels of LEDs are needed, multiple ISL97673s with each driver having its own supporting components can be controlled together with the common SMBus/I^{2}C. While the ISL97673 does not have extra pins strappable slave address feature, but a separate EN signal can be applied to each driver for asynchronous operation. A trade-off of such scheme is that an exact faulty channel cannot be identified since both ICs have the same I2C slave address.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
August 1, 2012	FN7633.2	On page 12, changed 401.8 to 410.5 in Equations 2 and 4.
July 18, 2012	FN7633.1	Stamped page 1 “Not Recommended for New Designs”
June 24, 2010	FN7633.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ISL97673

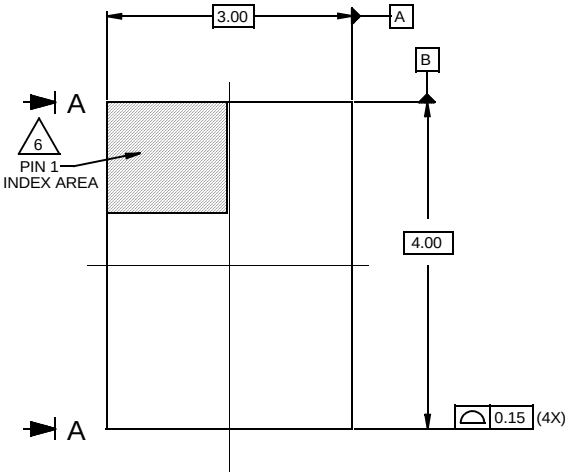
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

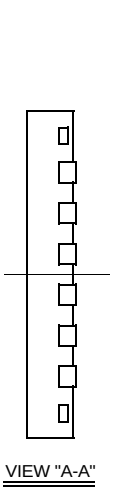
Package Outline Drawing

L20.3x4

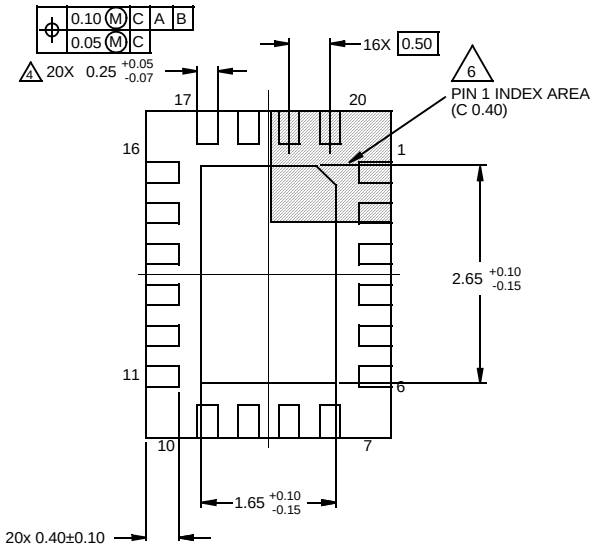
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 3/10



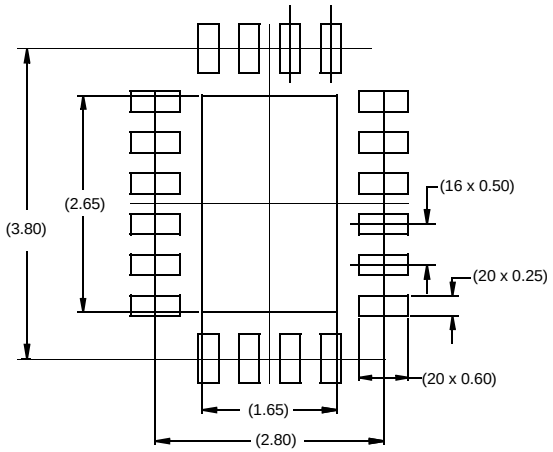
TOP VIEW



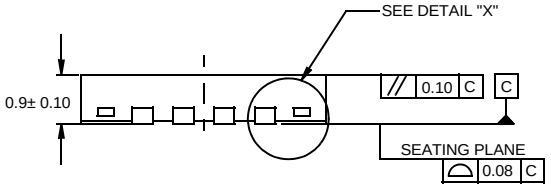
VIEW "A-A"



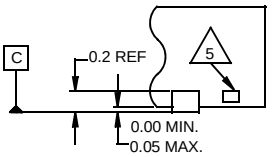
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.