



BT139B-800E

4Q Triac

27 September 2013

Product data sheet

1. General description

Planar passivated sensitive gate four quadrant triac in a SOT404 (D2PAK) surface-mountable plastic package intended for use in general purpose bidirectional switching and phase control applications. This sensitive gate "series E" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Direct triggering from low power drivers and logic ICs
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate
- Surface-mountable package
- Triggering in all four quadrants

3. Applications

- General purpose phase control
- General purpose switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 20 \text{ ms}$; Fig. 4 ; Fig. 5		-	-	155	A
$I_T(\text{RMS})$	RMS on-state current	full sine wave; $T_{mb} \leq 99^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3		-	-	16	A
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2+ G+; $T_j = 25^\circ\text{C}$; Fig. 7		-	2.5	10	mA
		$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2+ G-; $T_j = 25^\circ\text{C}$; Fig. 7		-	4	10	mA



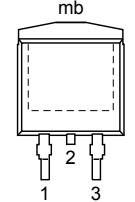
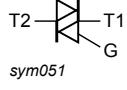
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2- G-; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 7		-	5	10	mA
		$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2- G+; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 7		-	11	25	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2	 D2PAK (SOT404)	

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT139B-800E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 99$ °C; Fig. 1 ; Fig. 2 ; Fig. 3		-	16	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4 ; Fig. 5		-	155	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	170	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		-	120	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/ μ s; T2+ G+		-	50	A/μ s
		$I_T = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/ μ s; T2+ G-		-	50	A/μ s
		$I_T = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/ μ s; T2- G-		-	50	A/μ s
		$I_T = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/ μ s; T2- G+		-	10	A/μ s
I_{GM}	peak gate current			-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C

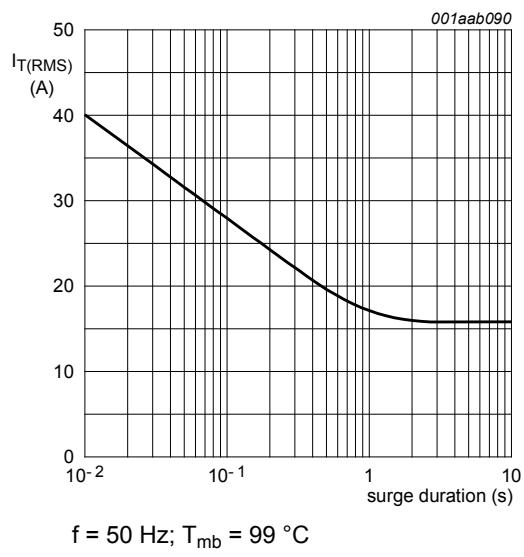


Fig. 1. RMS on-state current as a function of surge duration; maximum values

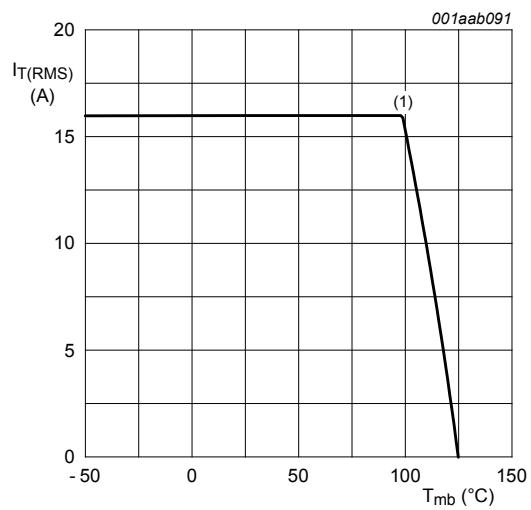


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values

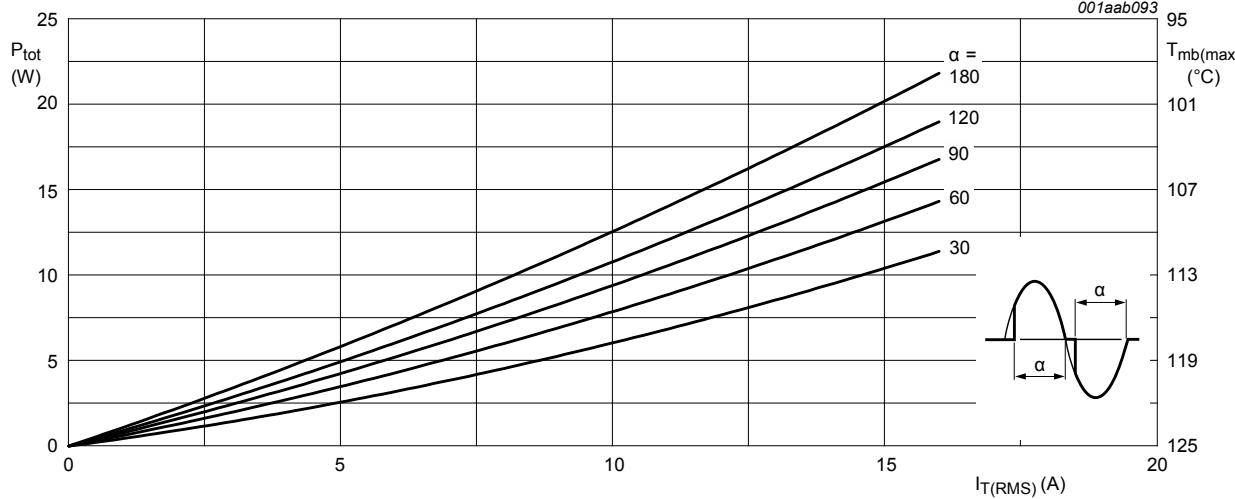
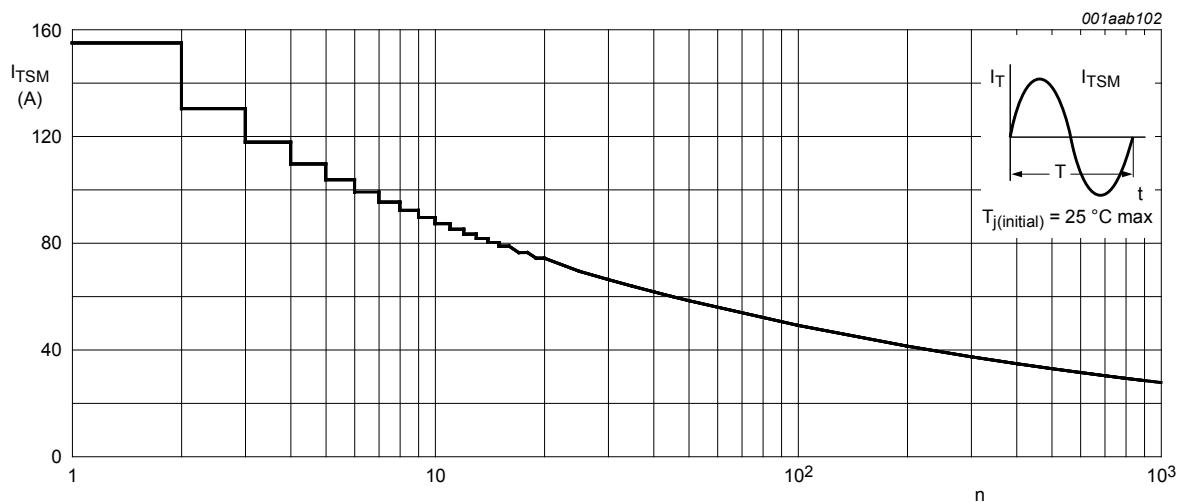
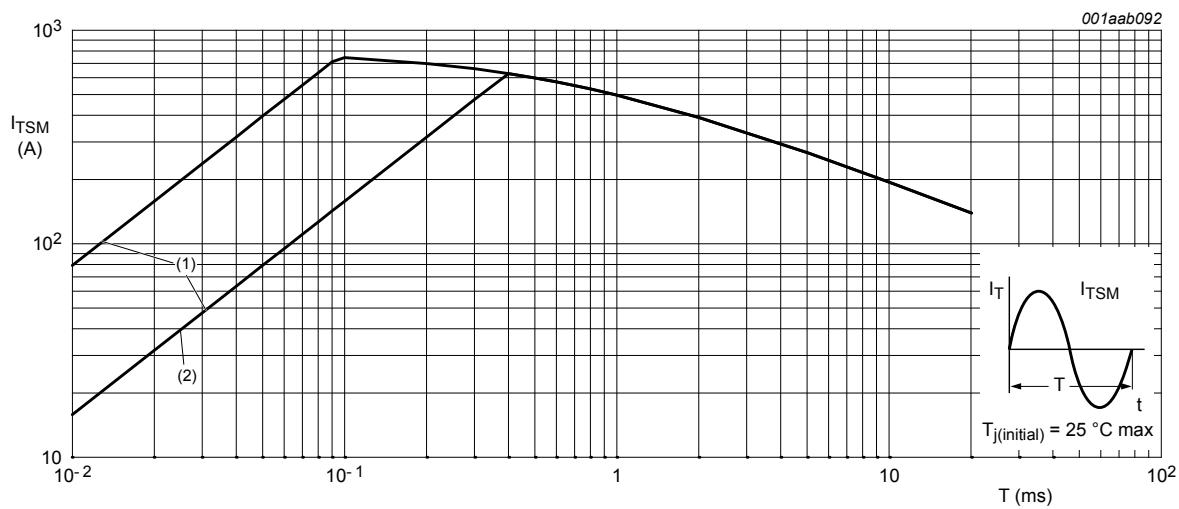


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values.



$f = 50$ Hz; n = number of cycles

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dl_T/dt limit

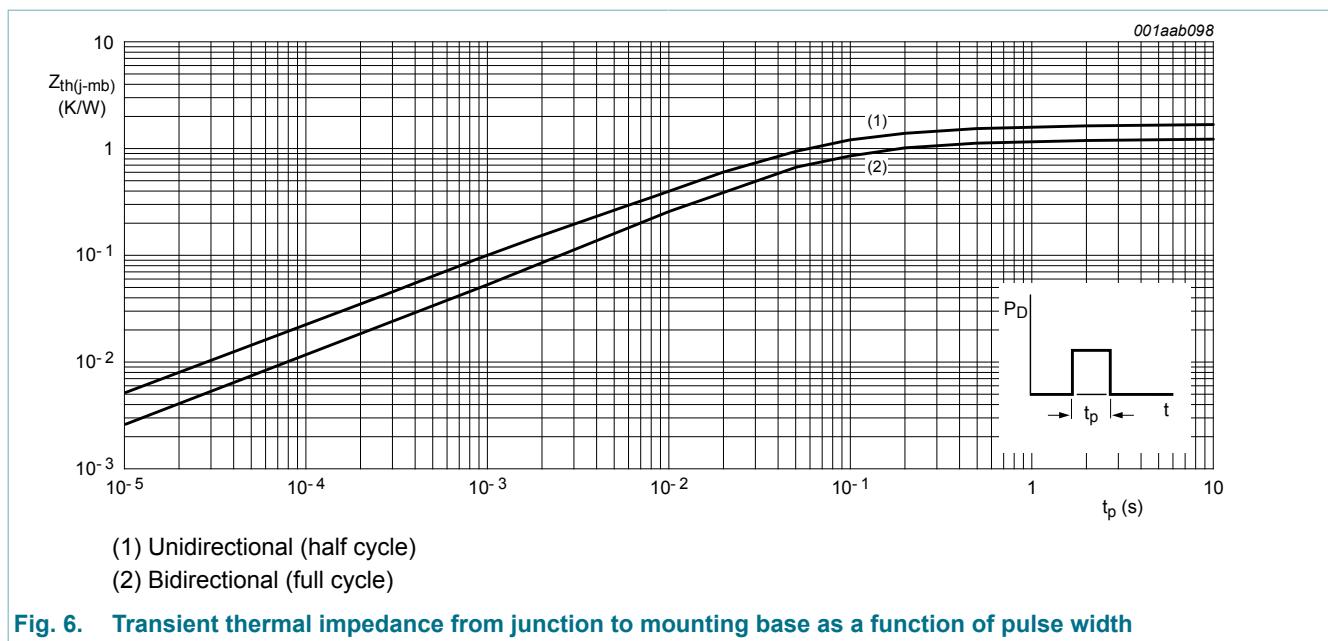
(2) T2- G+ quadrant limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	half cycle; Fig. 6	-	-	1.7	K/W
		full cycle; Fig. 6	-	-	1.2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; FR4 board	-	55	-	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 7		-	2.5	10	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 7		-	4	10	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 7		-	5	10	mA
		V _D = 12 V; I _T = 0.1 A; T2- G+; T _j = 25 °C; Fig. 7		-	11	25	mA
I _L	latching current	V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 8		-	3.2	30	mA
		V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 8		-	16	40	mA
		V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; Fig. 8		-	4	30	mA
		V _D = 12 V; I _G = 0.1 A; T2- G+; T _j = 25 °C; Fig. 8		-	5.5	40	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 9		-	4	45	mA
V _T	on-state voltage	I _T = 20 A; T _j = 25 °C; Fig. 10		-	1.2	1.6	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11		-	0.7	1	V
		V _D = 400 V; I _T = 0.1 A; T _j = 125 °C; Fig. 11		0.25	0.4	-	V
I _D	off-state current	V _D = 800 V; T _j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit		-	50	-	V/μs
t _{gt}	gate-controlled turn-on time	I _{TM} = 20 A; V _D = 800 V; I _G = 0.1 A; dI _G /dt = 5 A/μs		-	2	-	μs

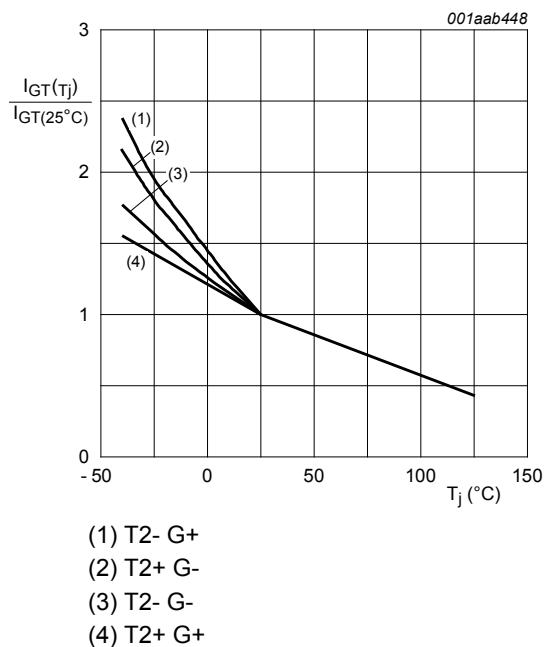


Fig. 7. Normalized gate trigger current as a function of junction temperature

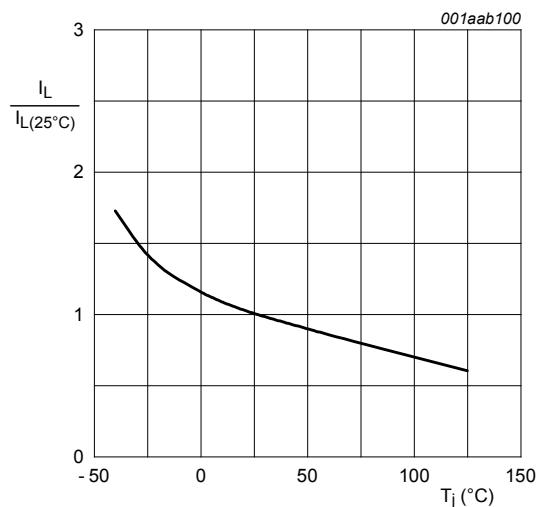


Fig. 8. Normalized latching current as a function of junction temperature

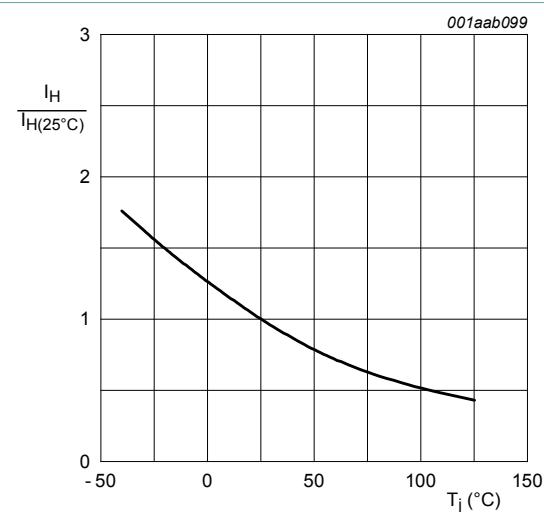


Fig. 9. Normalized holding current as a function of junction temperature

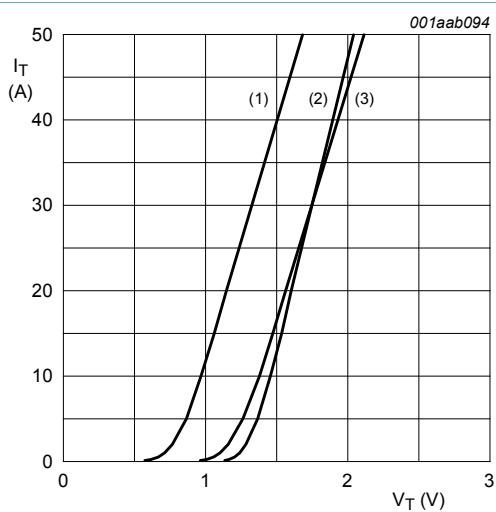


Fig. 10. On-state current as a function of on-state voltage

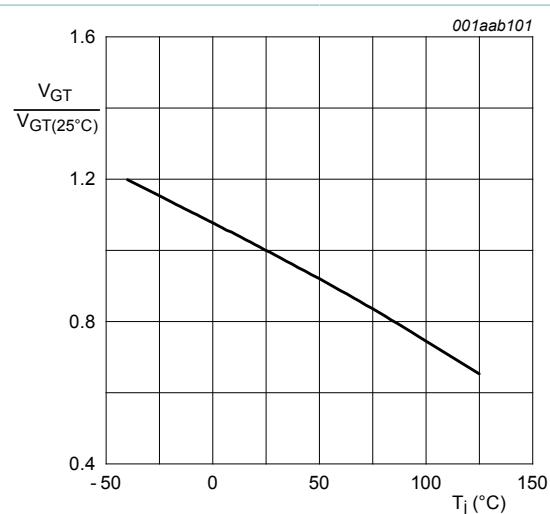


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

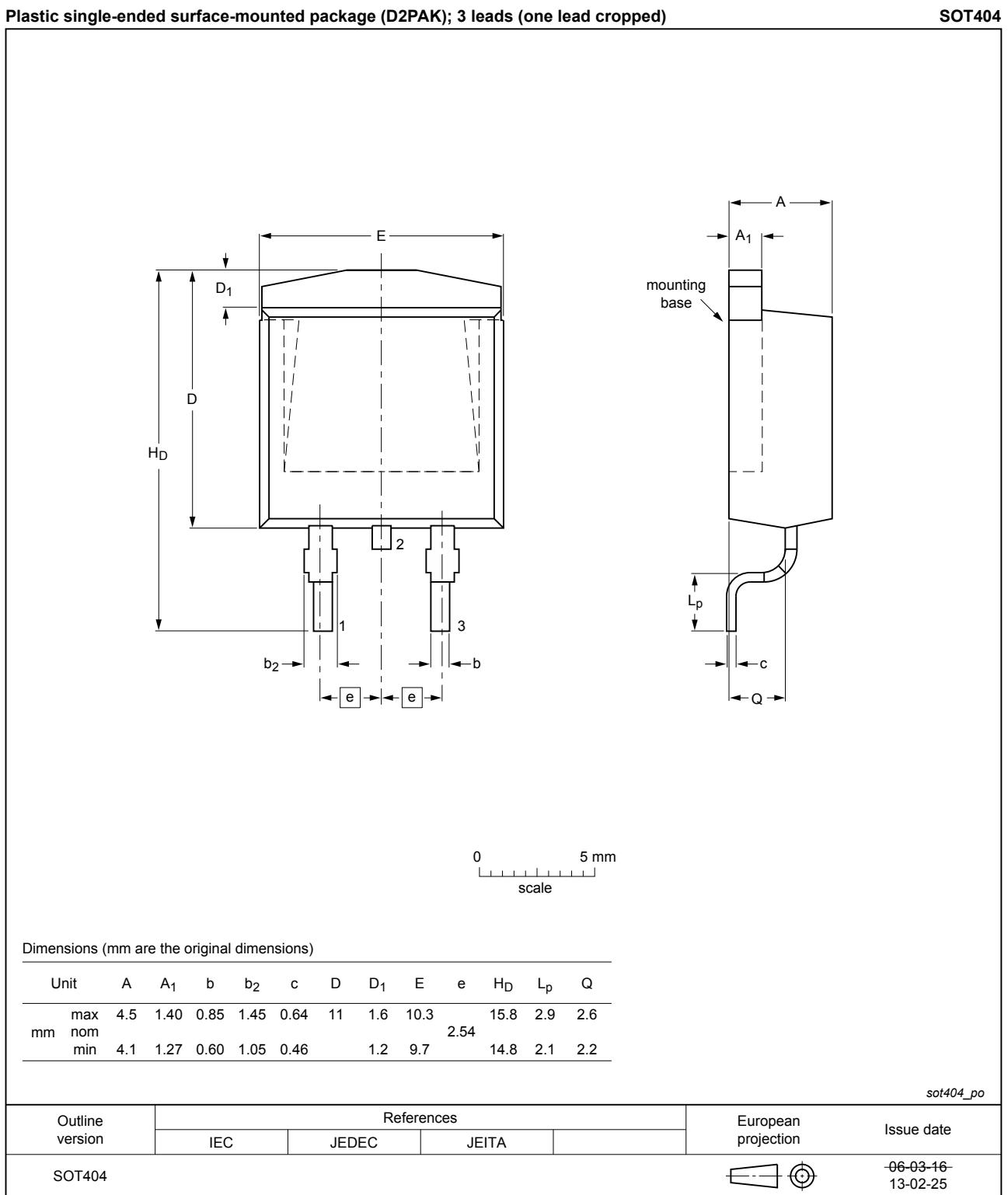


Fig. 12. Package outline D2PAK (SOT404)

11. Soldering

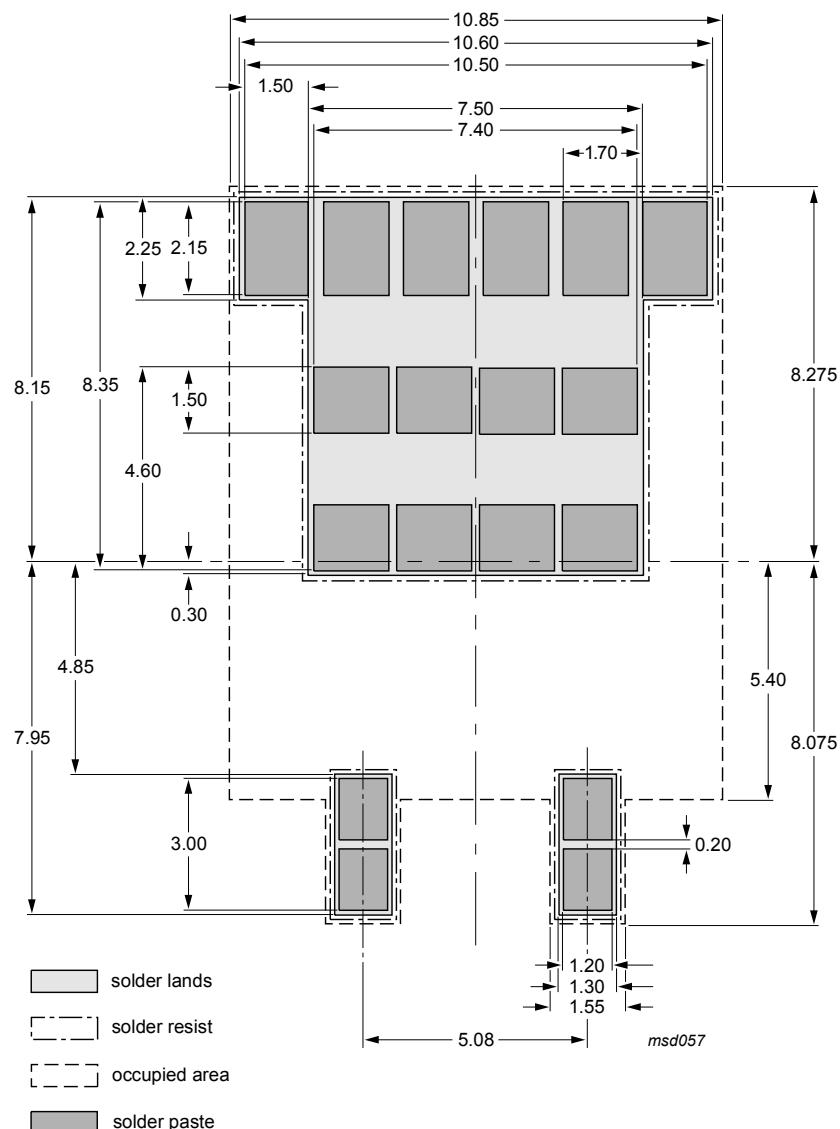


Fig. 13. Reflow soldering footprint for D2PAK (SOT404)

12. Legal information

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Date of release: 27 September 2013

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