

CYPRESS  
SEMICONDUCTORT. 46-13-29  
PRELIMINARYCY7C258  
CY7C2592K x 16 Reprogrammable  
State Machine PROM

## Features

- High speed: 83-MHz operation
  - $t_{CP} = 12$  ns
  - $t_{CKO} = 9$  ns
  - $t_{AS} = 3$  ns
- 16-bit-wide state word
- Optimum speed/ power
- Individually bypassable input and output registers
- Individually programmable address/feedback muxes
- Synchronous and asynchronous chip select
- Synchronous and asynchronous **INIT** and programmable initialize word
- 16 outputs (CY7C259)
- Software support
- CY7C258 available in 28-pin, 300-mil plastic and ceramic DIP, LCC, PLCC
- CY7C259 available in 44-pin LCC and PLCC
- Reprogrammable in windowed packages
- Capable of withstanding greater than 2001V static discharge

## Functional Description

The CY7C258 and CY7C259 are 2K x 16 CMOS PROMS specifically designed for use in state machine applications.

State machines are one of the most common applications for registered PROMs. The CY7C258 and CY7C259 feature internal state feedback and a variety of programmable features to support 83-MHz state machines with as many as 2,048 distinct states.

It is easy to use a PROM as a state machine. Each array location contains output data as well as information fed back to select the next state. Note that a PROM is only limited by the number of array inputs. If a given state machine can be implemented in the number of inputs/feedbacks available (11 on the CY7C258/259), then it will always fit in the device. No software minimization is required.

Among the programmable features of the CY7C258/CY7C259 are individually bypassable input and output registers. The registers run off the same clock for pipeline capability. Each individual register can be programmed to capture data at the rising edge of the clock or to be transparent.

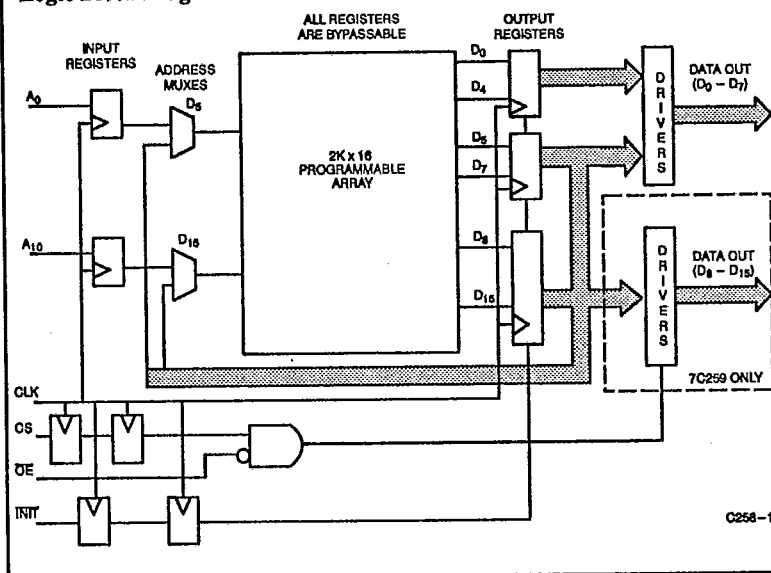
The registers at the inputs are useful for signals that require short set-up times ( $t_{AS} = 3$  ns). The input register does introduce a cycle of latency, however. For signals that directly affect the next state of the machine, each input register can be bypassed. Note that the cycle time remains the same (12-ns min.), even if the inputs are bypassed.

Registers at the output are used to hold both state information and output data. These registers are also bypassable for maximum flexibility. Occasionally, an individual output cannot wait for the next clock edge. These outputs are sometimes called Mealy outputs, and can be created by bypassing the appropriate output register.

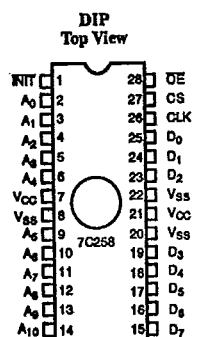
Since the CY7C258 and CY7C259 contain a 2K array, they each require 11 inputs. Each of these inputs can come from an input pin or from internal output register feedback. Eleven individually programmable address muxes allow the user to select the ratio of pin input and state feedback.

These devices have both an asynchronous output (OE) and a synchronous chip select (CS). The CS input is polarity

## Logic Block Diagram



## Pin Configurations



C258-2

C258-1



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### Functional Description (continued)

programmable and registered twice. Each of the CS registers can be bypassed in the same manner as the address input and output registers.

A separately controllable INIT input is included for user resets. If INIT is sampled LOW on the rising edge of CLK, the user programmable initialization word will appear at the outputs after the next CLK cycle. Each of the INIT registers can be bypassed in the same manner as the address input and output registers.

The difference between the CY7C258 and CY7C259 is in the packaging. The CY7C258 has three different types of outputs. D<sub>4</sub> - D<sub>0</sub> are dedicated outputs that do not feed back to the input registers. D<sub>5</sub> - D<sub>7</sub> appear on the outputs and are fed back to the input muxes. Finally, D<sub>8</sub> - D<sub>15</sub> are dedicated feedback lines that do not appear at the external outputs. The dedicated feedback allows the CY7C258 to be packaged in 28-pin packages. The CY7C259 is available in 28-pin LCC, PLCC, and slim 300-mil DIP packages.

On the CY7C259, all 16 array outputs are available at the pins. Outputs D<sub>4</sub> - D<sub>0</sub> remain as dedicated outputs while D<sub>5</sub> - D<sub>15</sub> appear at the pins and are also fed back to the input muxes. This organization allows the user maximum flexibility in selecting the ratio of outputs to state feedback. The availability of state information at pins also improves testability. The CY7C259 is packaged in 44-pin LCC and PLCC packages.

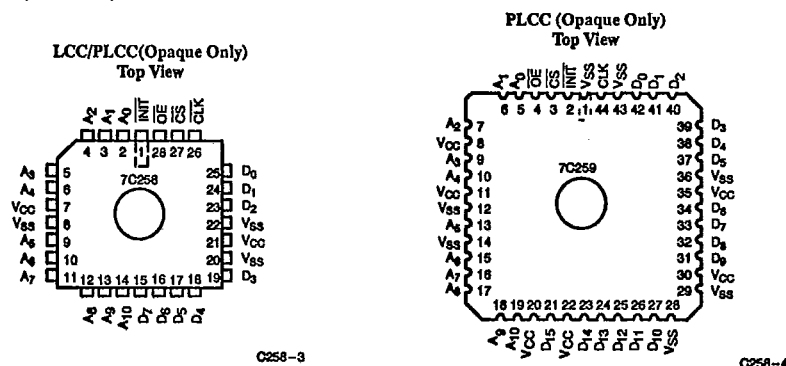
To make it easier to use the CY7C258 and CY7C259, the devices are supported in the Cypress PLD Toolkit, including the waveform simulator. Several third-party programmers also feature support for PROMs as state machines, including Data I/O (ABEL) and ISDATA (LOG/IC).

The CY7C258 and CY7C259 offer the advantage of low power, superior performance, and programming yield. The EPROM cells allow for each memory location to be 100% tested, with each location being written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.



PROMS

### Pin Configurations (continued)



### Selection Guide

|                                             | Commercial |            |            | Military   |            |             | Units |
|---------------------------------------------|------------|------------|------------|------------|------------|-------------|-------|
|                                             | 12 ns      | 15 ns      | 18 ns      | 15 ns      | 18 ns      | 25 ns       |       |
| Minimum Cycle Time                          | 12         | 15         | 18         | 15         | 18         | 25          | ns    |
| Registered Input Set-Up/Hold <sup>[1]</sup> | 3/3 or 7/0 | 4/4 or 8/1 | 5/5 or 9/2 | 4/4 or 8/1 | 5/5 or 9/2 | 6/6 or 10/3 | ns    |
| Bypassed Input Set-Up/Hold                  | 12/0       | 15/0       | 18/0       | 15/0       | 18/0       | 25/0        | ns    |
| Clock-to-Output                             | 9          | 11         | 13         | 11         | 13         | 15          | ns    |
| Maximum Operating Current                   | 175        | 175        | 175        | 200        | 200        | 200         | mA    |

Shaded area contains advanced information.

Notes:

1. This parameter is programmable.

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**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

|                                                                |                  |
|----------------------------------------------------------------|------------------|
| Storage Temperature .....                                      | - 65°C to +150°C |
| Ambient Temperature with<br>Power Applied .....                | - 55°C to +125°C |
| Supply Voltage to Ground Potential<br>(Pin 28 to Pin 14) ..... | - 0.5V to +7.0V  |
| DC Voltage Applied to Outputs<br>in High Z State .....         | - 0.5V to +7.0V  |
| DC Input Voltage .....                                         | - 3.0V to +7.0V  |
| DC Program Voltage .....                                       | 13.0V            |

|                                |                                           |
|--------------------------------|-------------------------------------------|
| Static Discharge Voltage ..... | > 2001V<br>(per MIL-STD-883, Method 3015) |
| Latch-Up Current .....         | > 200 mA                                  |
| UV Exposure .....              | 7258 Wsec/cm <sup>2</sup>                 |

**Operating Range**

| Range                     | Ambient Temperature | V <sub>CC</sub> |
|---------------------------|---------------------|-----------------|
| Commercial                | 0°C to +70°C        | 5V ± 10%        |
| Industrial <sup>[2]</sup> | - 40°C to +85°C     | 5V ± 10%        |
| Military <sup>[3]</sup>   | - 55°C to +125°C    | 5V ± 10%        |

**Electrical Characteristics Over the Operating Range<sup>[4, 5, 6]</sup>**

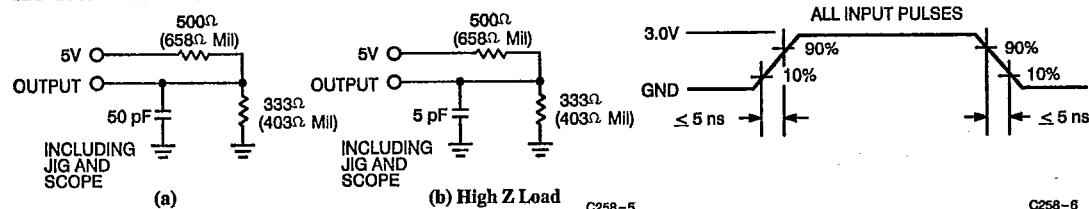
| Parameter       | Description                                 | Test Conditions                                            | Min.  | Max. | Units |
|-----------------|---------------------------------------------|------------------------------------------------------------|-------|------|-------|
| V <sub>OH</sub> | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = - 2 mA           | 2.4   |      | V     |
| V <sub>OL</sub> | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8 mA             |       | 0.4  | V     |
|                 |                                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 6 mA             |       | 0.4  | V     |
| V <sub>IH</sub> | Input HIGH Voltage                          | Guaranteed Input Logical HIGH Voltage for all Inputs       | 2.0   | 6.0  | V     |
| V <sub>IL</sub> | Input LOW Voltage                           | Guaranteed Input Logical LOW Voltage for all Inputs        | - 3.0 | 0.8  | V     |
| I <sub>IX</sub> | Input Load Current                          | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                    | - 10  | +10  | μA    |
| I <sub>OZ</sub> | Output Leakage Current                      | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled | - 40  | +40  | μA    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[7]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND             | - 20  | - 90 | mA    |
| I <sub>CC</sub> | Maximum Operating Current                   | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA            |       | 175  | mA    |
|                 |                                             | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA            |       | 200  | mA    |

**Capacitance<sup>[5]</sup>**

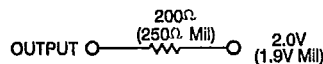
| Parameters       | Description        | Test Conditions                                             | Max. | Units |
|------------------|--------------------|-------------------------------------------------------------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 10   | pF    |
| C <sub>OUT</sub> | Output Capacitance |                                                             | 10   | pF    |

**Notes:**

- Contact a Cypress representative for industrial temperature range specification.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- See Introduction to CMOS PROMs in this Data Book for general information on testing.
- Data for 12-ns Commercial and 15-ns Military is advanced information.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

**AC Test Loads and Waveforms<sup>[4]</sup>**

Equivalent to: THEVENIN EQUIVALENT





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Switching Characteristics Over the Operating Range<sup>[3,4]</sup>

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| Parameters                  | Description                                            | Commercial |      |       |      |       |      | Military |      |       |      |       |      | Units |
|-----------------------------|--------------------------------------------------------|------------|------|-------|------|-------|------|----------|------|-------|------|-------|------|-------|
|                             |                                                        | 12 ns      |      | 15 ns |      | 18 ns |      | 15 ns    |      | 18 ns |      | 25 ns |      |       |
|                             |                                                        | Min.       | Max. | Min.  | Max. | Min.  | Max. | Min.     | Max. | Min.  | Max. | Min.  | Max. |       |
| t <sub>CP</sub>             | Clock Period                                           | 12         |      | 15    |      | 18    |      | 15       |      | 18    |      | 25    |      | ns    |
| t <sub>CH</sub>             | Clock HIGH                                             | 5          |      | 6.5   |      | 8     |      | 6.5      |      | 8     |      | 11.5  |      | ns    |
| t <sub>CL</sub>             | Clock LOW                                              | 5          |      | 6.5   |      | 8     |      | 6.5      |      | 8     |      | 11.5  |      | ns    |
| t <sub>AS</sub>             | Address Set-Up to CLK                                  | 3/7        |      | 4/8   |      | 5/9   |      | 4/8      |      | 5/9   |      | 6/10  |      | ns    |
| t <sub>AH</sub>             | Address hold from CLK                                  | 3/0        |      | 4/1   |      | 5/2   |      | 4/1      |      | 5/2   |      | 6/3   |      | ns    |
| t <sub>ABS</sub>            | Address Set-Up to CLK with Input Bypassed              | 12         |      | 15    |      | 18    |      | 15       |      | 18    |      | 25    |      | ns    |
| t <sub>ABH</sub>            | Address Hold from CLK with Input Bypassed              | 0          |      | 0     |      | 0     |      | 0        |      | 0     |      | 0     |      | ns    |
| t <sub>CSS</sub>            | Chip Select Set-Up to CLK                              | 3/7        |      | 4/8   |      | 5/9   |      | 4/8      |      | 5/9   |      | 6/10  |      | ns    |
| t <sub>CSH</sub>            | Chip Select Hold from CLK                              | 3/0        |      | 4/1   |      | 5/2   |      | 4/1      |      | 5/2   |      | 6/3   |      | ns    |
| t <sub>CKO</sub>            | CLK to Data Valid                                      |            | 9    |       | 11   |       | 13   |          | 11   |       | 13   |       | 15   | ns    |
| t <sub>DH</sub>             | Data Hold From CLK                                     | 0          |      | 0     |      | 0     |      | 0        |      | 0     |      | 0     |      | ns    |
| t <sub>COV</sub>            | CLK to Output Valid <sup>[7]</sup>                     |            | 9    |       | 11   |       | 13   |          | 11   |       | 13   |       | 15   | ns    |
| t <sub>COZ</sub>            | CLK to High Z Output <sup>[8]</sup>                    |            | 9    |       | 11   |       | 13   |          | 11   |       | 13   |       | 15   | ns    |
| t <sub>CSV</sub>            | CS to Output Valid with Input Bypassed <sup>[8]</sup>  |            | 12   |       | 15   |       | 18   |          | 15   |       | 18   |       | 21   | ns    |
| t <sub>CSZ</sub>            | CS to High Z Output with Input Bypassed <sup>[8]</sup> |            | 12   |       | 15   |       | 18   |          | 15   |       | 18   |       | 21   | ns    |
| t <sub>OE<sub>V</sub></sub> | OE to Output Valid <sup>[7]</sup>                      |            | 9    |       | 11   |       | 13   |          | 11   |       | 13   |       | 15   | ns    |
| t <sub>OE<sub>Z</sub></sub> | OE to High Z Output <sup>[8]</sup>                     |            | 9    |       | 11   |       | 13   |          | 11   |       | 13   |       | 15   | ns    |
| t <sub>IS</sub>             | INIT Set-Up to CLK                                     | 3/7        |      | 4/8   |      | 5/9   |      | 4/8      |      | 5/9   |      | 6/10  |      | ns    |
| t <sub>IH</sub>             | INIT Hold from CLK                                     | 3/0        |      | 4/1   |      | 5/2   |      | 4/1      |      | 5/2   |      | 6/3   |      | ns    |
| t <sub>IBS</sub>            | INIT Set-Up to CLK with Input Bypassed                 | 12         |      | 15    |      | 18    |      | 15       |      | 18    |      | 25    |      | ns    |
| t <sub>IBH</sub>            | INIT Hold from CLK with Input Bypassed                 | 0          |      | 0     |      | 0     |      | 0        |      | 0     |      | 0     |      | ns    |
| t <sub>PD</sub>             | Propagation Delay with Input and Output Bypassed       |            | 18   |       | 21   |       | 25   |          | 21   |       | 25   |       | 30   | ns    |
| t <sub>ICO</sub>            | CLK to Output Valid with Output Bypassed               |            | 18   |       | 21   |       | 25   |          | 21   |       | 25   |       | 30   | ns    |
| t <sub>IW</sub>             | Asynchronous INIT Pulse Width                          | 12         |      | 15    |      | 18    |      | 15       |      | 18    |      | 25    |      | ns    |
| t <sub>IDV</sub>            | Asynchronous INIT to Data Valid                        |            | 12   |       | 15   |       | 18   |          | 15   |       | 18   |       | 25   | ns    |
| t <sub>ICR</sub>            | Asynchronous INIT Recovery to Clock                    | 12         |      | 15    |      | 18    |      | 15       |      | 18    |      | 25    |      | ns    |

Shaded area contains advanced information.

Notes:

8. See Output Waveform—Measurement Level



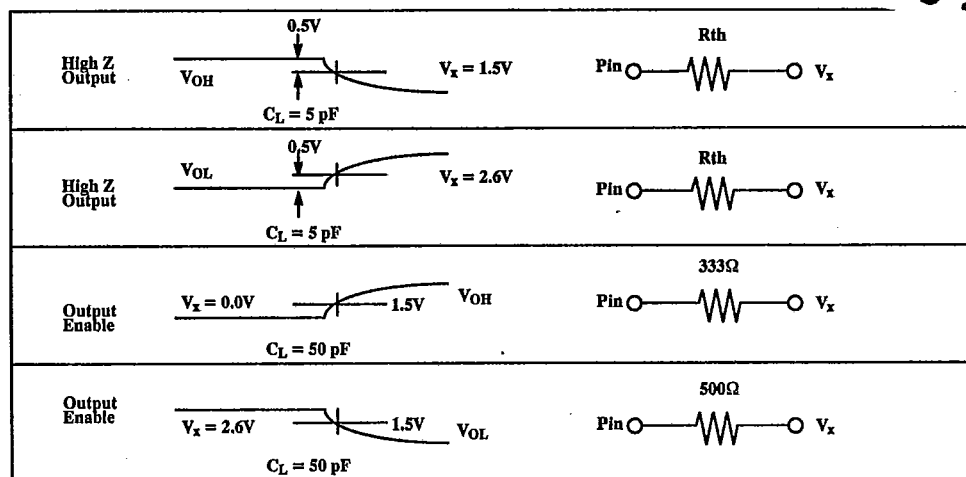
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## Output Waveform—Measurement Level

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C258-7



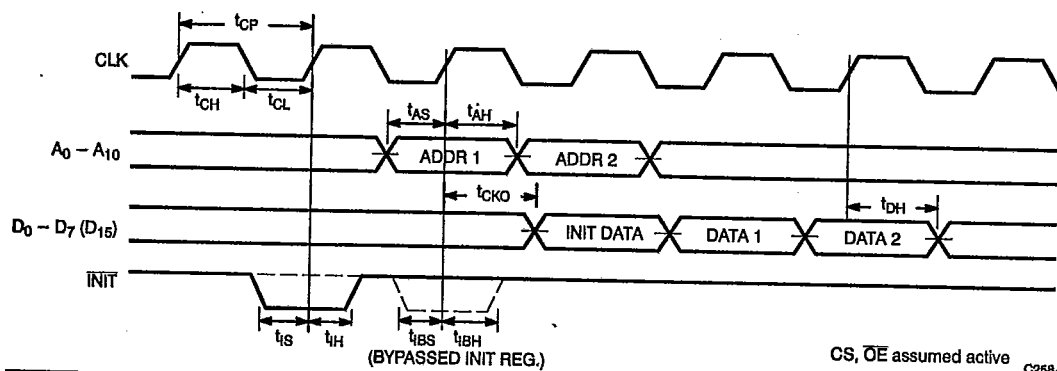
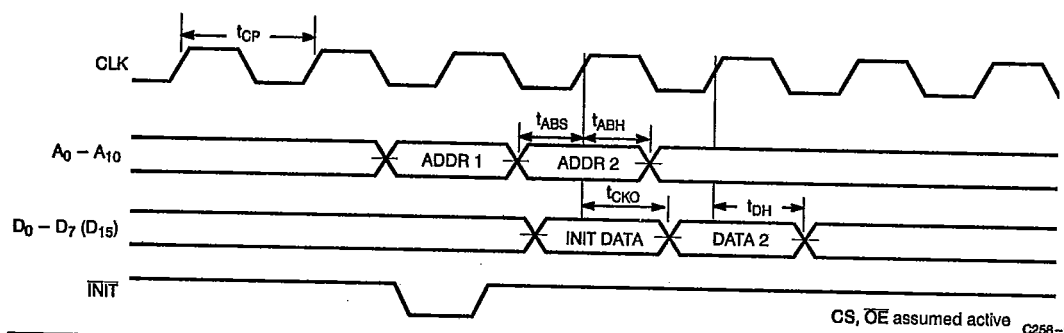
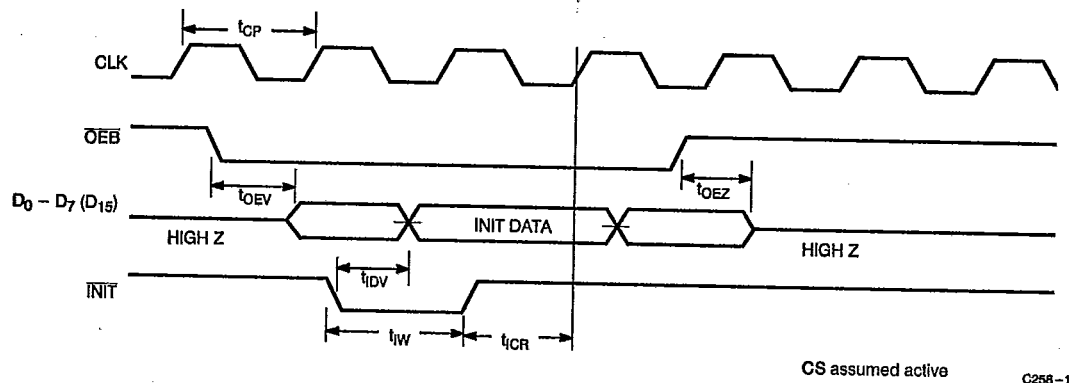
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## Switching Waveforms

T-46-13-29

Registered Input and Output (combined with  $\overline{\text{INIT}}$ )Bypassed Address and  $\overline{\text{INIT}}$  RegistersAsynchronous  $\overline{\text{INIT}}$  and  $\overline{\text{OE}}$ 

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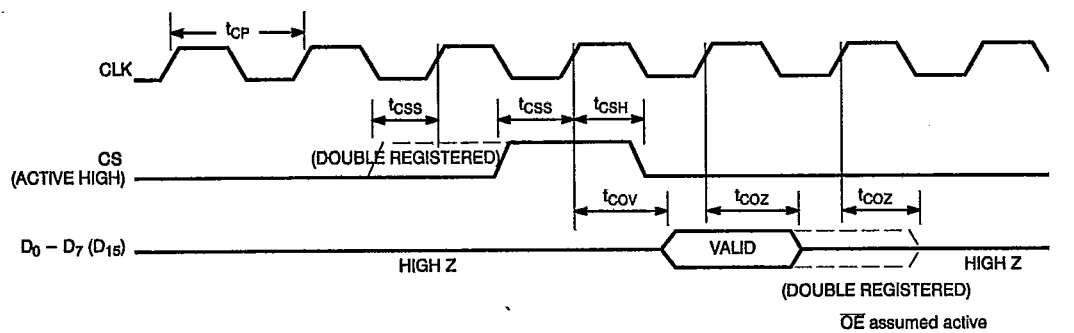


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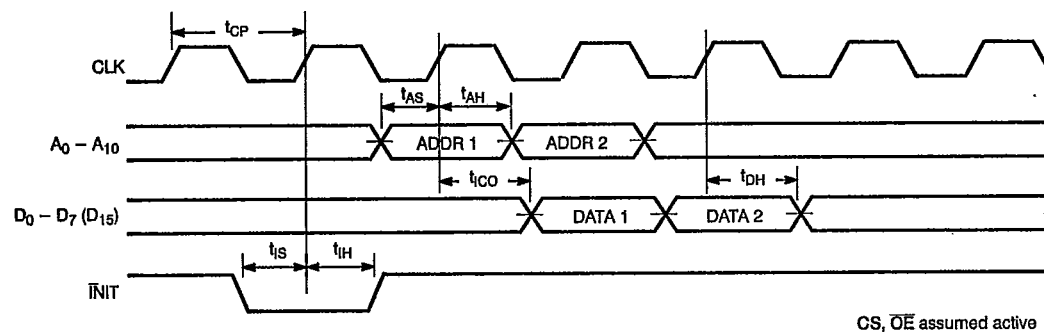
## Switching Waveforms

## Single- and Double-Registered Chip Select

T-46-13-29

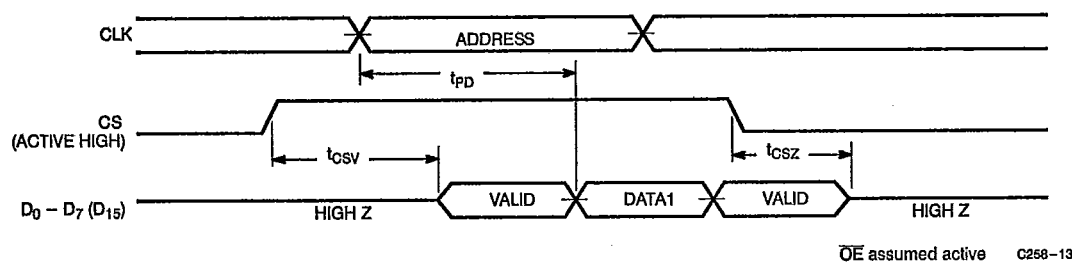


C258-11

Bypassed Output Register<sup>9)</sup>

C258-12

## Bypassed Input and Output Register (CS and Address)



C258-13

## Note:

9. INIT only sets output register even though register is bypassed (for feedback purposes).



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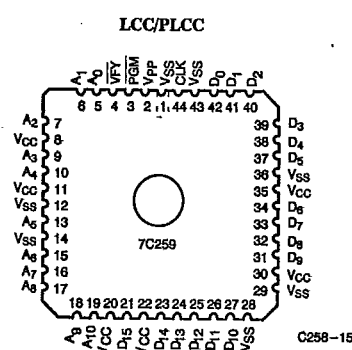
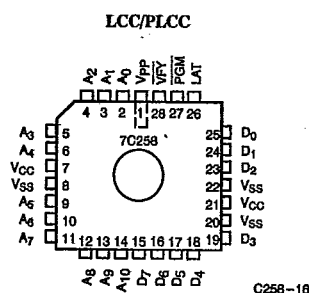
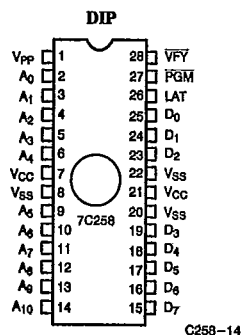
CY7C259

## Mode Table

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| Mode            | LAT<br>(7C258-CLK) | VPP<br>(INIT)   | PGM<br>(CS)      | VFY<br>(OE)      | D <sub>0</sub> -D <sub>15</sub> (259)<br>D <sub>0</sub> -D <sub>7</sub> (258) |
|-----------------|--------------------|-----------------|------------------|------------------|-------------------------------------------------------------------------------|
| Latch High Byte | V <sub>IHP</sub>   | V <sub>PP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> /V <sub>ILP</sub>                                            |
| Program Inhibit | V <sub>ILP</sub>   | V <sub>PP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | HI-Z                                                                          |
| Program Enable  | V <sub>ILP</sub>   | V <sub>PP</sub> | V <sub>ILP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> /V <sub>ILP</sub>                                            |
| Program Verify  | V <sub>ILP</sub>   | V <sub>PP</sub> | V <sub>IHP</sub> | V <sub>ILP</sub> | V <sub>OHP</sub> /V <sub>OLP</sub>                                            |

## Programming Pinouts



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## Programming Information

This datasheet provides some but not all the programming information necessary for on-board programming of the CY7C258 and CY7C259. For more information about on-board programming of Cypress PROMs contact your local Cypress Field Sales Engineer or Field Applications Engineer.

7C258 Bitmap<sup>[10]</sup>

| Programmer<br>Address<br>Decimal | Programmer<br>Address<br>Hex | Programmer<br>Memory<br>7C258                    | Bit Breakdown         |                 |                 |                 |                 |                 |                |                |                 |                |                |                |                |                |                |                |
|----------------------------------|------------------------------|--------------------------------------------------|-----------------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
|                                  |                              |                                                  | D <sub>15</sub>       | D <sub>14</sub> | D <sub>13</sub> | D <sub>12</sub> | D <sub>11</sub> | D <sub>10</sub> | D <sub>9</sub> | D <sub>8</sub> | D <sub>7</sub>  | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
| 0                                | 0                            | Data                                             | <div>Array Data</div> |                 |                 |                 |                 |                 |                |                |                 |                |                |                |                |                |                |                |
| .                                | .                            | .                                                |                       |                 |                 |                 |                 |                 |                |                |                 |                |                |                |                |                |                |                |
| .                                | .                            | .                                                |                       |                 |                 |                 |                 |                 |                |                |                 |                |                |                |                |                |                |                |
| .                                | .                            | .                                                |                       |                 |                 |                 |                 |                 |                |                |                 |                |                |                |                |                |                |                |
| .                                | .                            | .                                                |                       |                 |                 |                 |                 |                 |                |                |                 |                |                |                |                |                |                |                |
| 2047                             | 7FF                          | Data                                             |                       |                 |                 |                 |                 |                 |                |                |                 |                |                |                |                |                |                |                |
| 2048                             | 800                          | Address Register Select<br>(1=Bypassed Register) | A <sub>9</sub>        | A <sub>8</sub>  | A <sub>7</sub>  | A <sub>6</sub>  | A <sub>5</sub>  | A <sub>2</sub>  | A <sub>1</sub> | A <sub>0</sub> | A <sub>10</sub> | X              | X              | X              | X              | X              | A <sub>4</sub> | A <sub>3</sub> |
| 2049                             | 801                          | Array Input Select<br>(1= Feedback)              | A <sub>9</sub>        | A <sub>8</sub>  | A <sub>7</sub>  | A <sub>6</sub>  | A <sub>5</sub>  | A <sub>2</sub>  | A <sub>1</sub> | A <sub>0</sub> | A <sub>10</sub> | X              | X              | X              | X              | X              | A <sub>4</sub> | A <sub>3</sub> |
| 2050                             | 802                          | Output Register Select<br>(1= Bypassed Register) | X                     | X               | X               | X               | X               | X               | X              | X              | D <sub>7</sub>  | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
| 2051                             | 803                          | INIT WORD<br>(1= INIT Bit 1)                     | D <sub>15</sub>       | D <sub>14</sub> | D <sub>13</sub> | D <sub>12</sub> | D <sub>11</sub> | D <sub>10</sub> | D <sub>9</sub> | D <sub>8</sub> | D <sub>7</sub>  | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
| 2052                             | 804                          | Architecture                                     | X                     | X               | X               | X               | X               | X               | X              | X              | SH              | C <sub>1</sub> | C <sub>2</sub> | CP             | IB             | IA             | X              | X              |

## Notes:

10. All configurable bits default to 0.





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7C259 Bitmap<sup>[10]</sup>

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| Programmer<br>Address<br>Decimal | Programmer<br>Address<br>Hex | Programmer<br>Memory<br>7C259                     | Bit Breakdown   |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |
|----------------------------------|------------------------------|---------------------------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
|                                  |                              |                                                   | D <sub>15</sub> | D <sub>14</sub> | D <sub>13</sub> | D <sub>12</sub> | D <sub>11</sub> | D <sub>10</sub> | D <sub>9</sub> | D <sub>8</sub> | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
| 0                                | 0                            | Data                                              | Array Data      |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |
| .                                | .                            | .                                                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |
| .                                | .                            | .                                                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |
| .                                | .                            | .                                                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |
| .                                | .                            | .                                                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |
| 2047                             | 7FF                          | Data                                              |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |
| 2048                             | 800                          | Address RegisterSelect<br>(1 = Bypassed Register) | A <sub>10</sub> | A <sub>9</sub>  | A <sub>8</sub>  | A <sub>7</sub>  | A <sub>6</sub>  | A <sub>5</sub>  | X              | X              | X              | X              | X              | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |
| 2049                             | 801                          | Array Input Select<br>(1 = Feedback)              | A <sub>10</sub> | A <sub>9</sub>  | A <sub>8</sub>  | A <sub>7</sub>  | A <sub>6</sub>  | A <sub>5</sub>  | X              | X              | X              | X              | X              | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |
| 2050                             | 802                          | Output RegisterSelect<br>(1 = Bypassed Register)  | D <sub>15</sub> | D <sub>14</sub> | D <sub>13</sub> | D <sub>12</sub> | D <sub>11</sub> | D <sub>10</sub> | D <sub>9</sub> | D <sub>8</sub> | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
| 2051                             | 803                          | INIT WORD<br>(1 = INIT Bit 1)                     | D <sub>15</sub> | D <sub>14</sub> | D <sub>13</sub> | D <sub>12</sub> | D <sub>11</sub> | D <sub>10</sub> | D <sub>9</sub> | D <sub>8</sub> | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
| 2052                             | 804                          | Architecture                                      | SH              | C <sub>1</sub>  | C <sub>2</sub>  | CP              | IB              | IA              | X              | X              | X              | X              | X              | X              | X              | X              | X              | X              |

## Architecture Word

| Control Option                         | Control Word   |                 |                               | Function                                     |
|----------------------------------------|----------------|-----------------|-------------------------------|----------------------------------------------|
|                                        | Bit (258)      | Bit (259)       | Programmed level              |                                              |
| IA<br>(INIT Async)                     | D <sub>2</sub> | D <sub>10</sub> | 0 = Default<br>1 = Programmed | Synchronous INIT<br>Asynchronous INIT        |
| IB<br>(INIT Bypass)                    | D <sub>3</sub> | D <sub>11</sub> | 0 = Default<br>1 = Programmed | INIT Registered<br>Bypass INIT Register      |
| CP<br>(CS Polarity)                    | D <sub>4</sub> | D <sub>12</sub> | 0 = Default<br>1 = Programmed | CS Active LOW<br>CS Active HIGH              |
| C2<br>(CS Bypass)<br>(Buried Register) | D <sub>5</sub> | D <sub>13</sub> | 0 = Default<br>1 = Programmed | CS Input Registered<br>Bypass CS Register    |
| C1<br>(CS Bypass)<br>(Input Register)  | D <sub>6</sub> | D <sub>14</sub> | 0 = Default<br>1 = Programmed | CS Input Registered<br>Bypass CS Register    |
| SH<br>(Set-Up/Hold)                    | D <sub>7</sub> | D <sub>15</sub> | 0 = Default<br>1 = Programmed | Set-Up/Hold = 3/3 ns<br>Set-Up/Hold = 7/0 ns |



PRELIMINARY

CY7C258

CY7C259

## Ordering Information

T-46-13-29

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 12         | CY7C258-12DC  | D16          | Commercial      |
|            | CY7C258-12HC  | H64          |                 |
|            | CY7C258-12JC  | J64          |                 |
|            | CY7C258-12PC  | P15          |                 |
|            | CY7C258-12WC  | W22          |                 |
| 15         | CY7C258-15DC  | D16          | Commercial      |
|            | CY7C258-15HC  | H64          |                 |
|            | CY7C258-15JC  | J64          |                 |
|            | CY7C258-15PC  | P15          |                 |
|            | CY7C258-15WC  | W22          |                 |
|            | CY7C258-15HMB | H64          | Military        |
|            | CY7C258-15LMB | L64          |                 |
|            | CY7C258-15QMB | Q64          |                 |
|            | CY7C258-15WMB | W22          |                 |
|            |               |              |                 |
| 18         | CY7C258-18DC  | D16          | Commercial      |
|            | CY7C258-18HC  | H64          |                 |
|            | CY7C258-18JC  | J64          |                 |
|            | CY7C258-18PC  | P15          |                 |
|            | CY7C258-18WC  | W22          |                 |
|            | CY7C258-18HMB | H64          | Military        |
|            | CY7C258-18LMB | L64          |                 |
|            | CY7C258-18QMB | Q64          |                 |
|            | CY7C258-18WMB | W22          |                 |
|            |               |              |                 |
| 25         | CY7C258-25HMB | H64          | Military        |
|            | CY7C258-25LMB | L64          |                 |
|            | CY7C258-25QMB | Q64          |                 |
|            | CY7C258-25WMB | W22          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 12         | CY7C259-12HC  | H67          | Commercial      |
|            | CY7C259-12JC  | J67          |                 |
| 15         | CY7C259-15HC  | H67          | Commercial      |
|            | CY7C259-15JC  | J67          |                 |
|            | CY7C259-15HMB | H67          | Military        |
|            | CY7C259-15LMB | L67          |                 |
|            | CY7C259-15QMB | Q67          |                 |
| 18         | CY7C259-18HC  | H67          | Commercial      |
|            | CY7C259-18JC  | J67          |                 |
|            | CY7C259-18HMB | H67          | Military        |
|            | CY7C259-18LMB | L67          |                 |
|            | CY7C259-18QMB | Q67          |                 |
| 25         | CY7C259-25HMB | H67          | Military        |
|            | CY7C259-25LMB | L67          |                 |
|            | CY7C259-25QMB | Q67          |                 |

Shaded area contains advanced information.



PROMs



PRELIMINARY

**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing**

T-46-13-29

**DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1, 2, 3,  |
| V <sub>OL</sub> | 1, 2, 3,  |
| V <sub>IH</sub> | 1, 2, 3,  |
| V <sub>IL</sub> | 1, 2, 3,  |
| I <sub>IX</sub> | 1, 2, 3,  |
| I <sub>OZ</sub> | 1, 2, 3,  |
| I <sub>CC</sub> | 1, 2, 3,  |
| I <sub>SB</sub> | 1, 2, 3,  |

**Switching Characteristics**

| Parameters       | Subgroups       |
|------------------|-----------------|
| t <sub>CP</sub>  | 7, 8, 9, 10, 11 |
| t <sub>CH</sub>  | 7, 8, 9, 10, 11 |
| t <sub>CL</sub>  | 7, 8, 9, 10, 11 |
| t <sub>AS</sub>  | 7, 8, 9, 10, 11 |
| t <sub>ABS</sub> | 7, 8, 9, 10, 11 |
| t <sub>CSS</sub> | 7, 8, 9, 10, 11 |
| t <sub>CSH</sub> | 7, 8, 9, 10, 11 |
| t <sub>CKO</sub> | 7, 8, 9, 10, 11 |
| t <sub>DH</sub>  | 7, 8, 9, 10, 11 |
| t <sub>COV</sub> | 7, 8, 9, 10, 11 |
| t <sub>CSV</sub> | 7, 8, 9, 10, 11 |
| t <sub>CSZ</sub> | 7, 8, 9, 10, 11 |
| t <sub>OEV</sub> | 7, 8, 9, 10, 11 |
| t <sub>OEZ</sub> | 7, 8, 9, 10, 11 |
| t <sub>IS</sub>  | 7, 8, 9, 10, 11 |
| t <sub>IH</sub>  | 7, 8, 9, 10, 11 |
| t <sub>IBS</sub> | 7, 8, 9, 10, 11 |
| t <sub>IBH</sub> | 7, 8, 9, 10, 11 |
| t <sub>PD</sub>  | 7, 8, 9, 10, 11 |
| t <sub>ICO</sub> | 7, 8, 9, 10, 11 |
| t <sub>IW</sub>  | 7, 8, 9, 10, 11 |
| t <sub>IDV</sub> | 7, 8, 9, 10, 11 |
| t <sub>ICR</sub> | 7, 8, 9, 10, 11 |

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