#### **CMOS 4-Bit Microcontroller**

## TMP47C660AN,TMP47C860AN TMP47C660AF, TMP47C860AF

The TMP47C660A/860A are high speed and high performance 4-bit single chip micro computers, integrating the 8-bit AD converter based on the TLCS-470 series.

Part No.	ROM	RAM	Package	OTP
TMP47C660AN	6144 × 8-bit	384 × 4-bit	P-SDIP64-750-1.78	TMP47P860VN
TMP47C660AF	6144 X 8-DIL	6144 x 8-bit 384 x 4-bit	P-QFP64-1420-1.00A	TMP47P860VF
TMP47C860AN	360AN 9103 8 hit 513 4 hit		P-SDIP64-750-1.78	TMP47P860VN
TMP47C860AF	8192 × 8-bit	512 × 4-bit	P-QFP64-1420-1.00A	TMP47P860VF

#### **Features**

- ◆ 4-bit single chip microcomputer
- lacktriangle Instruction execution time: 1.3  $\mu$ s (at 6 MHz),

244  $\mu$ s (at 32.8 kHz)

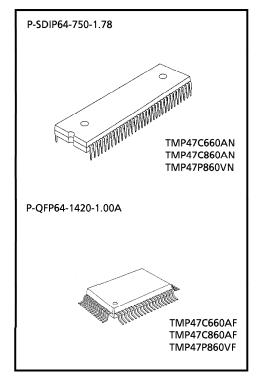
- ◆ 92 basic instructions
  - Table look-up instructions
  - 5-bit to 8-bit data conversion instruction
- ◆ Subroutine nesting: 15 levels max
- ◆ 6 interrupt sources (External: 2, Internal: 4)

All sources have independent latches each, and multiple interrupt control is available.

- ♦ I/O port (56 pins)
  - Input 2 ports 5 pins
  - Output 4 ports 16 pins
  - I/O 9 ports 35 pins
- Interval Timer
- ◆ Two 12-bit Timer / Counters

Timer, event counter, and pulse width measurement mode

◆ Watchdog Timer



For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.

● TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA

making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.

In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..

■ The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments traffic signal instruments control instruments medical instruments. all types of transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's

The products described in this document are subject to the foreign exchange and foreign trade laws.

The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.

The information contained herein is subject to change without notice.

- ◆ Serial Interface with 8-bit buffer
  - Simultaneous transmission and reception capability
  - 8/4-bit transfer, external / internal clock, and leading / trailing edge shift mode
- ◆ 8-bit successive approximate type AD converter
  - With sample and hold
  - 8 analog inputs
  - Conversion time: 32 μs (at 6 MHz)
- ◆ Remote control signal pre-processing capability
- ♦ High current outputs
  - LED direct drive capability (typ. 20 mA × 8 bits)
- ◆ Dual-clock operation
  - High-speed/Low-power-consumption operating mode
- ◆ Hold function
  - Battery/Capacitor back-up
- ◆ Real Time Emulator: BM47C860A

#### **Pin Assignments (Top View)** (1) P-SDIP64-750-1.78 (2) P-OFP64-1420-1.00A VAREF-HOLD XOUT XOUT XOUS VASS → R40 (AINO) ← □ 63 **←** RC3 3 62 **≺≻** RC2 R41 (AIN1) <del><>></del> □ Δ 61 □ ←→ RC1 R42 (AIN2) <del><></del> □ 60 ☐ <del><></del> RC0 ₽ **←>** R92 ( \$CK ) R43 (AIN3 ) ←> □ 6 59 R50 (AIN4) ←> R91 (SO) R90 (SI) 58 R51 (AIN5) ←> □ 57 R91 (SO) ← ► □ 52 R52 (AIN6) ←> □ 56 9 R92 (\$<del>CK</del>) → 53 31 → P30 R53 (AIN7) **←** 10 55 □ **←**➤ R82 (ĪNT1) RC0 ← ► □ 54 30 → P23 R60 <del><></del> □ **←>** R81 (T2) 11 54 RC1 ←→ □□□55 29 → P22 R61 <del><></del> □ **←→** R80 (ĪNT2) RC2<del><-></del>□ 28 → P21 R62 <del><>></del> □ 13 52 → HOLD (KEO) R63 <del><>></del> □ 14 51 → XOUT RC3 <del>← →</del> □ □ 57 27 → P20 VDD → 58 VAREF → 59 R70 <del><→</del> □ R71 (WTO) <del><→</del> □ 15 50 **←**XIN 26 VSS □ <del><---</del>RESET 16 49 25 TEST R72 (XTIN) → □ R73 (XTOUT) → □ VASS → □ □ 60 R40 (AINO) ← ► □ □ 61 17 48 -K03 24 → P13 47 18 -K02 23 → P12 22 → P11 RA0 <del>←→</del> □ 46 -K01 19 R41 (AIN1) --- 62 RA1 <del>←→</del> □ 45 -K00 20 R42 (AIN2) -- 63 21 → P10 RA2 **←**➤ 🖥 **←→** RB3 21 44 $\circ$ R43 (AIN3) -- 64 RA3 <del><>></del> ☐ 43 **←≻** RB2 20 → P03 22 **←** RB1 23 42 24 41 RB0 P02 <del><</del> 25 40 🗖 → P33 80 (A.IN4)-65 (A.IN5)-65 (A.IN5)-P03 <del>←</del> - 🛘 26 39 → P32 P10 <del>←</del> - 口 27 38 → P31 P11 **←** ☐ 28 37 —➤ P30 - 🛮 29 P12 🚤 36 D → P23 R71 7 R72 0 R73 (X 35 → P22 P13 -- 🛮 зо R50 R51 R52 R53 → 🛮 31 → P21 TEST-34 32 33 VSS. High current **Block Diagram** I/O port output ports Output port R63 PC3 to PC0 P33 to P30 RA3 RB3 P23 P13 P03 to RA0 to PQ0 to R60 to RB0 to P10 to P20 $\left\{ \begin{smallmatrix} VDD \\ VSS \end{smallmatrix} \right.$ Power Supply RA RB RC P1 P2 P0 Р3 R6 FLAG C Z S Program Counter Accumulator DMB HR LR Data Memory RAM address buffer (RAM) Program Memory (ROM) Hold input (Sense input) HOLD (KE0) STACK SPW Hold controller EIF TC1 TC2 DC Data table EIR RESET Reset input Interrupt controller System controller Test pin TEST System clock controlle 12-bit Timer/Counter (2ch) IR Interval timer 8-bit 8-bit Serial Interface Decoder AD converte XIN XOUT Osc. High-freq. Clock connecting Watchdog Timer Generator Low-freq. pins R9 ⇕ R8 R5 R7 Remote control signal pre-processor R4 R73 (XTOUT) R72 (XTIN) R71 (WTO) R70 R83 (T1) R82 (INT1) R92 (SCK) VAREF R43 (AIN3) R53 (AIN7) K03 R91 (SO) R90 (SI) VASS to K00 to to R40 (AIN0 R50 (AIN4) R81 (T2) R80 (INT2) Analog reference I/O port (Osc.connecting pins (Low-freq.) ) I/O ( T/C input Interrupt input) I/O port I/O port (Analog input) Input port

voltage

(Serial port)

# **Pin Function**

Pin Name	Input / Output	Functions				
K03 to K00	Input	4-bit input port				
P03 to P00		4-bit output port with latch				
P13 to P10	Outrot	4-bit output port with latch. 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].				
P23 to P20	Output					
P33 to P30		4-bit output port with latch				
R53 (AIN7) to R40 (AIN0)	I/O (Input)	4-bit I/O port with latch.	AD converter analog input			
R63 to R60	I/O	When used as input port, watchdog timer output or analog input, the latch must be set to "1".				
R73 (XTOUT)	I/O (Output)	Set to Dual-clock operating mode, when	Resonator connecting pin (Low-freq.). For inputting external clock, XTIN is			
R72 (XTIN)	I/O (Input)	R73,R72 pin use as clock generator.	used and XTOUT is opened.			
R71 (WTO)	I/O (Output)	Can be set, cleared, and tested for each bit as specified by L register indirect addressing bit manipulation instructions.	Watchdog timer output			
R70	I/O					
R83 (T1)		4-bit I/O port with latch.	Timer/Counter 1 external input			
R82 (INT1)		When used as input port, external interrupt input pin, or timer/counter external input	External interrpt 1 input			
R81 (T2)	I/O (Input)	pin, the latch must be set to "1".	Timer/Counter 2 external input			
R80 ( <del>INT2</del> )			External interrpt 2 or REMO-COM input			
R92 (SCK)	I/O(I/O)		Serial clock I/O			
R91 (SO)	I/O (Output)	3-bit I/O port with latch.  When used as input port or serial port, the	Serial data output			
R90 (SI)	I/O (Input)	latch must be set to "1".	Serial data input			
RA3 to RA0						
RB3 to RB0	I/O	4-bit I/O port with latch. When used as input port, the latch must be set t	be set to "1".			
RC3 to RC0						
XIN	Input	Resonator connecting pin (High-frequency) .				
хоит	Output	For inputting external clock, XIN is used and X	OUT is opened.			
RESET	Input	Reset signal input				
HOLD (KEO)	Input (Input)	HOLD request/release signal input	Sence input			
TEST	Input	Test pin for out-going test. Be opened or fixed	d to low level.			
VDD		+5 V				
vss	Davisan susandu	0 V (GND)				
VAREF	Power supply	AD converter analog reference voltage (High)				
VASS		AD converter analog reference voltage (Low)				

### **Operational Description**

### 1. System Configuration

- ◆ Internal CPU Function
  - 2.1 Program Counter (PC)
  - 2.2 Program Memory (ROM)
  - 2.3 H Register, L Register, and Data Memory Bank Selector (DMB)
  - 2.4 Data Memory (RAM)
    - Stack
    - Stack Pointer Word (SPW)
    - Data Counter (DC)
  - 2.5 Accumulator
  - 2.6 Flags
  - 2.7 Clock Generator, Timing Generator, System Clock Controller
  - 2.8 Interrupt Controller
  - 2.9 Reset Circuit
- Peripheral Hardware Function
  - 3.1 Input/Output Ports
  - 3.2 Interval Timer
  - 3.3 Timer / Counters (TC1, TC2)
  - 3.4 Watchdog Timer
  - 3.5 Remote Control Pulse Detector
  - 3.6 AD Converter
  - 3.7 Serial Interface

Concerning the above component parts, the hardware configuration and functions are described.

#### 2. Internal CPU Function

#### 2.1 Program Counter (PC)

The program counter is a 13-bit binary counter which indicates the address of the program memory storing the next instruction to be executed. Normally, the PC is incremented by the number of bytes of the instruction every time it is fetched. When a branch instruction or a subroutine instruction has been executed or an interrupt has been accepted, the specified values listed in Table 2-1 are set to the PC. The PC is initialized to "0" during reset.

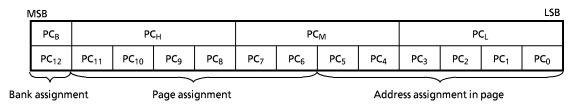


Figure 2-1. Configuration of program counter

The PC can directly address an 8192-byte address space. However, with the short/middle branch and subroutine call instructions, the following points must be considered:

- (1) Short branch instruction [BSS a]
  - In [BSS a] instruction execution, when the branch condition is satisfied the status flag is "1", the value specified in the instruction is set to the lower 6 bits of the PC. That is, [BSS a] becomes the inpage branch instruction. When [BSS a] is stored at the last address of the page, the upper 7 bits of the PC point the next page, so that branch is made to the next page.
- (2) Middle branch instruction [BS a]
  - In [BS a] instruction execution, when the branch condition is satisfied, the value specified in the instruction is set to the lower 12 bits of the PC. That is, [BS a] becomes the in-bank branch instruction.
  - When first byte or second byte of this instruction is stored at the last address of the bank, the most significant bit of the PC point the next bank, so that branch is made to the next bank.
- (3) Subroutine call instruction [CALL a]
  - In [CALL a] instruction execution, the contents of the PC are saved to the stack then the value specified by the instruction is set to the PC. The address which can be specified by the instruction consists of 11 bits and the upper 2 bits of the PC is always "0". Therefore, the entry address of the subroutine should be within an address range of 0000<sub>H</sub> through 07FF<sub>H</sub>.

Instruction Program Counter (PC) Condition Operation PC12 PC11 PC10 PC9 PC8 PC7 PC6 PC5 PC4 PC3 PC2 PC1 PC0 (Branch condition is satisfied) Immediata data specified by the instruction BSL SF = 0(Branch condition is not satisfied) Lower 12-bit address ≠ FFE, FFF<sub>H</sub> Hold Immediata data specified by the instruction SF = 1 Lower 12-bit address = FFE, FFF<sub>H</sub> BS а + 1 Immediata data specified by the instruction  $\subseteq$ (Last address in bank) SF = 0 + 2 4 Immediata data specified by the o Lower 6-bit address ≠ 3F<sub>H</sub> Hold SF = 1 Lower 6-bit address = 3F<sub>H</sub> Immediata data specified by the BSS + 1 (Last address in page) instruction 4 SF = 0 + 1 \_ CALL 0 Immediata data specified by the instruction 0 а The value generated by the immediate CALLS 0 0 0 1 data specified by the instruction RET The return address restored from stack RETI The return address restored from stack Others Incremented by the number of bytes in the instruction 0 0 0 0 0 0 0 Interrupt vector Interrupt acceptance 0 0 0 0 0 0 0 0 0 0 0 0 Reset

Table 2-1. Status change of program counter

#### 2.2 Program Memory (ROM)

Programs and fixed data are stored in the program memory. The instruction to be executed next is read from the address indicated by the contents of the PC. The fixed data can be read Bank by using the table look-up instructions or 5-bit to 8-bit data conversion instruction.

(1) Table look-up instructions [LDL A,@DC], [LDH A,@DC+] The table look-up instructions read the lower and upper 4 bits of the fixed data stored at the address specified in the data counter (DC) to place them into the accumulator. [LDL A,@DC] instruction reads the lower 4 bits of fixed data and [LDH A,@DC +] instruction reads the upper 4 bits. The DC is a 12-bit register, and it can specify an address within the range of 1000<sub>H</sub> through 1FFF<sub>H</sub> of the program memory.

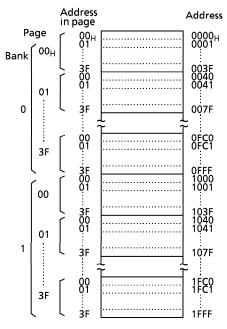


Figure 2-2. Configuration of program memory

### (2) 5-bit to 8-bit data conversion instruction [OUTB @HL]

The 5-bit to 8-bit data conversion instruction reads the fixed data (8 bits) from the data conversion table in the program memory to output the upper 4 bits to port P2 and the lower 4 bits to port P1. The table is located in the last 32-byte space (addresses 17E0 through 17FFH for the TMP47C660A and addresses 1FEOH through 1FFFH for the TMP47C860A) in the program memory with the lower address consisting of the 5 bits obtained by linking the data memory contents specified by the HL register pair and the content of the carry flag.

This instruction is suitable for such applications as converting BCD data into an output code to the 7-segment display elements.

Example: The following shows that the BCD data at address  $2F_H$  in data memory is converted into the 7-segment code (anode common LED) to be output to ports P2 and P1.

HL,#2F<sub>H</sub>; HL←2F<sub>H</sub> (Data memory address is set) LD

**TEST** CF

; CF←0 (The table is specified at addresses 1FE0<sub>H</sub> - 1FEF<sub>H</sub>)

**OUTB** @HL

ORG ; Data conversion table 1FE0H

DATA OCOH.OF9H.OA4H.OBOH.99H.92H.82H.OD8H.80H.98H

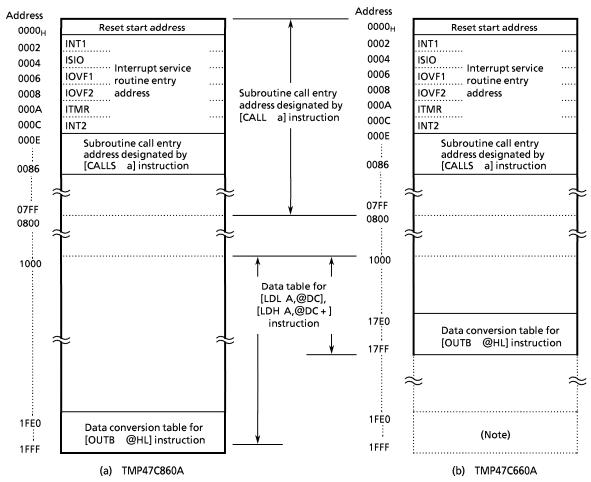


#### 2.2.1 **Program memory map**

Figure 2-3 shows the program memory map. Address 0000 through 0086H and 1FE0 through 1FFFH for the TMP47C860A, 0000 through 0086H and 17E0 through 17FFH for the TMP47C660A, of the program memory are also used for special purposes.

#### 2.2.2 Program memory capacity

The TMP47C860A has  $8192 \times 8$  bits (addresses 0000 through 1FFF<sub>H</sub>) and the TMP47C660A has  $6144 \times 8$  bits (0000 through 17FF<sub>H</sub>), of the program memory (mask ROM).



ote: In case of the TMP47C660A, 5-bit to 8-bit data conversion table is at address 17E0 through 1FFF $_{\rm H}$ . When the piggyback is used in order to evaluate the TMP47C660A, it is necessary to also place a conversion table at address 1FE0 through 1FFF $_{\rm H}$  and operation are exactly the same.

Figure 2-3. Program memory map

## 2.3 H Register, L Register, and Data Memory Bank Selector (DMB)

The H register and the L register are 4-bit general registers. They are also used as a register pair (HL) for the data memory (RAM) addressing pointer. The data memory consists of pages, each page being 16 words long (1 word = 4 bits). The H register specifies a page and the L register specifies an address in the page. The data memory consists of two banks (bank0 and bank1). The data memory bank selector (DMB) is a 1-bit register to specify a data memory bank. During reset, the DMB is initialized to "0". The DMB is set or cleared by the [CLR DMB] or [SET DMB] instructions. The currently selected data memory bank can be known by executing the [TEST DMB] or [TESTP DMB] instruction.

The L register has the automatic post-increment/decrement capability, implementing the execution of composite instructions. For example, [ST A,@HL +] instruction automatically increments the contents of the L register after data transfer. During the execution [SET @L], [CLR @L], or [TEST @L] instruction, the L register is also used to specify the bits corresponding to I/O port pins R73 through R40 (the indirect addressing of port bits by the L register).

#### **Electrical Characteristics**

Absolute Maximum Ratings  $(V_{SS} = 0 V)$ 

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	$V_{DD}$		– 0.3 to 6.5	V
Input Voltage	$V_{IN}$		- 0.3 to V <sub>DD</sub> + 0.3	٧
Output Voltage	V <sub>OUT</sub>		- 0.3 to V <sub>DD</sub> + 0.3	٧
	I <sub>OUT1</sub>	Ports R	3.2	
Output Current (per 1 pin)	lOUT2	Ports P1, P2	30	mA
	I <sub>OUT3</sub>	Ports P0, P3	15	
Output Compant (tatal)	Σ I <sub>OUT1</sub>	Ports P0, P1	120	A
Output Current (total)	Σ I <sub>OUT2</sub>	Ports P2, P3	120	mA
Power Dissipation [Topr = 70°C]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 40 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

**Recommended Opeating Conditions** 

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
			In the Normal mode	4.5		
Supply Voltage	$V_{DD}$		In the SLOW mode	2.7	5.5	V
			In the HOLD mode	2.0		
	V <sub>IH1</sub>	Except Hysteresis Input	V >45V	$V_{DD} \times 0.7$		
Input High Voltage	V <sub>IH2</sub>	Hysteresis Input	V <sub>DD</sub> ≧ 4.5 V	$V_{DD} \times 0.75$	$V_{DD}$	V
	V <sub>IH3</sub>		V <sub>DD</sub> < 4.5 V V <sub>DD</sub> × 0.9			
	V <sub>IL1</sub>	Except Hysteresis Input	V >45V		$V_{DD} \times 0.3$	
Input Low Voltage	$V_{IL2}$	Hysteresis Input	V <sub>DD</sub> ≧ 4.5 V	0	$V_{DD} \times 0.25$	V
	V <sub>IL3</sub>		V <sub>DD</sub> <4.5 V		$V_{DD} \times 0.1$	
Clask Francians	fc	XIN, XOUT		0.4	6.0	MHz
Clock Frequency	fs	XTIN, XTOUT		30	34	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Input voltage  $V_{IH3}$ ,  $V_{IL3}$ : In the SLOW or HOLD mode.

DC Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis Voltage	$V_{HS}$	Hysteresis Input		_	0.7	_	٧
Input Current	I <sub>IN1</sub>	Port K0, TEST, RESET, HOLD	V <sub>DD</sub> = 5.5 V,	_	-	± 2	_
	I <sub>IN2</sub>	Ports R (open drain)	V <sub>IN</sub> = 5.5 V / 0 V				μΑ
Low Input Current	I <sub>IL</sub>	Ports R (push-pull )	$V_{DD} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	-	1	- 2	mA
Input Resistance	R <sub>IN1</sub>	Port KO with pull-up/pull-down		30	70	150	
input Resistance	R <sub>IN2</sub>	RESET		100	220	450	kΩ
Output Leakage Current	I <sub>LO</sub>	Ports (open drain)	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V	_	1	2	μΑ
Output High Voltage	V <sub>OH</sub>	Ports (push-pull )	V <sub>DD</sub> = 4.5 V,   I <sub>OH</sub> = - 200 μA	2.4	1	ı	v
Output Low Voltage	$V_{OL}$	Except XOUT, ports P	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$	_	1	0.4	V
	I <sub>OL2</sub>			_	30	ı	mA
Output Low Current	I <sub>OL3</sub>	Ports P0, P3	$V_{DD} = 4.5 \text{ V}, V_{OL} = 1.0 \text{ V}$	_	13	1	1112
Supply Current (in the Normal mode)	I <sub>DD</sub>		$V_{DD} = 5.5 V$ fc = 4 MHz	_	3	6	mA
Supply Current	I <sub>DDS</sub>		V <sub>DD</sub> = 3.0 V	_	30	60	μA
(in the SLOW mode)			fs = 32.768 kHz				
Supply Current (in the HOLD mode)	I <sub>DDH</sub>		V <sub>DD</sub> = 5.5 V	_	0.5	10	μΑ

- Note 1: Typ. values show those at  $T_{opr} = 25$ °C,  $V_{DD} = 5$  V.
- Note 2: Input Current I<sub>IN1</sub>; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.
- Note 3: Supply Current  $I_{DD}$ ,  $I_{DDH}$ ;  $V_{IN} = 5.3 \text{ V} / 0.2 \text{ V}$

The KO port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.

Supply Current  $I_{DDS}$ ;  $V_{IN} = 2.8 V/0.2 V$ 

Low frequency clock is only osillated (connecting XTIN, XTOUT).

**AD Conversion Characteristics** 

 $(Topr = -40 \text{ to } 70^{\circ}C)$ 

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
	V <sub>AREF</sub>		V <sub>DD</sub> _ 1.5	_	V <sub>DD</sub>	
Analog Reference Voltage	V <sub>ASS</sub>		V <sub>SS</sub>	_	1.5	V
Analog Reference Voltage Range	$_{\Delta}V_{AREF}$	V <sub>AREF</sub> -V <sub>ASS</sub>	2.5	_	_	V
Analog Input Voltage	V <sub>AIN</sub>		V <sub>ASS</sub>	_	V <sub>AREF</sub>	V
Analog Supply Current	I <sub>REF</sub>		_	0.5	1.0	mA
Nonlinearity Error			_	_	± 1	
Zero Point Error		$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, V_{SS} = 0.0 \text{ V}$ $V_{AREF} = V_{DD} \pm 0.001 \text{ V}$	_	_	± 1	
Full Scale Error			_	_	± 1	LSB
Total Error		$V_{ASS} = 0.000 V$	_	_	± 2	

**AC Characteristics** 

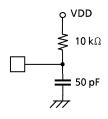
 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 70^{\circ}\text{C})$ 

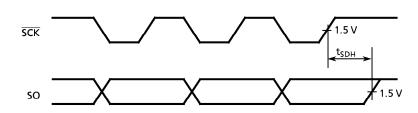
Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Instruction Cycle Time	tcy	In the Normal mode	1.3	_	20	ns
mod dedicti cycle mile		In the SLOW mode	235	_	267	
High level Clock pulse Width	t <sub>WCH</sub>	E tourist de la contra	00			
Low level Clock pulse Width	t <sub>WCL</sub>	External clock mode	80	_	_	ns
AD Sampling Time	t <sub>AIN</sub>	fc = 4 MHz	_	4	_	μS
Shift Data Hold Time	t <sub>SDH</sub>		0.5 tcy – 0.3	_	_	μS

Note: Shift Data Hold Time

External circuit for SCK pin and SO pin

Serial port (completion of transmission)





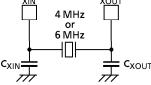
**Recommended Oscillating Conditions** 

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 70^{\circ}\text{C})$ 

(1) 6 MHz

**Ceramic Resonator** 

CSA6.00MGU (MURATA)  $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ KBR-6.00MS (KYOCERA)  $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ 

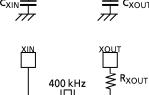


(2) 4 MHz

**Ceramic Resonator** 

CSA4.00MG (MURATA)  $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ KBR-4.00MS (KYOCERA)  $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ Crystal Oscillator

204B-6F 4.0000 (TOYOCOM)  $C_{XIN} = C_{XOUT} = 20 pF$ 

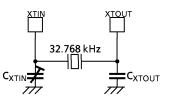


(3) 400 kHz

**Ceramic Resonator** 

CSB400B (MURATA)  $C_{XIN} = C_{XOUT} = 220 \text{ pF}, R_{XOUT} = 6.8 \text{ k}\Omega$ KBR-400B (KYOCERA)  $C_{XIN} = C_{XOUT} = 100 \text{ pF}, R_{XOUT} = 10 \text{ k}\Omega$ 

(4) 32.768 kHz (V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 2.7 to 6.0V, Topr =  $-30 \text{ to } 70^{\circ}\text{C}$ ) Crystal Oscillator  $C_{\text{XTIN}}$ ,  $C_{\text{XTOUT}}$ ; 10 to 33 pF



2000-10-19

Note: In order to get the accurate oscillation frequency, the adjustment of capacitors must be required.

## **Typical Characteristics**

