CMOS 4-Bit Microcontroller

TMP47C660AN,TMP47C860AN TMP47C660AF, TMP47C860AF

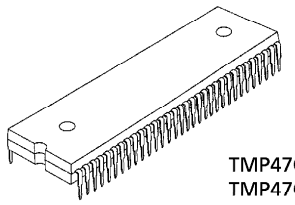
The TMP47C660A/860A are high speed and high performance 4-bit single chip micro computers, integrating the 8-bit AD converter based on the TLCS-470 series.

Part No.	ROM	RAM	Package	OTP
TMP47C660AN	6144 × 8-bit	384 × 4-bit	P-SDIP64-750-1.78	TMP47P860VN
TMP47C660AF			P-QFP64-1420-1.00A	TMP47P860VF
TMP47C860AN	8192 × 8-bit	512 × 4-bit	P-SDIP64-750-1.78	TMP47P860VN
TMP47C860AF			P-QFP64-1420-1.00A	TMP47P860VF

Features

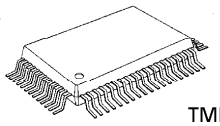
- ◆ 4-bit single chip microcomputer
- ◆ Instruction execution time: 1.3 μs (at 6 MHz), 244 μs (at 32.8 kHz)
- ◆ 92 basic instructions
  - Table look-up instructions
  - 5-bit to 8-bit data conversion instruction
- ◆ Subroutine nesting: 15 levels max
- ◆ 6 interrupt sources (External: 2, Internal: 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆ I/O port (56 pins)
  - Input 2 ports 5 pins
  - Output 4 ports 16 pins
  - I/O 9 ports 35 pins
- ◆ Interval Timer
- ◆ Two 12-bit Timer / Counters
  Timer, event counter,and pulse width measurement mode
- ◆ Watchdog Timer

P-SDIP64-750-1.78



TMP47C660AN
TMP47C860AN
TMP47P860VN

P-QFP64-1420-1.00A



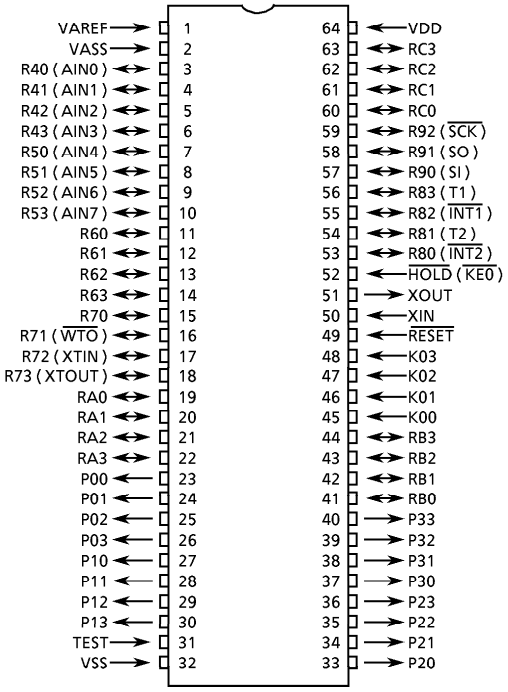
TMP47C660AF
TMP47C860AF
TMP47P860VF

000707EBA1

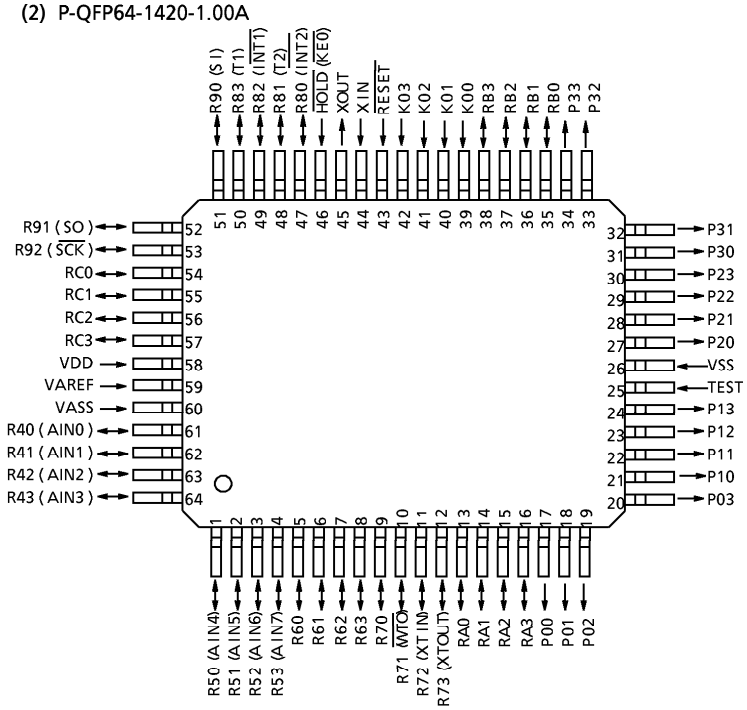
- ◆ Serial Interface with 8-bit buffer
  - Simultaneous transmission and reception capability
  - 8/4-bit transfer, external / internal clock, and leading / trailing edge shift mode
- ◆ 8-bit successive approximate type AD converter
  - With sample and hold
  - 8 analog inputs
  - Conversion time: 32 μs (at 6 MHz)
- ◆ Remote control signal pre-processing capability
- ◆ High current outputs
  LED direct drive capability (typ. 20 mA × 8 bits)
- ◆ Dual-clock operation
  High-speed/Low-power-consumption operating mode
- ◆ Hold function
  Battery/Capacitor back-up
- ◆ Real Time Emulator: BM47C860A

Pin Assignments (Top View)

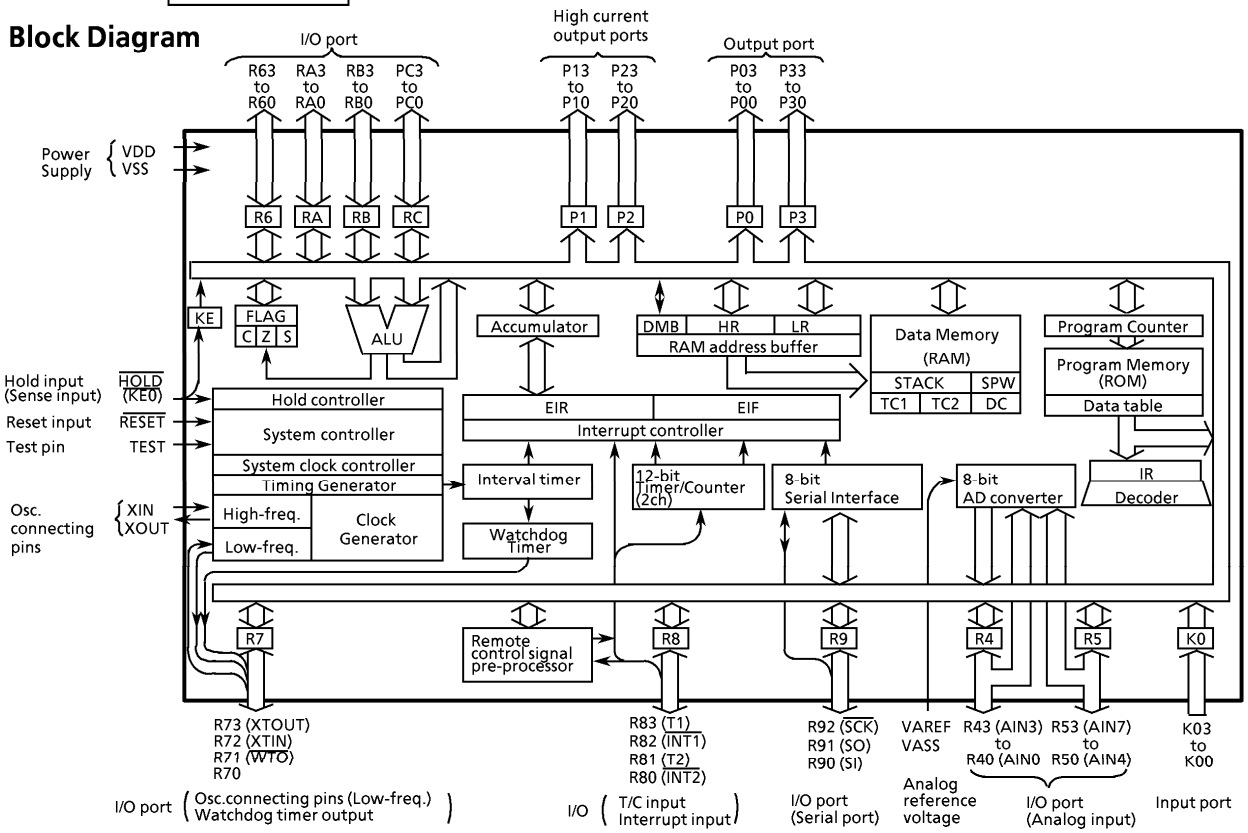
(1) P-SDIP64-750-1.78



(2) P-QFP64-1420-1.00A



Block Diagram



Pin Function

Pin Name	Input / Output	Functions	
K03 to K00	Input	4-bit input port	
P03 to P00	Output	4-bit output port with latch	
P13 to P10		4-bit output port with latch. 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
P23 to P20			
P33 to P30		4-bit output port with latch	
R53 (AIN7) to R40 (AIN0)	I/O (Input)	4-bit I/O port with latch. When used as input port, watchdog timer output or analog input, the latch must be set to "1". Set to Dual-clock operating mode, when R73,R72 pin use as clock generator. Can be set, cleared, and tested for each bit as specified by L register indirect addressing bit manipulation instructions.	AD converter analog input
R63 to R60	I/O		
R73 (XTOUT)	I/O (Output)		Resonator connecting pin (Low-freq.). For inputting external clock, XTIN is used and XTOUT is opened.
R72 (XTIN)	I/O (Input)		
R71 ($\overline{WTO}$)	I/O (Output)		Watchdog timer output
R70	I/O		
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrpt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrpt 2 or REMO-COM input
R92 ($\overline{SCK}$)	I/O(I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
RA3 to RA0	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
RB3 to RB0			
RC3 to RC0			
XIN	Input	Resonator connecting pin (High-frequency) . For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	HOLD request/release signal input	Sence input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5 V	
VSS		0 V (GND)	
VAREF		AD converter analog reference voltage (High)	
VASS		AD converter analog reference voltage (Low)	

Operational Description

1. System Configuration

◆ Internal CPU Function

2.1 Program Counter (PC)
2.2 Program Memory (ROM)
2.3 H Register, L Register, and Data Memory Bank Selector (DMB)
2.4 Data Memory (RAM)
- Stack
- Stack Pointer Word (SPW)
- Data Counter (DC)

2.5 Accumulator
2.6 Flags
2.7 Clock Generator, Timing Generator, System Clock Controller
2.8 Interrupt Controller
2.9 Reset Circuit

◆ Peripheral Hardware Function

3.1 Input/Output Ports
3.2 Interval Timer
3.3 Timer / Counters (TC1, TC2)
3.4 Watchdog Timer
3.5 Remote Control Pulse Detector
3.6 AD Converter
3.7 Serial Interface

Concerning the above component parts, the hardware configuration and functions are described.

2. Internal CPU Function

2.1 Program Counter (PC)

The program counter is a 13-bit binary counter which indicates the address of the program memory storing the next instruction to be executed. Normally, the PC is incremented by the number of bytes of the instruction every time it is fetched. When a branch instruction or a subroutine instruction has been executed or an interrupt has been accepted, the specified values listed in Table 2-1 are set to the PC. The PC is initialized to "0" during reset.

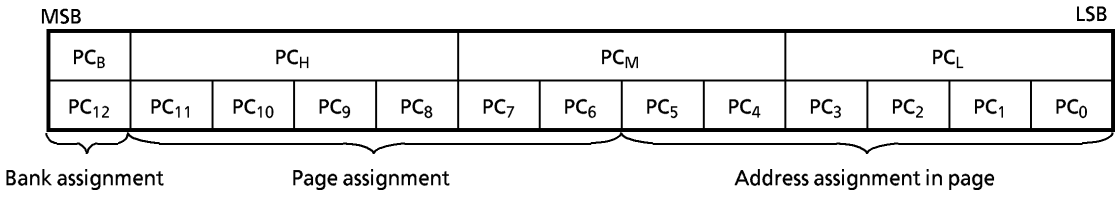


Figure 2-1. Configuration of program counter

The PC can directly address an 8192-byte address space. However, with the short/middle branch and subroutine call instructions, the following points must be considered:

(1) Short branch instruction [BSS a]

In [BSS a] instruction execution, when the branch condition is satisfied the status flag is "1", the value specified in the instruction is set to the lower 6 bits of the PC. That is, [BSS a] becomes the in-page branch instruction. When [BSS a] is stored at the last address of the page, the upper 7 bits of the PC point the next page, so that branch is made to the next page.

(2) Middle branch instruction [BS a]

In [BS a] instruction execution, when the branch condition is satisfied, the value specified in the instruction is set to the lower 12 bits of the PC. That is, [BS a] becomes the in-bank branch instruction.

When first byte or second byte of this instruction is stored at the last address of the bank, the most significant bit of the PC point the next bank, so that branch is made to the next bank.

(3) Subroutine call instruction [CALL a]

In [CALL a] instruction execution, the contents of the PC are saved to the stack then the value specified by the instruction is set to the PC. The address which can be specified by the instruction consists of 11 bits and the upper 2 bits of the PC is always "0". Therefore, the entry address of the subroutine should be within an address range of 0000_H through $07FF_H$.

Table 2-1. Status change of program counter

Instruction or Operation		Condition		Program Counter (PC)
				PC_{12} PC_{11} PC_{10} PC_9 PC_8 PC_7 PC_6 PC_5 PC_4 PC_3 PC_2 PC_1 PC_0
Instruction	BSL a	SF = 1 (Branch condition is satisfied)		Immediata data specified by the instruction
		SF = 0 (Branch condition is not satisfied)		+ 3
	BS a	SF = 1	Lower 12-bit address ≠ FFE, FFF_H	Hold : Immediata data specified by the instruction
			Lower 12-bit address = FFE, FFF_H (Last address in bank)	+ 1 : Immediata data specified by the instruction
		SF = 0		+ 2
	BSS a	SF = 1	Lower 6-bit address ≠ $3F_H$	Hold : Immediata data specified by the instruction
			Lower 6-bit address = $3F_H$ (Last address in page)	+ 1 : Immediata data specified by the instruction
		SF = 0		+ 1
	CALL a			0 0 : Immediata data specified by the instruction
	CALLS a			0 0 0 0 0 : The value generated by the immediate data specified by the instruction : 1 1 0
	RET			The return address restored from stack
	RETI			The return address restored from stack
	Others			Incremented by the number of bytes in the instruction
Interrupt acceptance				0 0 0 0 0 0 0 0 0 : Interrupt vector : 0
Reset				0 0 0 0 0 0 0 0 0 0 0 0 0

2.2 Program Memory (ROM)

Programs and fixed data are stored in the program memory. The instruction to be executed next is read from the address indicated by the contents of the PC. The fixed data can be read by using the table look-up instructions or 5-bit to 8-bit data conversion instruction.

(1) Table look-up instructions [LDL A ,@DC], [LDH A,@DC +]

The table look-up instructions read the lower and upper 4 bits of the fixed data stored at the address specified in the data counter (DC) to place them into the accumulator. [LDL A,@DC] instruction reads the lower 4 bits of fixed data and [LDH A,@DC +] instruction reads the upper 4 bits.The DC is a 12-bit register, and it can specify an address within the range of 1000_H through $1FFF_H$ of the program memory.

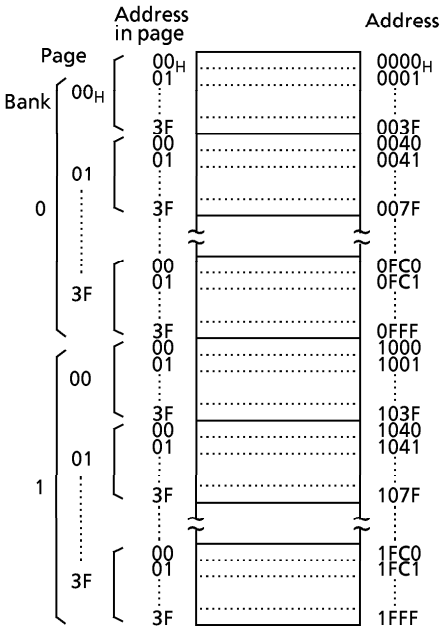


Figure 2-2. Configuration of program memory

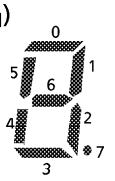
(2) 5-bit to 8-bit data conversion instruction [OUTB @HL]

The 5-bit to 8-bit data conversion instruction reads the fixed data (8 bits) from the data conversion table in the program memory to output the upper 4 bits to port P2 and the lower 4 bits to port P1. The table is located in the last 32-byte space (addresses 17E0 through $17FF_H$ for the TMP47C660A and addresses $1FE0_H$ through $1FFF_H$ for the TMP47C860A) in the program memory with the lower address consisting of the 5 bits obtained by linking the data memory contents specified by the HL register pair and the content of the carry flag.

This instruction is suitable for such applications as converting BCD data into an output code to the 7-segment display elements.

Example: The following shows that the BCD data at address $2F_H$ in data memory is converted into the 7-segment code (anode common LED) to be output to ports P2 and P1.

```
LD      HL,#2FH   ; HL←2FH (Data memory address is set)
TEST    CF        ; CF←0 (The table is specified at addresses 1FE0H - 1FEFH)
OUTB    @HL
  ⋮
ORG     1FE0H     ; Data conversion table
DATA    0C0H,0F9H,0A4H,0B0H,99H,92H,82H,0D8H,80H,98H
```

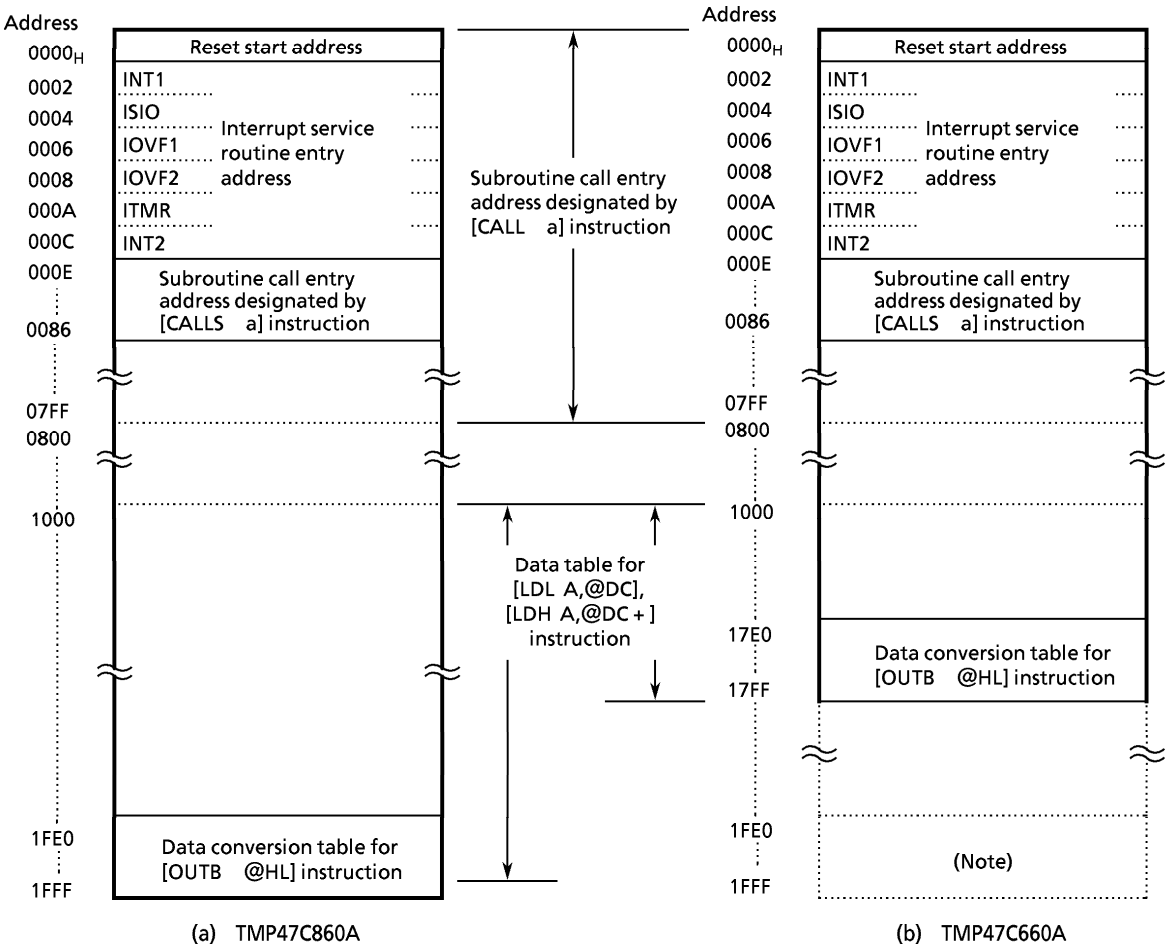


2.2.1 Program memory map

Figure 2-3 shows the program memory map. Address 0000 through 0086_H and 1FE0 through $1FFF_H$ for the TMP47C860A, 0000 through 0086_H and 17E0 through $17FF_H$ for the TMP47C660A, of the program memory are also used for special purposes.

2.2.2 Program memory capacity

The TMP47C860A has 8192 × 8 bits (addresses 0000 through 1FFF$_H$) and the TMP47C660A has 6144 × 8bits (0000 through 17FF$_H$), of the program memory (mask ROM).



Note: In case of the TMP47C660A, 5-bit to 8-bit data conversion table is at address 17E0 through 1FFF$_H$. When the piggyback is used in order to evaluate the TMP47C660A, it is necessary to also place a conversion table at address 1FE0 through 1FFF$_H$ and operation are exactly the same.

Figure 2-3. Program memory map

2.3 H Register, L Register, and Data Memory Bank Selector (DMB)

The H register and the L register are 4-bit general registers. They are also used as a register pair (HL) for the data memory (RAM) addressing pointer. The data memory consists of pages, each page being 16 words long (1 word = 4 bits). The H register specifies a page and the L register specifies an address in the page. The data memory consists of two banks (bank0 and bank1). The data memory bank selector (DMB) is a 1-bit register to specify a data memory bank. During reset, the DMB is initialized to "0". The DMB is set or cleared by the [CLR DMB] or [SET DMB] instructions. The currently selected data memory bank can be known by executing the [TEST DMB] or [TESTP DMB] instruction.

The L register has the automatic post-increment/decrement capability, implementing the execution of composite instructions. For example, [ST A,@HL+] instruction automatically increments the contents of the L register after data transfer. During the execution [SET @L], [CLR @L], or [TEST @L] instruction, the L register is also used to specify the bits corresponding to I/O port pins R73 through R40 (the indirect addressing of port bits by the L register).

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output Current (per 1 pin)	I_{OUT1}	Ports R	3.2	mA
	I_{OUT2}	Ports P1, P2	30	
	I_{OUT3}	Ports P0, P3	15	
Output Current (total)	ΣI_{OUT1}	Ports P0, P1	120	mA
	ΣI_{OUT2}	Ports P2, P3		
Power Dissipation [Topr = 70°C]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 40 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Opeating Conditions (V_{SS} = 0 V, Topr = – 40 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		In the Normal mode	4.5	5.5	V
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz
	fs	XTIN, XTOUT		30	34	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Input voltage V_{IH3}, V_{IL3}: In the SLOW or HOLD mode.

DC Characteristics

(V_{SS} = 0 V, Topr = – 40 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	—	—	± 2	μA
	I_{IN2}	Ports R (open drain)					
Low Input Current	I_{IL}	Ports R (push-pull)	V_{DD} = 5.5 V, V_{IN} = 0.4 V	—	—	– 2	mA
Input Resistance	R_{IN1}	Port KO with pull-up/pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports (open drain)	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
Output High Voltage	V_{OH}	Ports (push-pull)	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	—	—	V
Output Low Voltage	V_{OL}	Except XOUT, ports P	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	
Output Low Current	I_{OL2}	Ports P1, P2	V_{DD} = 4.5 V, V_{OL} = 1.0 V	—	30	—	mA
	I_{OL3}	Ports P0, P3		—	13	—	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5 V fc = 4 MHz	—	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0 V fs = 32.768 kHz	—	30	60	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5 V	—	0.5	10	μA

Note 1: Typ. values show those at T_{opr} = 25°C, V_{DD} = 5 V.

Note 2: Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3: Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3 V / 0.2 V
The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.
Supply Current I_{DDS} ; V_{IN} = 2.8 V /0.2 V
Low frequency clock is only osillated (connecting XTIN, XTOUT).

AD Conversion Characteristics

(Topr = – 40 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	—	V_{DD}	V
	V_{ASS}		V_{SS}	—	1.5	
Analog Reference Voltage Range	$_{\Delta}V_{AREF}$	$V_{AREF} - V_{ASS}$	2.5	—	—	V
Analog Input Voltage	V_{AIN}		V_{ASS}	—	V_{AREF}	V
Analog Supply Current	I_{REF}		—	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 4.5 to 5.5 V, V_{SS} = 0.0 V V_{AREF} = V_{DD} ± 0.001 V V_{ASS} = 0.000 V	—	—	± 1	LSB
Zero Point Error			—	—	± 1	
Full Scale Error			—	—	± 1	
Total Error			—	—	± 2	

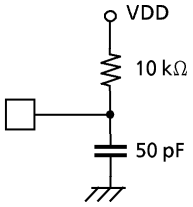
AC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 40 to 70°C)

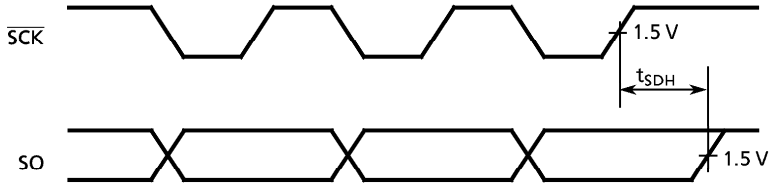
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Instruction Cycle Time	tcy	In the Normal mode	1.3	—	20	ns
		In the SLOW mode	235	—	267	
High level Clock pulse Width	t_{WCH}	External clock mode	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
AD Sampling Time	t_{AIN}	fc = 4 MHz	—	4	—	μs
Shift Data Hold Time	t_{SDH}		0.5 tcy – 0.3	—	—	μs

Note: Shift Data Hold Time

External circuit for $\overline{SCK}$ pin and SO pin



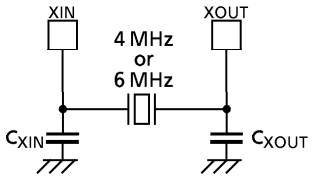
Serial port (completion of transmission)



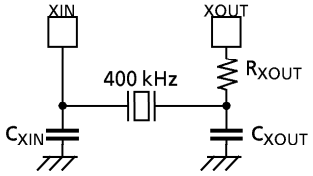
Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 40 to 70°C)

(1) 6 MHz
Ceramic Resonator
CSA6.00MGU (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF
KBR-6.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF

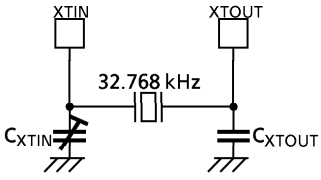


(2) 4 MHz
Ceramic Resonator
CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF
KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF
Crystal Oscillator
204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20 pF



(3) 400 kHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220 pF, R_{XOUT} = 6.8 kΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100 pF, R_{XOUT} = 10 kΩ

(4) 32.768 kHz (V_{SS} = 0 V, V_{DD} = 2.7 to 6.0V, Topr = – 30 to 70°C)
Crystal Oscillator C_{XTIN}, C_{XTOUT} ; 10 to 33 pF



Note: In order to get the accurate oscillation frequency, the adjustment of capacitors must be required.

Typical Characteristics