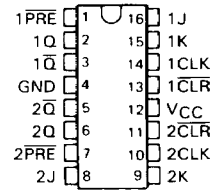
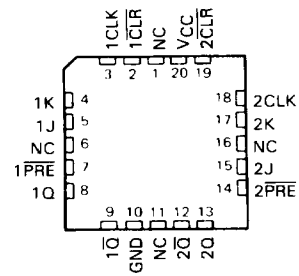
TI0103—D3339, JUNE 1989—REVISED JANUARY 1990

- **Inputs are TTL-Voltage Compatible**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11112 . . . J PACKAGE
74ACT11112 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11112 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The 54ACT11112 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11112 is characterized for operation from −40°C to 85°C.

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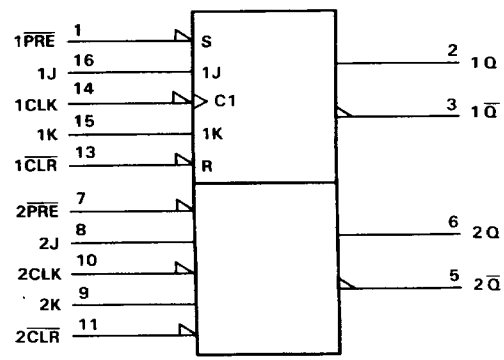
FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

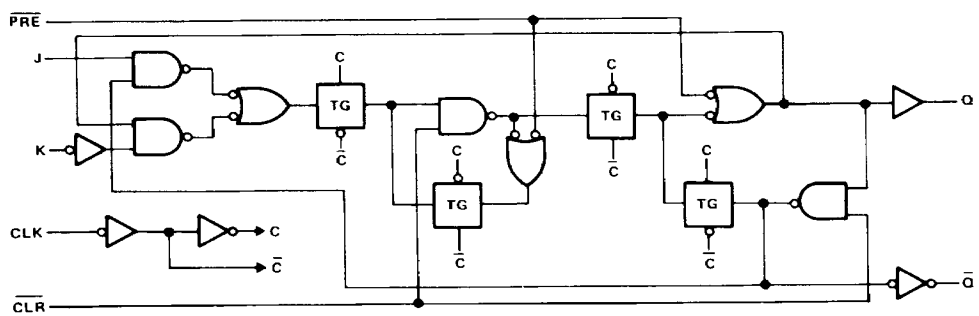
† This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to the inactive (high) level.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (each flip-flop) (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($VO = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11112		74ACT11112		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11112		74ACT11112		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡	V_I = V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This parameter is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER			T_A = 25°C		54ACT11112		74ACT11112		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			125		125		125	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4		4		4		ns
		CLK low or high	4		4		4		
t_{su}	Setup time, data before CLK ↓	Data high or low	3.5		3.5		4.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2		2		2		
t_h	Hold time, data after CLK ↓		1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11112		74ACT11112		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125			125		125		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.5	3.6	6.3	1.5	7.1	1.5	6.8	ns
t_{PHL}			1.5	4.6	7.4	1.5	8.4	1.5	8	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	4.2	7	1.5	8	1.5	7.7	ns
t_{PHL}			1.5	4.7	7.4	1.5	8.9	1.5	8.4	

C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF, f = 1 MHz, T_A = 25°C	39	pF

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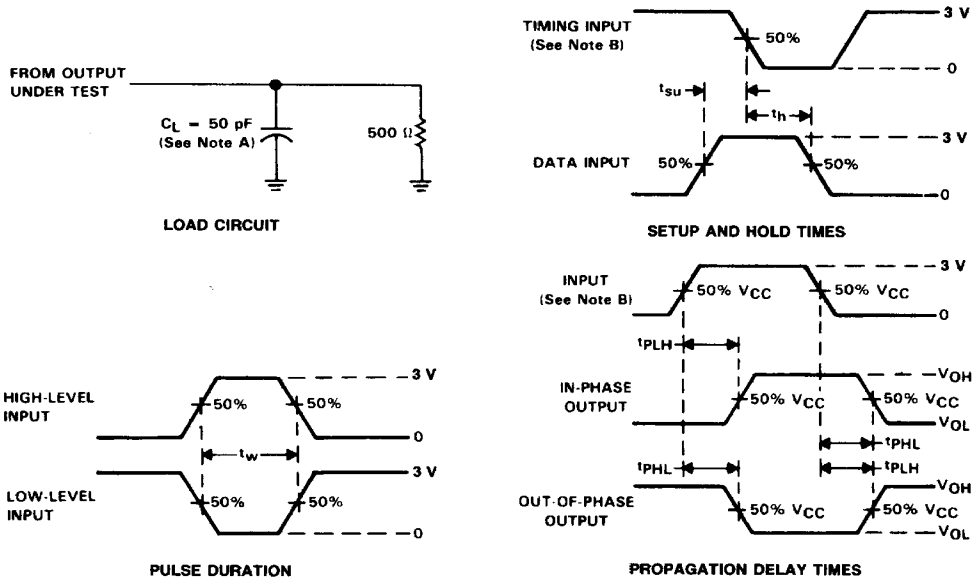
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing f_{max} and pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS