

74H Series TTL (High-Speed)

The gates, inverters and expanders in the 74H series are high speed versions of the similarly numbered devices in National's standard TTL family (Series 74). The two series are completely compatible, being specified to the same voltages and temperature range (0°C to 70°C). They can be used in combination, with Series 74H circuits located wherever minimum propagation delays are needed. Each Series 74H input has a maximum current flow of 2mA out of the input at logical "0" voltage and a maximum current flow into the input of 50µA at logical "1" voltage. Each Series 74H gate output is specified to drive 10 such loads and has a current sink capability of 20mA. Typical power dissipation per NAND gate is 23mW at 50% duty cycle. Open-collector gates have a fanout of 10 when not wire-OR'd and a fanout up to 9 when wire-OR'd. The output is connected to V_{CC} through an external load resistor. Value of the load resistor is calculated by the same method used for Series 74 open-collector devices, except that the input and sink currents given above are substituted for the Series 74 current values.

To maintain optimum switching times and noise immunity, unused inputs should receive current at the logical "1" level (except that unused expander inputs should be left open). The unused inputs may be connected to used inputs on the same gate provided the fanout of the driving output is not exceeded. Unused inputs may also be connected to V_{CC}, if a resistor is placed in the supply line to protect the inputs from transients above 5.5V. Up to 25 inputs may be connected through a 1-kilohm resistor. Or, the unused inputs may be connected to an independent supply, preferably 2.4 to 3.5V.

FEATURES

Typical gates delay down to 6ns.

Typical DC noise margin of 1V.

Low susceptibility to AC noise.

Minimum output short-circuit current of -40mA for gates.

Higher source and sink currents than standard TTL.

Fanout of 10 Series 74H loads or 12 Series 74 loads.

Waveform integrity over full load and temperature range.

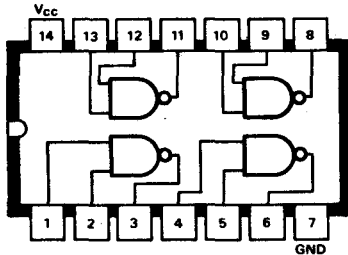
AND gates and open-collector gates available.

REFERENCE TABLE See outline drawings Nos. 109, 111 and 114 for physical dimensions.

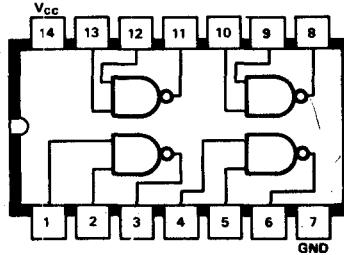
Code	Function	Stock No.	Connection Drawing No.
DM74H00N	Quad 2 NAND Gate	30616E	B1
DM74H01N	Quad 2 NAND Gate (Open Collector)	30617C	B2
DM74H04N	Hex Inverter	30618A	B5
DM74H05N	Hex Inverter (Open Collector)	31619X	B6
DM74H08N	Quad 2 AND Gate	30620B	B9
DM74H10N	Triple 3 NAND Gate	30621X	B11
DM74H11N	Triple 3 AND GATE	30622R	B12
DM74H20N	Dual 4 NAND Gate	30623G	B19
DM74H21N	Dual 4 AND Gate	29726B	B20
DM74H22N	Dual 4 NAND Gate (Open Collector)	30635X	B21
DM74H30N	Eight Input NAND Buffer	30624E	B26
DM74H40N	Dual 4 NAND Buffer	30625C	B31
DM74H50N	Exp Dual 2-Input AND OR INVERT Gate	30626A	B40
DM74H51N	Dual 2-Input AND OR Invert Gate	30627X	B41
DM74H52N	Exp 2-2-2-3-Input AND OR Gate	31048X	B42
DM74H53N	Exp 4 2-2-2-3 AND OR INVERT Gate	30628H	B43
DM74H54N	2-2-2-3-AND OR Invert Gate	30629F	B44
DM74H55N	Exp 4-Input AND OR INVERT Gate	30630R	B45
DM74H60N	Dual 4 Expander	30631G	B46
DM74H61N	Triple 3 Expander	30636H	B47
DM74H62N	3-2-2-3 Expander	30632E	B48
DM74H71N	J-K Flip-Flop (Master/Slave)	31321A	B52
DM74H72N	J-K Flip-Flop (Master/Slave)	30633C	B53
DM74H73N	Dual J-K Flip-Flop (Master/Slave)	31322X	B54
DM74H74N	Dual D Flip-Flop	30634A	B55
DM74H76N	Dual J-K Flip-Flop (Master/Slave)	31323H	B57
DM74H78N	Dual J-K Flip-Flop (Master/Slave)	31324F	B58
DM74H106N	Dual J-K Flip-Flop	33267X	B79
DM74H108N	Dual J-K Flip-Flop	33268R	B81

MANUFACTURER'S CURRENT LIST PRICES ARE ALWAYS CHARGED

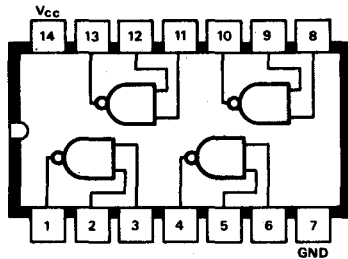
B1 SN7400N/AN
SN74H00N/SN74S00N
SN74L00N/SN74C00N
 Quad 2-input NAND gate



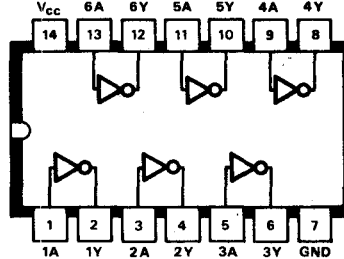
B4 SN7403N/AN
SN74S03N/SN74L03N
 Quad 2-input NAND gate
 with open collector output



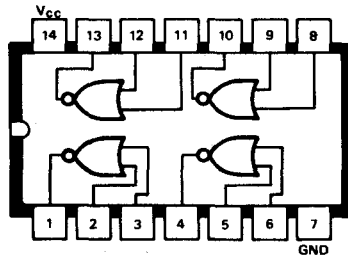
B2 SN7401N/AN
SN74H01N
 Quad 2-input NAND gate
 with open collector output



B5 SN7404N
SN74H04N/SN74S04N
SN74L04N/SN74C04N
 Hex Inverter



B3 SN7402N
SN74L02N/SN74C02N
 Quad 2-input NOR gate



B6 SN7405N/AN
SN74H05N/SN74S05N
 Hex Inverter
 with open collector output

