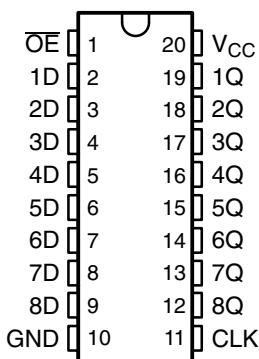


# SN54LVC574A, SN74LVC574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

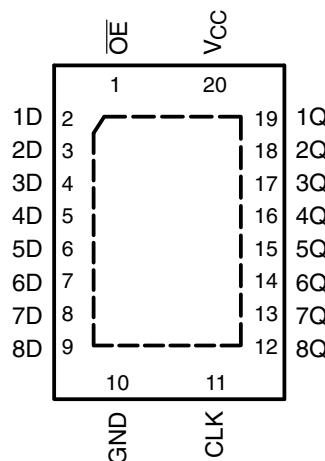
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- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Specified From -40°C to 85°C, -40°C to 125°C, and -55°C to 125°C
- Max  $t_{pd}$  of 7 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

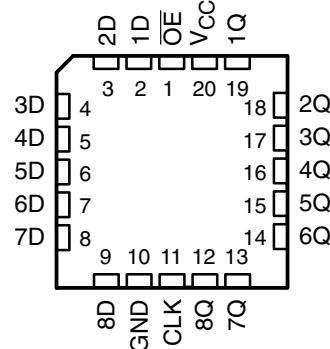
SN54LVC574A . . . J OR W PACKAGE  
SN74LVC574A . . . DB, DGV, DW, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LVC574A . . . RGY PACKAGE  
(TOP VIEW)



SN54LVC574A . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

The SN54LVC574A octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC574A octal edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested  
unless otherwise noted. On all other products, production  
processing does not necessarily include testing of all parameters.

**SN54LVC574A, SN74LVC574A  
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**description/ordering information (continued)**

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

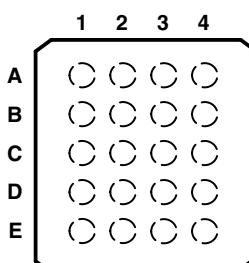
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

**ORDERING INFORMATION**

$T_A$	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC574ARGYR	LC574A
	VFBGA – GQN	Reel of 1000	SN74LVC574AGQNR	LC574A
	VFBGA – ZQN (Pb-free)		SN74LVC574AZQNR	
-40°C to 125°C	PDIP – N	Tube of 20	SN74LVC574AN	SN74LVC574AN
	SOIC – DW	Tube of 25	SN74LVC574ADW	LVC574A
		Reel of 2000	SN74LVC574ADWR	
	SOP – NS	Reel of 2000	SN74LVC574ANSR	LVC574A
	SSOP – DB	Reel of 2000	SN74LVC574ADBR	LC574A
	TSSOP – PW	Tube of 70	SN74LVC574APW	LC574A
		Reel of 2000	SN74LVC574APWR	
		Reel of 250	SN74LVC574APWT	
-55°C to 125°C	TVSOP – DGV	Reel of 2000	SN74LVC574ADGVR	LC574A
	CDIP – J	Tube of 20	SNJ54LVC574AJ	SNJ54LVC574AJ
	CFP – W	Tube of 85	SNJ54LVC574AW	SNJ54LVC574AW
	LCCC – FK	Tube of 55	SNJ54LVC574AFK	SNJ54LVC574AFK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**GQN OR ZQN PACKAGE  
(TOP VIEW)**



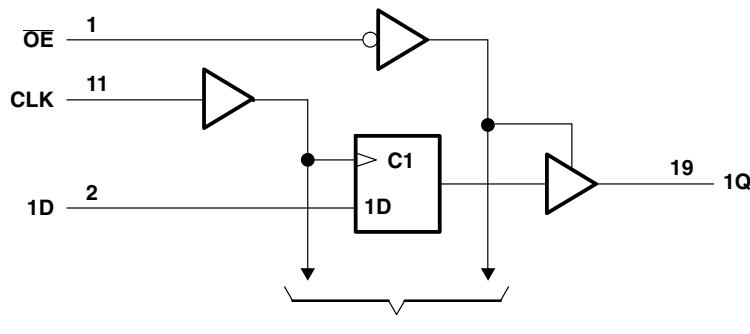
**terminal assignments**

	1	2	3	4
A	1D	$\overline{OE}$	$V_{CC}$	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	CLK	8Q

**FUNCTION TABLE  
(each flip-flop)**

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

## logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, EK, J, N, NS, PW, BGY, and W packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed. 2. The value of  $V_{CC}$  is provided in the recommended operating conditions table. 3. The package thermal impedance is calculated in accordance with JESD 51-7. 4. The package thermal impedance is calculated in accordance with JESD 51-5. 5. For the DW package: above 70°C the value of  $P_{tot}$  derates linearly with 8 mW/K. 6. For the DB, DGV, N, NS, and PW packages: above 60°C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

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WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 7)**

				<b>SN54LVC574A</b>	<b>UNIT</b>
				<b>-55 TO 125°C</b>	
				<b>MIN</b> <b>MAX</b>	
$V_{CC}$	Supply voltage		Operating	2    3.6	$V$
			Data retention only	1.5	
$V_{IH}$	High-level input voltage		$V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$	2	$V$
$V_{IL}$	Low-level input voltage		$V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$	0.8	$V$
$V_I$	Input voltage			0    5.5	$V$
$V_O$	Output voltage		High or low state	0 $V_{CC}$	$V$
			3-state	0    5.5	
$I_{OH}$	High-level output current		$V_{CC} = 2.7\text{ V}$	-12	$mA$
			$V_{CC} = 3\text{ V}$	-24	
$I_{OL}$	Low-level output current		$V_{CC} = 2.7\text{ V}$	12	$mA$
			$V_{CC} = 3\text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate			6	$ns/V$

NOTE 7: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**recommended operating conditions (see Note 7)**

		<b>SN74LVC574A</b>						<b>UNIT</b>	
		$T_A = 25^\circ\text{C}$		$-40\text{ TO }85^\circ\text{C}$		$-40\text{ TO }125^\circ\text{C}$			
		<b>MIN</b>	<b>MAX</b>	<b>MIN</b>	<b>MAX</b>	<b>MIN</b>	<b>MAX</b>		
$V_{CC}$	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	
		Data retention only	1.5		1.5		1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65\text{ V}$ to $1.95\text{ V}$	$0.65 \times V_{CC}$	$0.65 \times V_{CC}$	$0.65 \times V_{CC}$			$V$	
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	1.7	1.7	1.7	1.7			
		$V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$	2	2	2	2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65\text{ V}$ to $1.95\text{ V}$	$0.35 \times V_{CC}$	$0.35 \times V_{CC}$	$0.35 \times V_{CC}$	$0.35 \times V_{CC}$		$V$	
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	0.7	0.7	0.7	0.7			
		$V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$	0.8	0.8	0.8	0.8			
$V_I$	Input voltage	0	5.5	0	5.5	0	5.5	$V$	
$V_O$	Output voltage	High or low state	0	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$	
		3-state	0	5.5	0	5.5	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 1.65\text{ V}$	-4	-4	-4	-4		$mA$	
		$V_{CC} = 2.3\text{ V}$	-8	-8	-8	-8			
		$V_{CC} = 2.7\text{ V}$	-12	-12	-12	-12			
		$V_{CC} = 3\text{ V}$	-24	-24	-24	-24			
$I_{OL}$	Low-level output current	$V_{CC} = 1.65\text{ V}$	4	4	4	4		$mA$	
		$V_{CC} = 2.3\text{ V}$	8	8	8	8			
		$V_{CC} = 2.7\text{ V}$	12	12	12	12			
		$V_{CC} = 3\text{ V}$	24	24	24	24			
$\Delta t/\Delta v$	Input transition rise or fall rate	6		6		6		$ns/V$	

NOTE 7: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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**SN54LVC574A, SN74LVC574A**  
**OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC574A			UNIT	
			-55 TO 125°C				
			MIN	TYP <sup>†</sup>	MAX		
V <sub>OH</sub>	I <sub>OH</sub> = -100 µA	2.7 V to 3.6 V	V <sub>CC</sub> - 0.2			V	
	I <sub>OH</sub> = -12 mA	2.7 V	2.2				
	I <sub>OH</sub> = -24 mA	3 V	2.4				
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	2.7 V to 3.6 V		0.2		V	
	I <sub>OL</sub> = 12 mA	2.7 V		0.4			
	I <sub>OL</sub> = 24 mA	3 V		0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V		±5	µA		
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V	3.6 V		±15	µA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0	3.6 V		10	µA	
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>‡</sup>				10		
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND		2.7 V to 3.6 V		500	µA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		4	pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V		5.5	pF	

<sup>†</sup> T<sub>A</sub> = 25°C

<sup>‡</sup> This applies in the disabled state only.

**SN54LVC574A, SN74LVC574A  
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN74LVC574A						UNIT	
			T <sub>A</sub> = 25°C			-40 TO 85°C		-40 TO 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 µA	1.65 V to 3.6 V	V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2				V
	I <sub>OH</sub> = -4 mA	1.65 V	1.29			1.2		1.2		
	I <sub>OH</sub> = -8 mA	2.3 V	1.9			1.7		1.7		
	I <sub>OH</sub> = -12 mA	2.7 V	2.2			2.2		2.2		
	I <sub>OH</sub> = -24 mA	3 V	2.4			2.4		2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	1.65 V to 3.6 V		0.1		0.2		0.2		V
	I <sub>OL</sub> = 4 mA	1.65 V		0.24		0.45		0.45		
	I <sub>OL</sub> = 8 mA	2.3 V		0.3		0.7		0.7		
	I <sub>OL</sub> = 12 mA	2.7 V		0.4		0.4		0.4		
	I <sub>OL</sub> = 24 mA	3 V		0.55		0.55		0.55		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V		±1		±5		±5	µA	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0		±4		±10		±10	µA	
I <sub>OZ</sub>	V <sub>I</sub> = 0 to 5.5 V	3.6 V		±1		±10		±10	µA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V		1.5		10		10	µA	
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>†</sup>			1.5		10		10		
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V		500		500		500	µA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		4					pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		5.5					pF	

<sup>†</sup> This applies in the disabled state only.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

			V <sub>CC</sub>	SN54LVC574A		UNIT		
				-55 TO 125°C				
				MIN	MAX			
f <sub>clock</sub>	Clock frequency		2.7 V		150	MHz		
			3.3 V ± 0.3 V		150			
t <sub>w</sub>	Pulse duration, CLK high or low		2.7 V		3.3	ns		
			3.3 V ± 0.3 V		3.3			
t <sub>su</sub>	Setup time, data before CLK↑		2.7 V		2	ns		
			3.3 V ± 0.3 V		2			
t <sub>h</sub>	Hold time, data after CLK↑		2.7 V		2	ns		
			3.3 V ± 0.3 V		2			

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**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN54LVC574A		UNIT	
				-55 TO 125°C			
				MIN	MAX		
f <sub>max</sub>			2.7 V	150		MHz	
				3.3 V ± 0.3 V	150		
t <sub>pd</sub>	CLK	Q	2.7 V	8		ns	
				3.3 V ± 0.3 V	1 7		
t <sub>en</sub>	OE	Q	2.7 V	9		ns	
				3.3 V ± 0.3 V	1 7.5		
t <sub>dis</sub>	OE	Q	2.7 V	7		ns	
				3.3 V ± 0.3 V	0.5 6.4		

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		V <sub>CC</sub>	SN74LVC574A						UNIT	
			T <sub>A</sub> = 25°C			-40 TO 85°C		-40 TO 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	1.8 V ± 0.15 V		55		55		40		MHz
		2.5 V ± 0.2 V		95		95		80		
		2.7 V		150		150		150		
		3.3 V ± 0.3 V		150		150		150		
t <sub>w</sub>	Pulse duration, CLK high or low	1.8 V ± 0.15 V	9		9	9		9		ns
		2.5 V ± 0.2 V	4		4	4		4		
		2.7 V	3.3		3.3	3.3		3.3		
		3.3 V ± 0.3 V	3.3		3.3	3.3		3.3		
t <sub>su</sub>	Setup time, data before CLK↑	1.8 V ± 0.15 V	6		6	6		6		ns
		2.5 V ± 0.2 V	4		4	4		4		
		2.7 V	2		2	2		2		
		3.3 V ± 0.3 V	2		2	2		2		
t <sub>h</sub>	Hold time, data after CLK↑	1.8 V ± 0.15 V	4		4	4		4		ns
		2.5 V ± 0.2 V	2		2	2		2		
		2.7 V	1.5		1.5	1.5		1.5		
		3.3 V ± 0.3 V	1.5		1.5	1.5		1.5		

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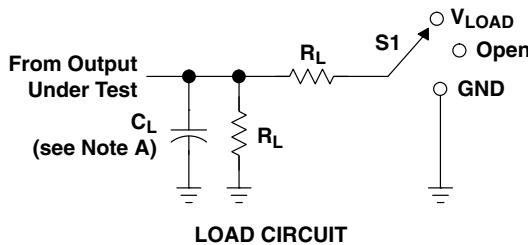
**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN74LVC574A						UNIT	
				T <sub>A</sub> = 25°C			-40 TO 85°C		-40 TO 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			1.8 V ± 0.15 V	55			55		40	MHz	
			2.5 V ± 0.2 V	95			95		80		
			2.7 V	150			150		150		
			3.3 V ± 0.3 V	150			150		150		
t <sub>pd</sub>	CLK	Q	1.8 V ± 0.15 V	1.0	7.1	21.5	1	21.6	1.0	21.6	ns
			2.5 V ± 0.2 V	1.0	4.9	10.0	1	10.5	1.0	10.5	
			2.7 V	1.0	5.0	7.8	1	8	1.0	8.0	
			3.3 V ± 0.3 V	2.2	4.6	6.8	2.2	7	2.2	7.0	
t <sub>en</sub>	OE	Q	1.8 V ± 0.15 V	1.0	6.6	19.0	1	19.5	1.0	19.5	ns
			2.5 V ± 0.2 V	1.0	4.8	10.0	1	10.5	1.0	10.5	
			2.7 V	1.0	5.5	8.3	1	8.5	1.0	8.5	
			3.3 V ± 0.3 V	1.5	4.4	7.3	1.5	7.5	1.5	7.5	
t <sub>dis</sub>	OE	Q	1.8 V ± 0.15 V	1.0	5.4	18.3	1	18.8	1.0	18.8	ns
			2.5 V ± 0.2 V	1.0	3.0	7.3	1	7.8	1.0	7.8	
			2.7 V	1.0	4.0	6.8	1	7	1.0	7.3	
			3.3 V ± 0.3 V	1.7	3.9	6.2	1.7	6.4	1.7	6.6	
t <sub>sk(o)</sub>			3.3 V ± 0.3 V				1		1	ns	

**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER				TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT	
C <sub>pd</sub>	Power dissipation capacitance per flip-flop	Outputs enabled	f = 10 MHz	1.8 V	25		pF	
				2.5 V	29			
				3.3 V	30			
		Outputs disabled		1.8 V	9			
				2.5 V	9			
				3.3 V	11			

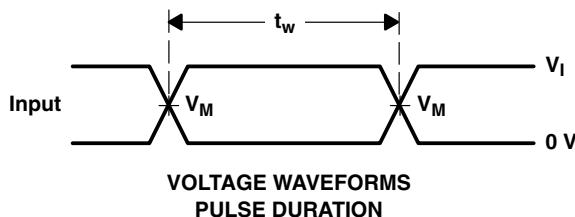
PARAMETER MEASUREMENT INFORMATION



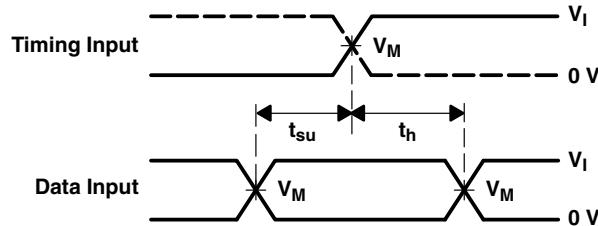
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

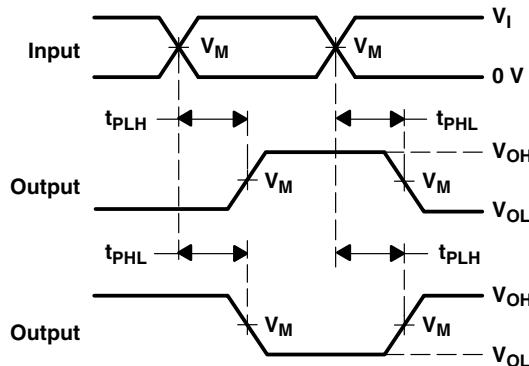
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_\Delta$
	$V_I$	$t_r/t_f$					
$1.8 V \pm 0.15 V$	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 V \pm 0.2 V$	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3 V \pm 0.3 V$	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



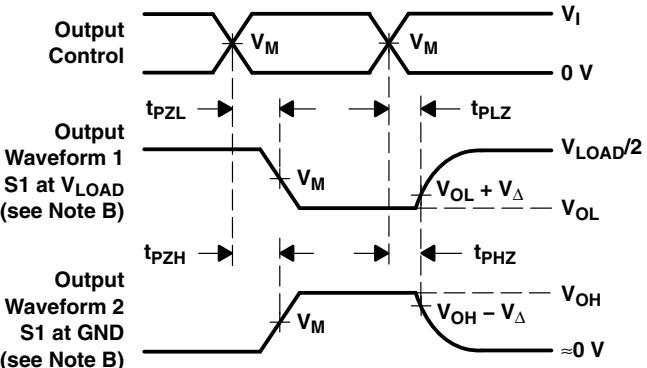
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50 \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

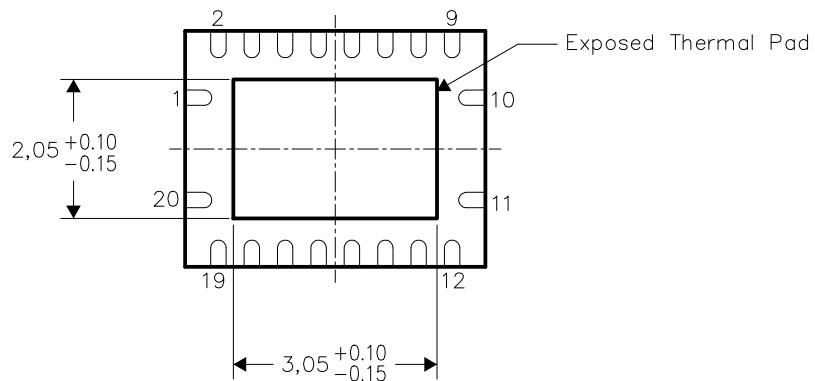
Figure 1. Load Circuit and Voltage Waveforms

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9757601Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9757601Q2A SNJ54LVC574AFK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9757601QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9757601QR A SNJ54LVC574AJ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9757601QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9757601QS A SNJ54LVC574AW	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ADBLE	OBsolete	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVC574ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC574AGQNR	OBsolete	BGA MICROSTAR JUNIOR	GQN	20		TBD	Call TI	Call TI	-40 to 85	LC574A	
SN74LVC574AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LVC574AN	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LVC574AN	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574APWLE	OBsolete	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVC574APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC574ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC574AZQNR	ACTIVE	BGA MICROSTAR JUNIOR	ZQN	20	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LC574A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LVC574AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9757601Q2A SNJ54LVC 574AFK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LVC574AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9757601QR A SNJ54LVC574AJ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LVC574AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9757601QS A SNJ54LVC574AW	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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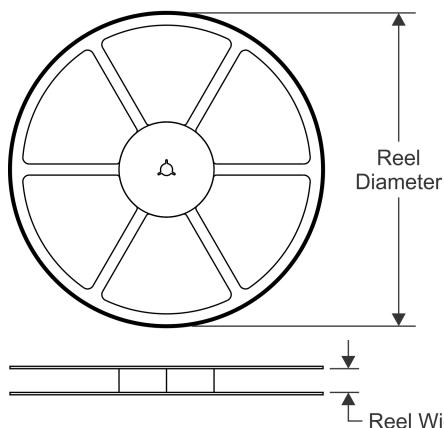
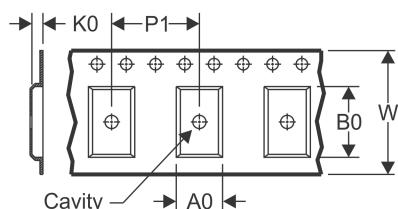
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC574A, SN74LVC574A :**

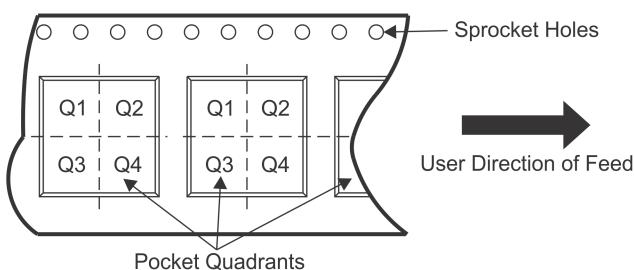
- Catalog: [SN74LVC574A](#)
- Automotive: [SN74LVC574A-Q1](#), [SN74LVC574A-Q1](#)
- Enhanced Product: [SN74LVC574A-EP](#), [SN74LVC574A-EP](#)
- Military: [SN54LVC574A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC574ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC574ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC574ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVC574ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LVC574APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC574APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC574APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC574APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC574ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN74LVC574AZQNR	BGA MI CROSTA R JUNI OR	ZQN	20	1000	330.0	12.4	3.3	4.3	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

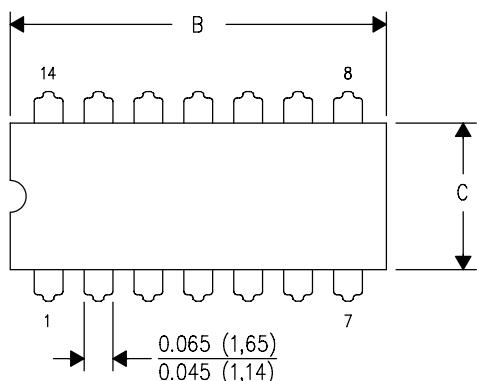

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC574ADBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LVC574ADGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74LVC574ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVC574ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVC574APWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LVC574APWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LVC574APWRG4	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LVC574APWT	TSSOP	PW	20	250	367.0	367.0	38.0
SN74LVC574ARGYR	VQFN	RGY	20	3000	367.0	367.0	35.0
SN74LVC574AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	338.1	338.1	20.6

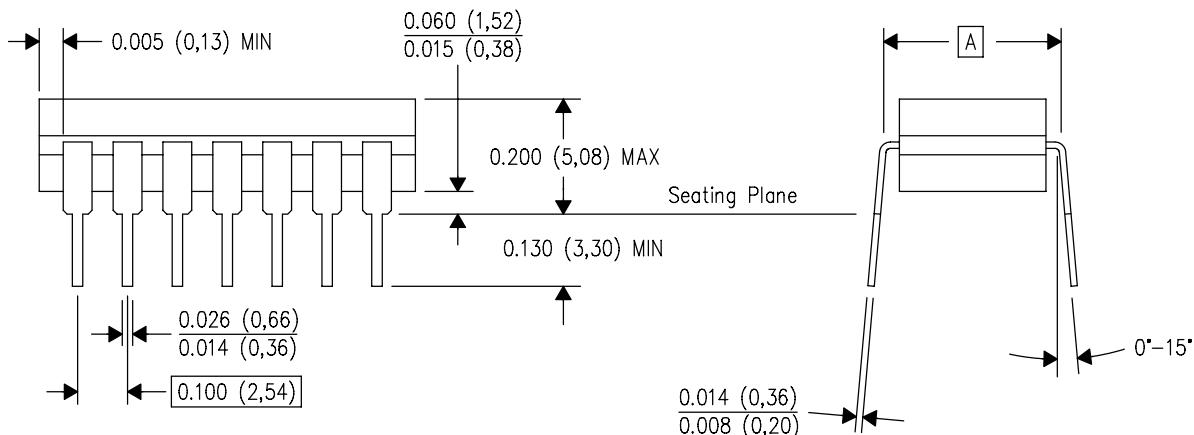
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

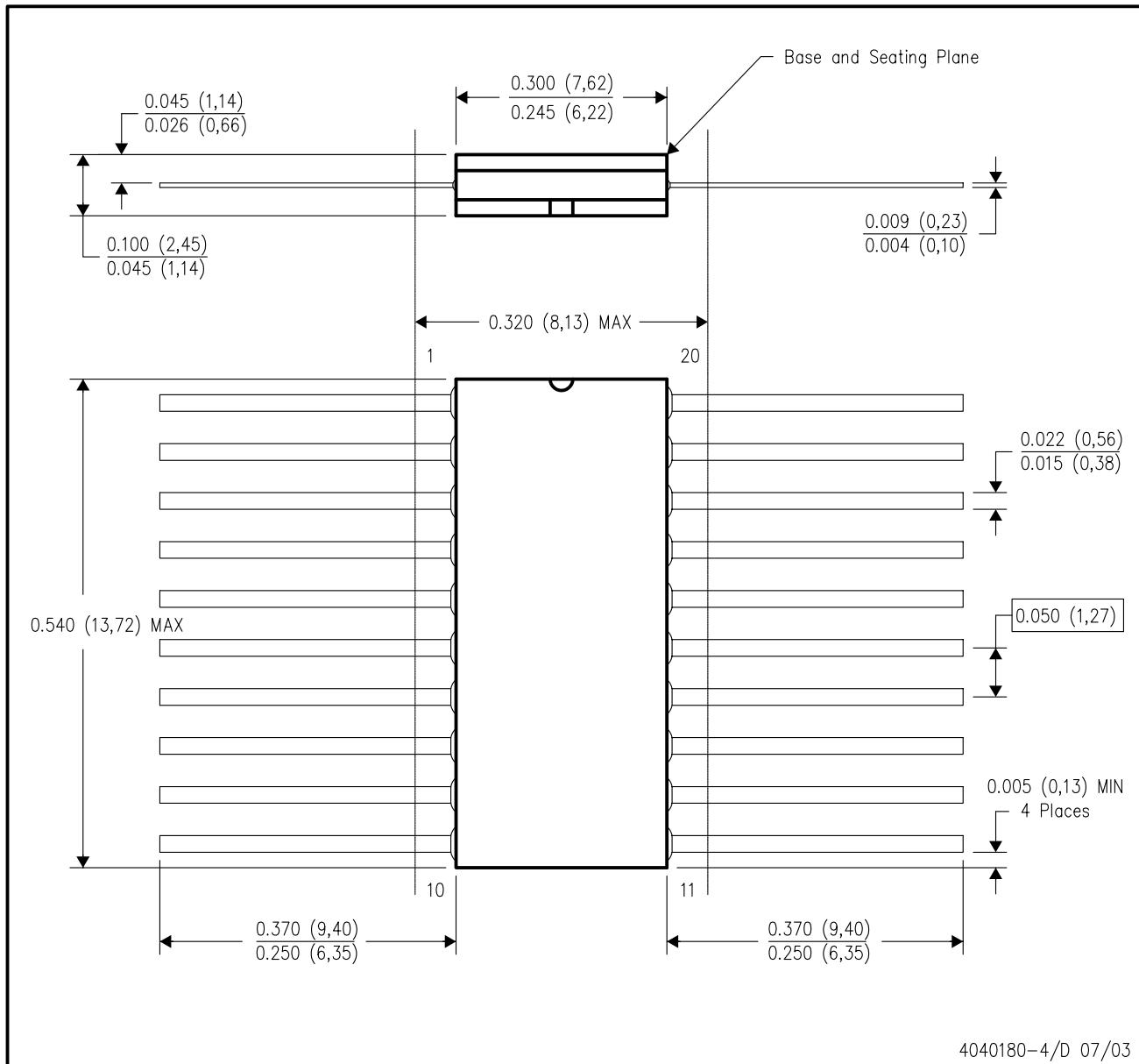


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



4040180-4/D 07/03

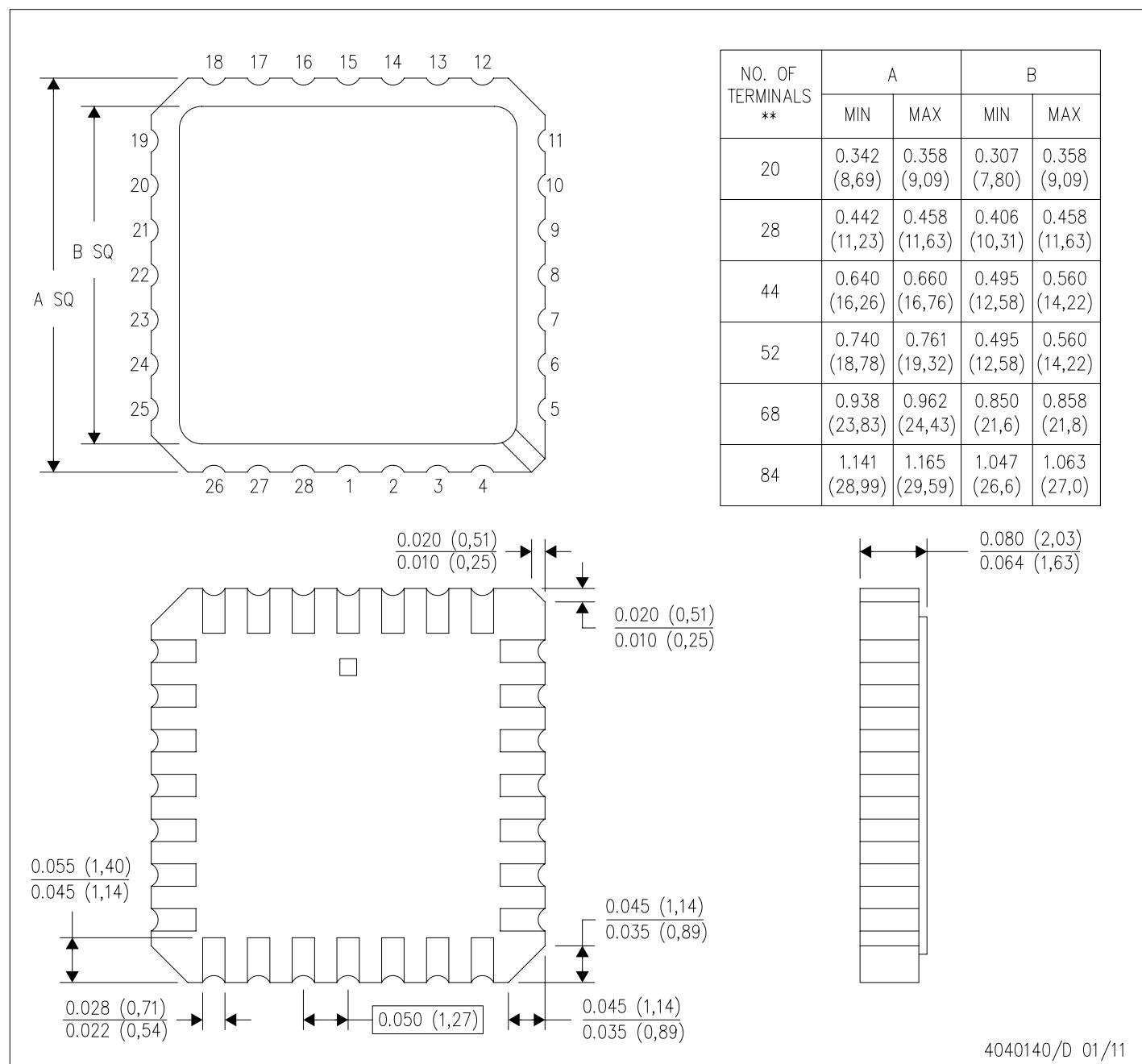
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



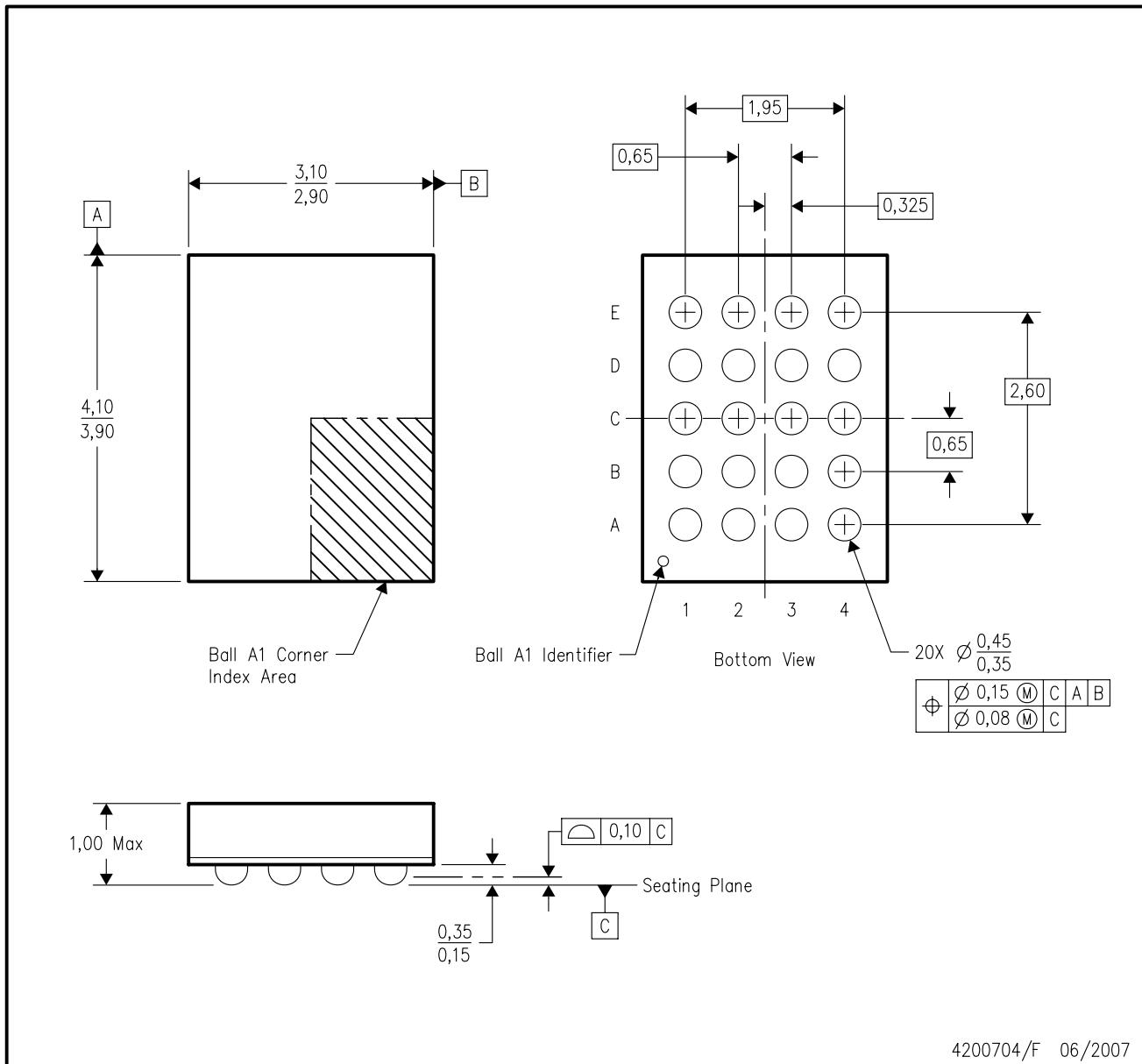
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a metal lid.
- Falls within JEDEC MS-004

4040140/D 01/11

## GQN (R-PBGA-N20)

## PLASTIC BALL GRID ARRAY



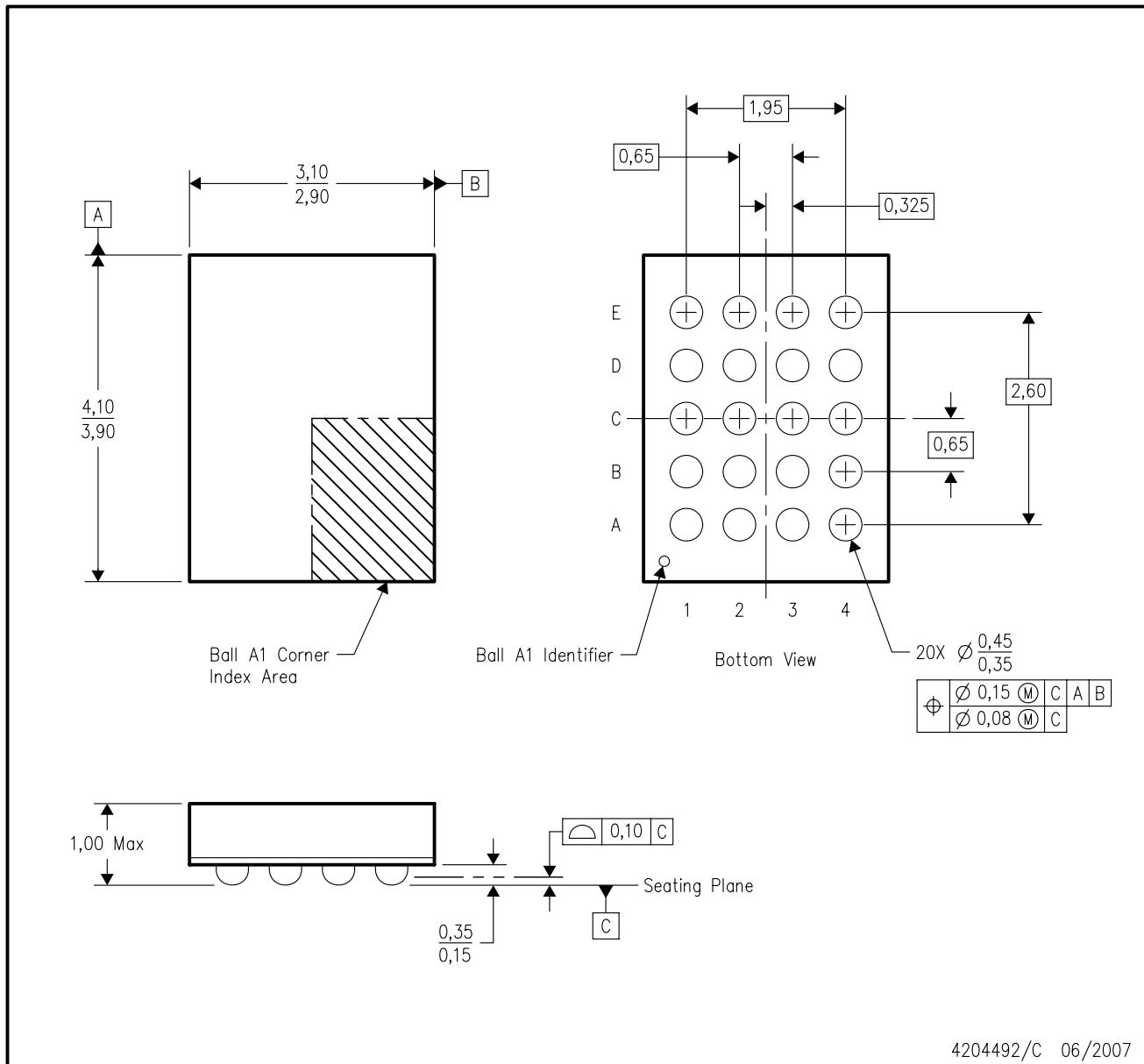
4200704/F 06/2007

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-285 variation BC-2.
- This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

## ZQN (R-PBGA-N20)

## PLASTIC BALL GRID ARRAY



4204492/C 06/2007

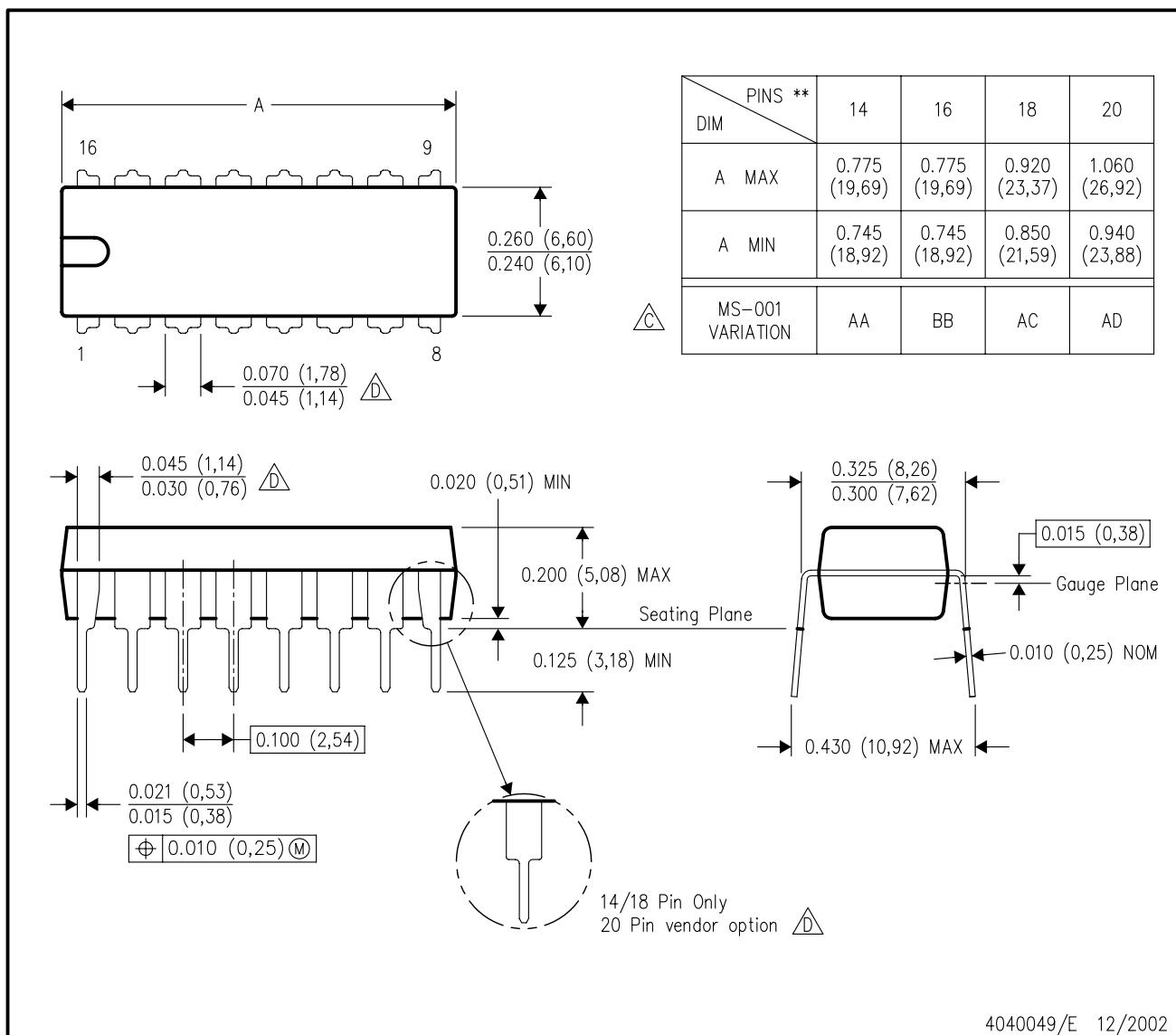
NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-285 variation BC-2.
- This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

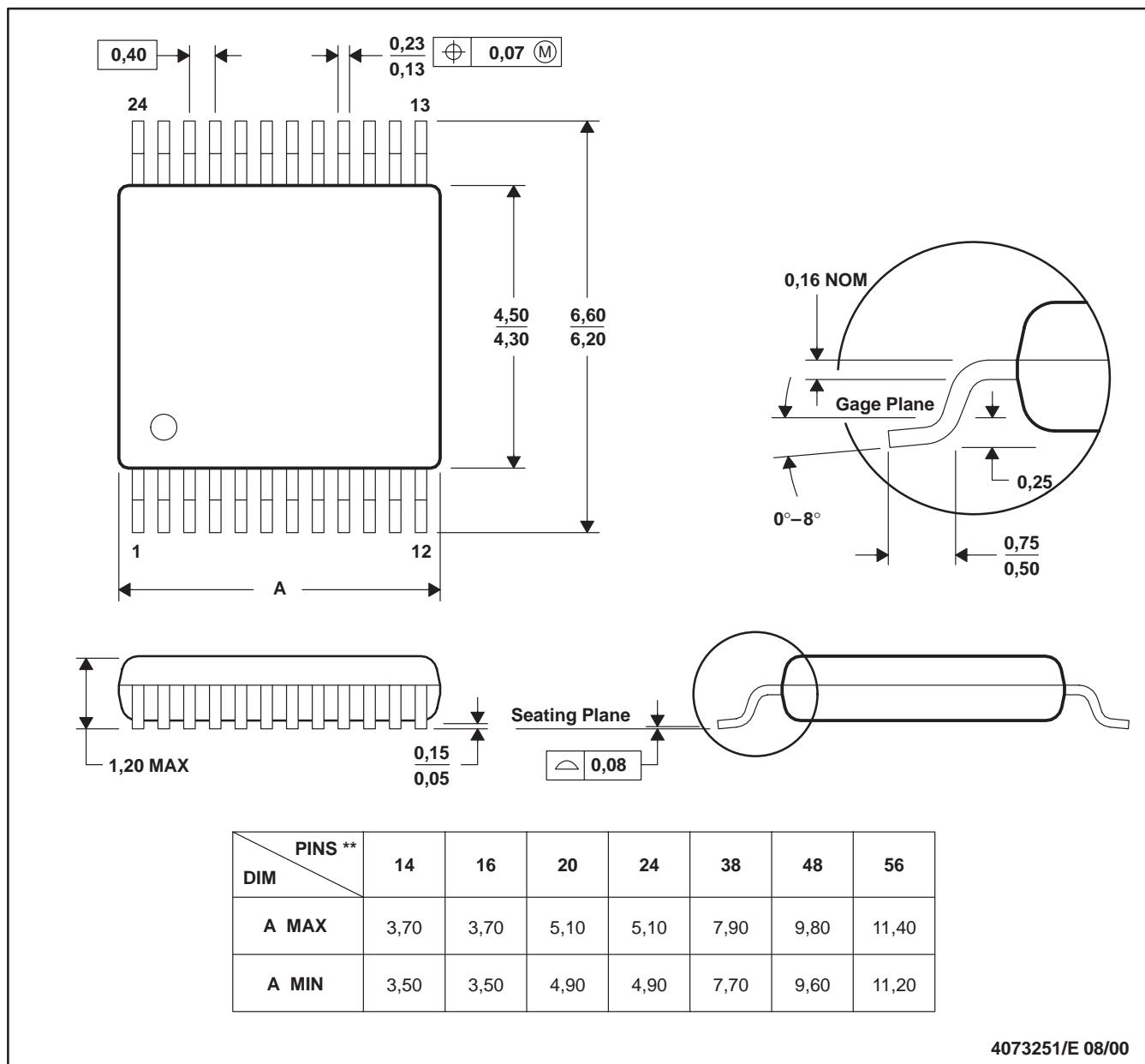
△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

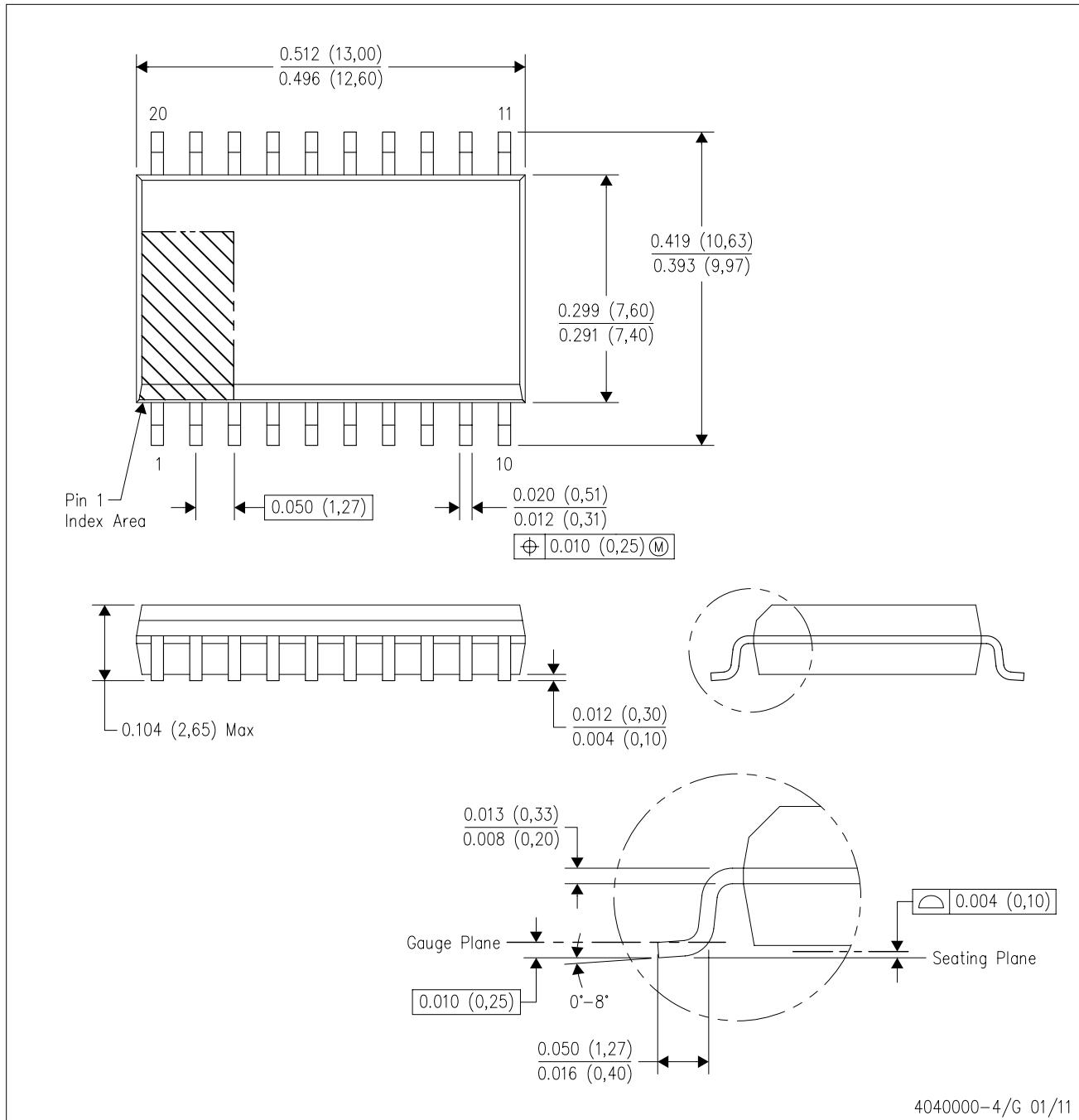
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

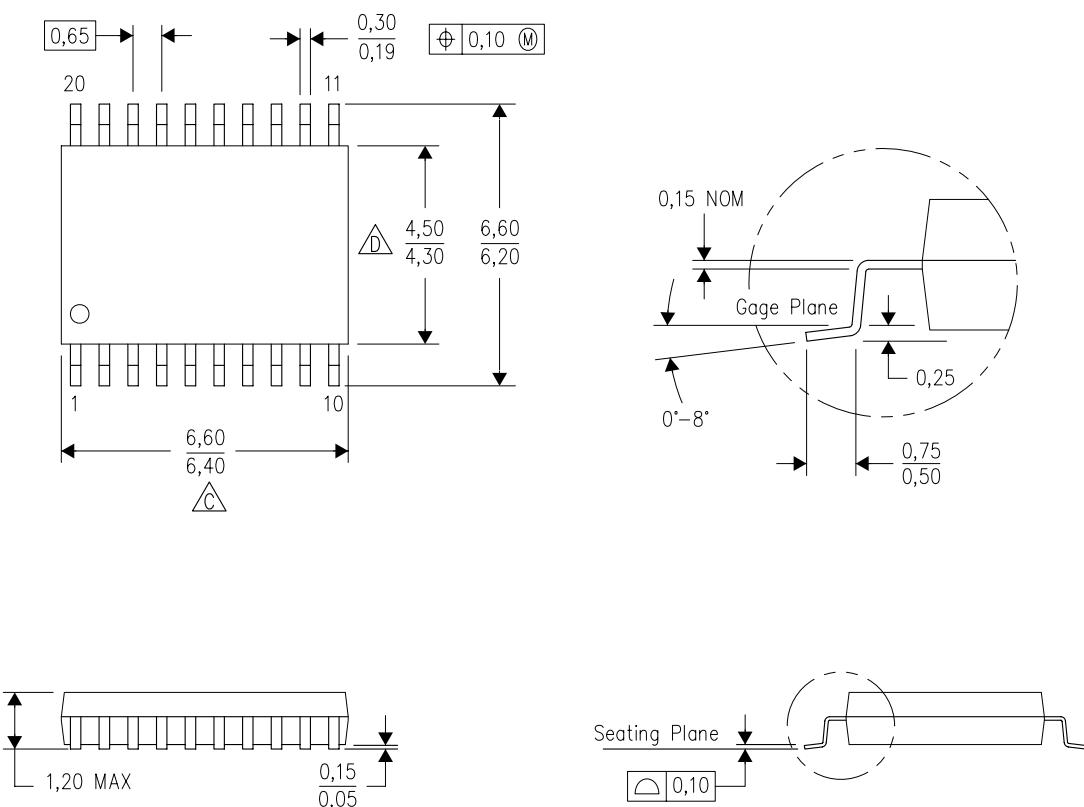


NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

PW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

 Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

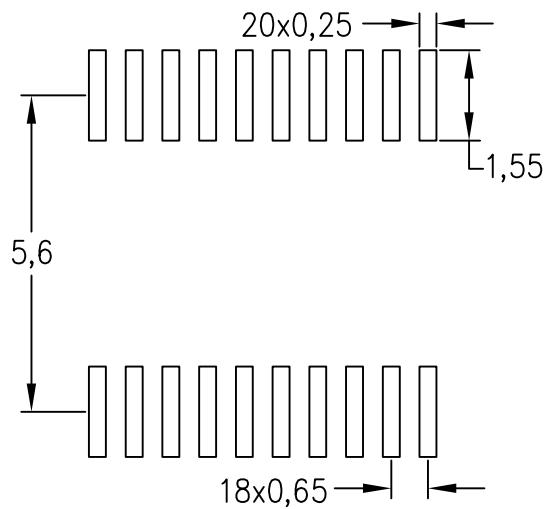
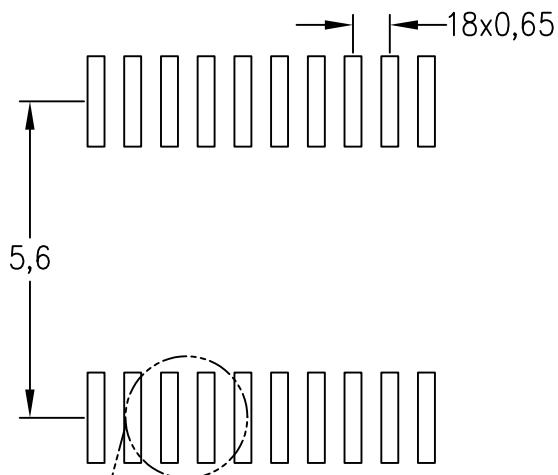
E. Falls within JFDEC M0-153

## PW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE

## Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).



Example  
Non Soldermask Defined Pad

Example  
Solder Mask Opening  
(See Note F)

Pad Geometry

0,3  
1,6  
0,07  
All Around

4211284-5/F 12/12

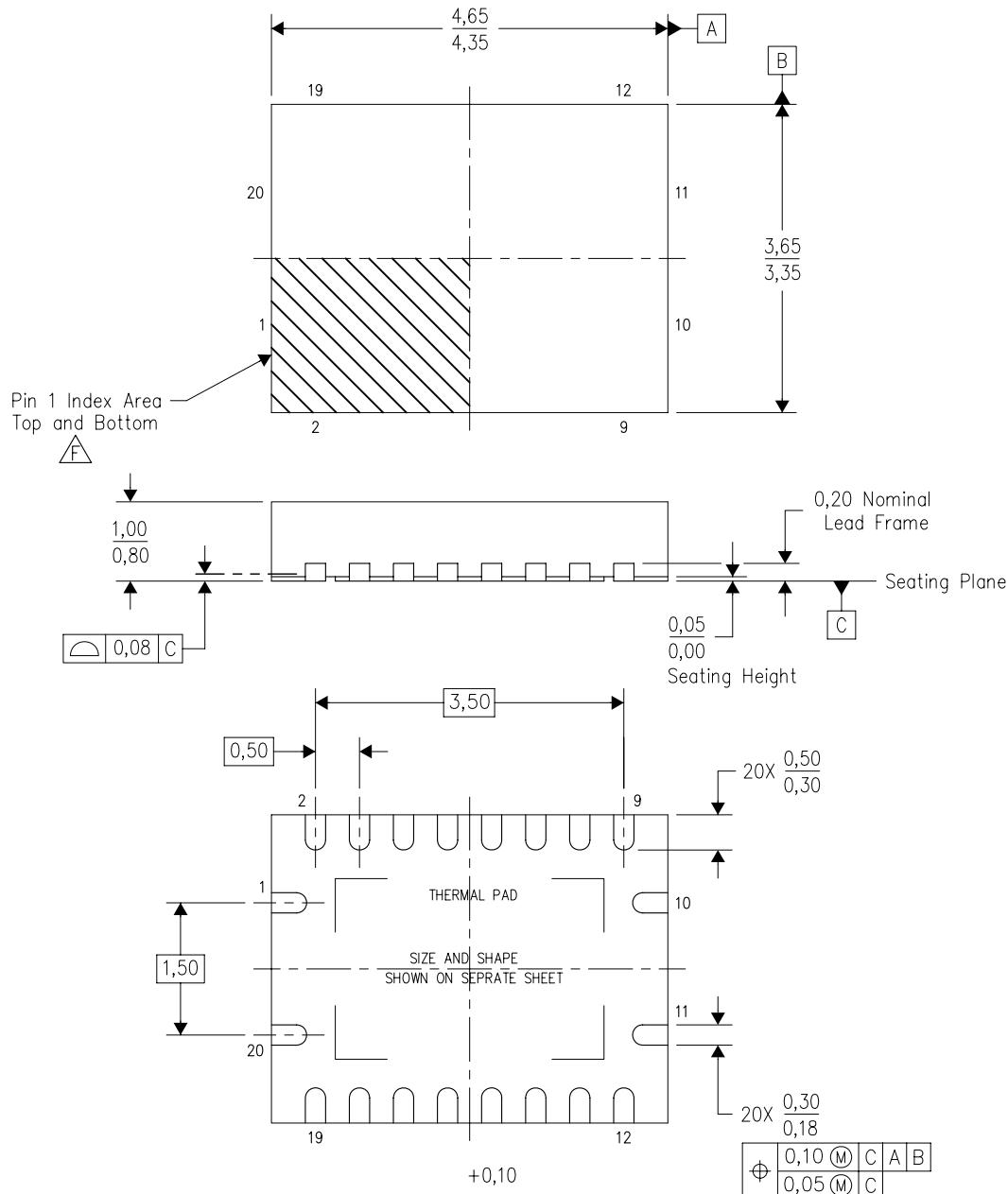
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-4/l 06/2011

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- QFN (Quad Flatpack No-Lead) package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

# THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N20)

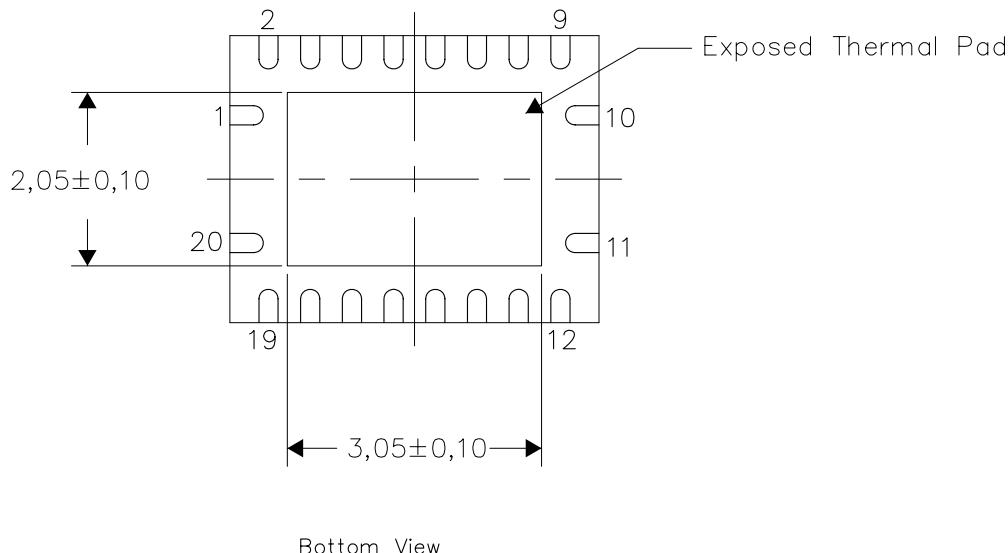
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



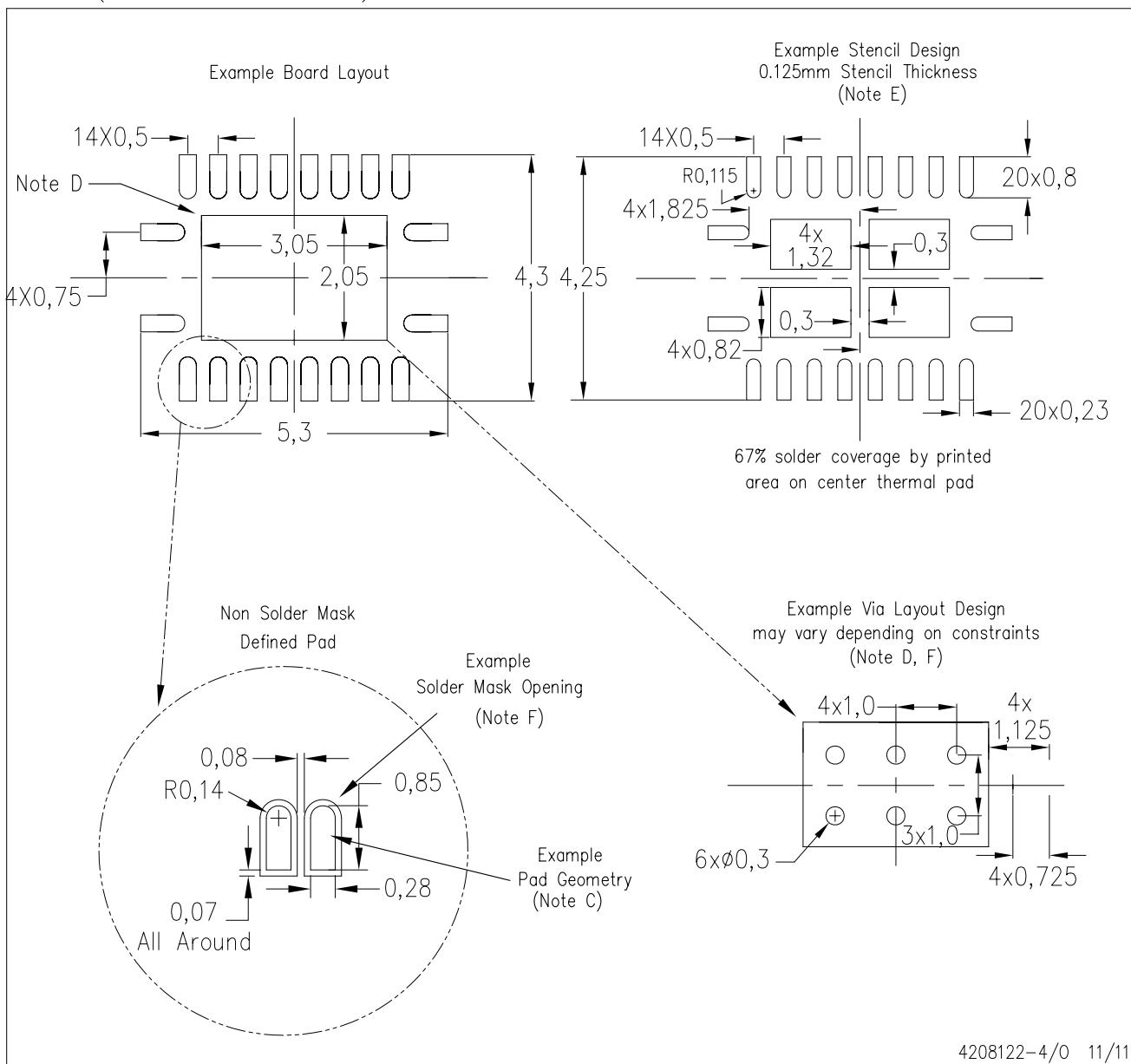
Exposed Thermal Pad Dimensions

4206353-4/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

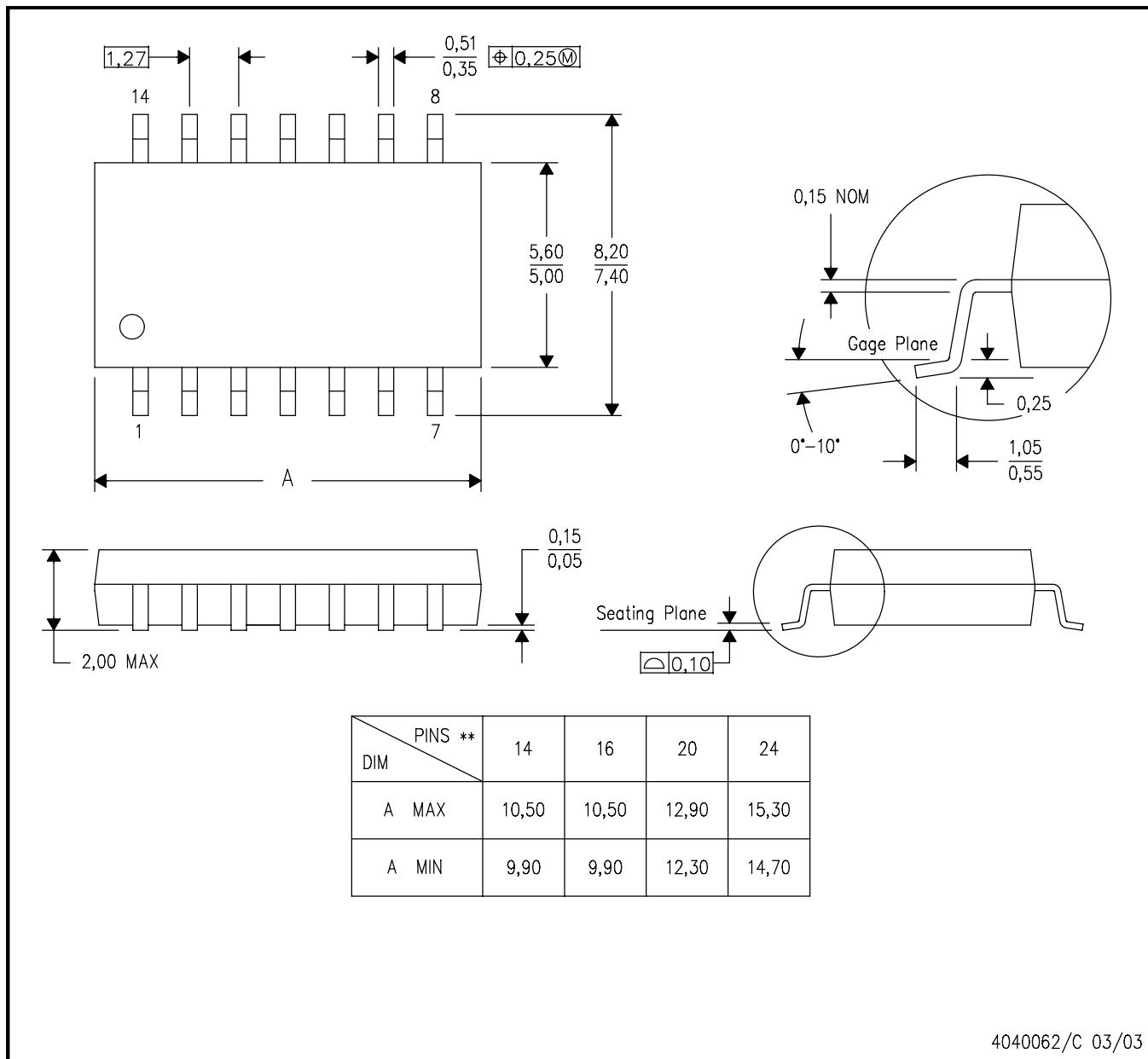
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



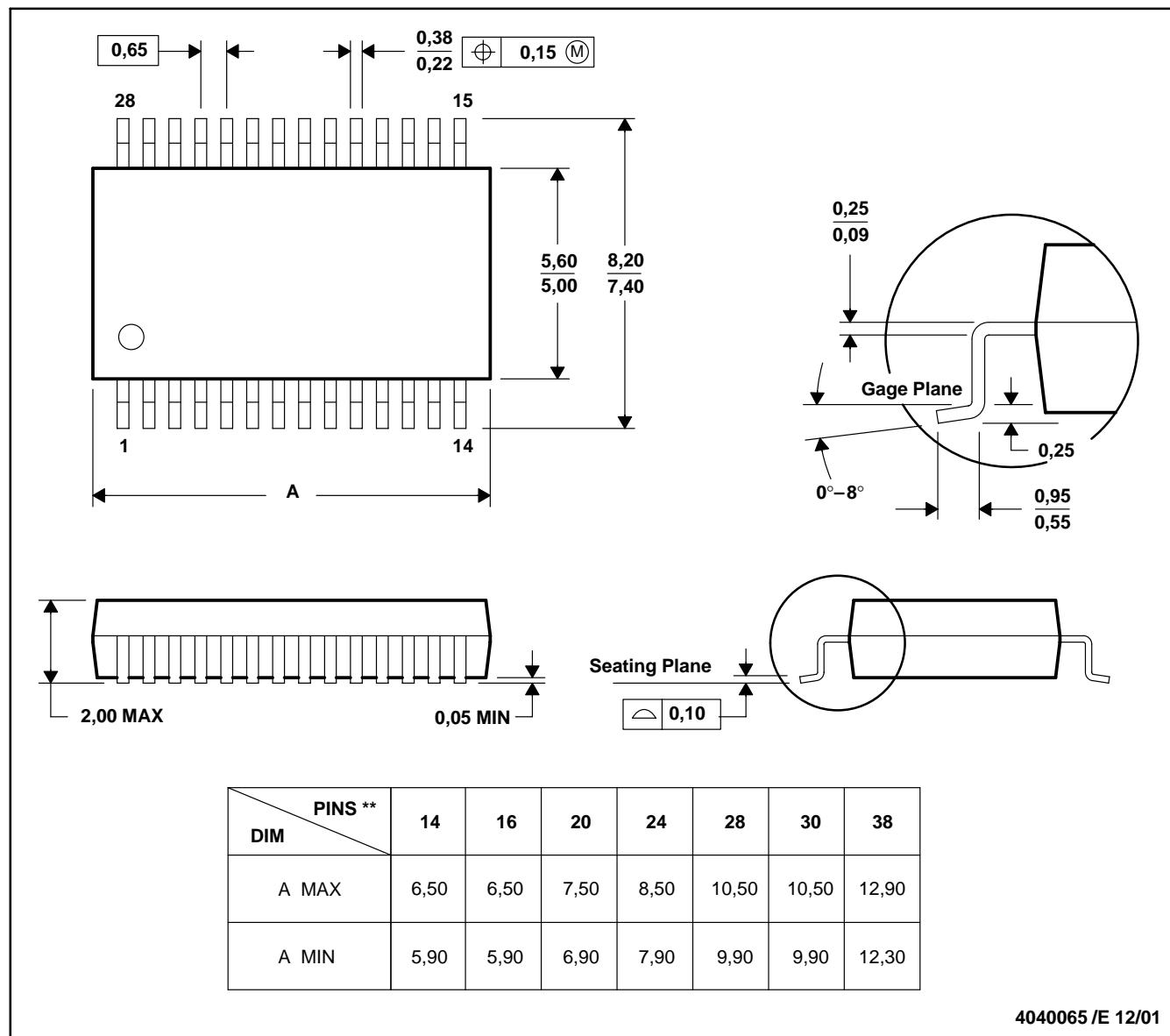
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
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