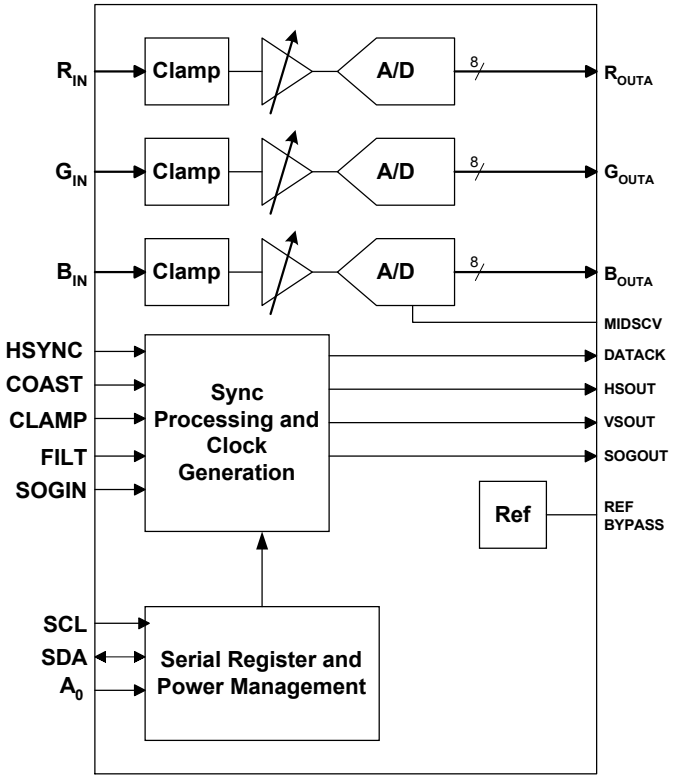
140 MSPS Analog Flat Panel Interface

Preliminary Technical Data AD9883A

FEATURES

140 MSPS Maximum Conversion Rate
300 MHz Analog Bandwidth
0.5V to 1.0V Analog Input Range
500pS p-p PLL clock jitter at 140 MSPS
3.3V power supply
Full sync processing
Sync Detect for "Hot Plugging"
Mid-Scale Clamping
Powerdown Mode
4:2:2 Output Format Mode
Low Power: 550 mW Typical

APPLICATIONS
RGB Graphics Processing
LCD Monitors and Projectors
Plasma Display Panels
Scan Converters
Microdisplays
Digital TV



The AD9883A is a complete 8-bit 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full-power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280 x 1024 at 75 Hz).

The AD9883A includes a 140MHz triple ADC with internal +1.25V reference, a PLL, and programmable gain, offset, and clamp control. The user provides only a +3.3V power supply, analog input, and HSYNC and COAST signals. Three-state CMOS outputs may be powered from 2.5V to 3.3V.

The AD9883A's on-chip PLL generates a pixel clock from HSYNC and COAST inputs. Pixel clock output frequencies range from 12 to 140 MHz. PLL clock jitter is 500ps p-p typical at 140 MSPS. When the COAST signal is presented, the PLL maintains its output frequency in the absence of HSYNC. A sampling phase adjustment is provided. Data, HSYNC and Clock output phase relationships are maintained. The AD9883A also offers full sync processing for composite sync and sync-on-green applications.

A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This interface is fully programmable via a two wire serial interface.

Fabricated in an advanced CMOS process, the AD9883A is provided in a space-saving 80-lead LQFP surface mount plastic package and is specified over the 0°C to +70°C temperature range.

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Analog Interface

ELECTRICAL CHARACTERISTICS (V_D = +3.3V, V_{DD} = +3.3V, ADC Clock = Maximum conversion rate)

Parameter	Temp	Test Level	AD9883AKST-110 Min	AD9883AKST-110 Typical	AD9883AKST-110 Max	AD9883AKST-140 Min	AD9883AKST-140 Typical	AD9883AKST-140 Max	Units
RESOLUTION				8			8		bits
DC ACCURACY									
Differential Nonlinearity	+25°C	I		+/- 0.5	+1.25/-1.0		+/- 0.5	+1.25/-1.0	LSB
	Full	VI			+1.35/-1.0			+1.35/-1.0	LSB
Integral Nonlinearity	+25°C	I		+/- 0.5	+/- 1.85		+/- 0.5	+/- 1.85	LSB
	Full	VI			+/- 2.0			+/- 2.0	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range									
Minimum	Full	VI			0.5			0.5	V p–p
Maximum	Full	VI	1.0			1.0			V p–p
Gain Tempco	+25°C	V		100			100		ppm/°C
Input Bias Current	+25°C	IV			1			1	µA
	Full	IV			1			1	µA
Input Offset Voltage	Full	VI		7	50		7	50	mV
Input Full-Scale Matching	Full	VI		1.5	6.0		1.5	6.0	% FS
Offset Adjustment Range	Full	VI	46	49	52	46	49	52	% FS
REFERENCE OUTPUT									
Output Voltage	Full	VI	+1.20	+1.25	+1.32	+1.20	+1.25	+1.32	V
Temperature Coefficient	Full	V		+/- 50			+/- 50		ppm/°C
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	110			140			MSPS
Minimum Conversion Rate	Full	IV			10			10	MSPS
Data to Clock Skew	Full	IV	-0.5		+2.0	-0.5		+2.0	ns
t_{BUFF}	Full	VI	4.7			4.7			uS
t_{STAH}	Full	VI	4.0			4.0			uS
t_{DHO}	Full	VI	0			0			uS
t_{DAL}	Full	VI	4.7			4.7			uS
t_{DAH}	Full	VI	4.0			4.0			uS
t_{DSU}	Full	VI	250			250			uS
t_{STASU}	Full	VI	4.7			4.7			uS
t_{STOSU}	Full	VI	4.0			4.0			uS
HSYNC Input Frequency	Full	IV	15		110	15		110	KHz
Maximum PLL Clock Rate	Full	VI	110			140			MHz
Minimum PLL Clock Rate	Full	IV			12			12	MHz
PLL Jitter	+25°C	IV		400	700[1]		400	700[1]	ps p-p
	Full	IV			1000[1]			1000[1]	ps p-p
Sampling Phase Tempco	Full	IV		15			15		ps/°C
DIGITAL INPUTS									
Input Voltage, High (V_{IH})	Full	VI	2.5			2.5			V
Input Voltage, Low (V_{IL})	Full	VI			0.8			0.8	V
Input Current, High (I_{IH})	Full	V			-1.0			-1.0	uA
Input Current, Low (I_{IL})	Full	V			1.0			1.0	uA
Input Capacitance	+25°C	V		3			3		pF
DIGITAL OUTPUTS									
Output Voltage, High (V_{OH})	Full	VI	V_D - 0.1			V_D - 0.1			V
Output Voltage, Low (V_{OL})	Full	VI			0.1			0.1	V
Duty Cycle, DATACK	Full	IV	45	50	55	45	50	55	%
Output Coding				Binary			Binary		
POWER SUPPLY									
V_D Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
V_{DD} Supply Voltage	Full	IV	2.2	3.3	3.6	2.2	3.3	3.6	V
P_{VD} Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
I_D Supply Current (V_D)	+25°C	V		132			163		mA

Parameter	Temp	Test Level	AD9883AKST-110 Min	AD9883AKST-110 Typical	AD9883AKST-110 Max	AD9883AKST-140 Min	AD9883AKST-140 Typical	AD9883AKST-140 Max	Units
I_{DD} Supply Current (V_{DD})[2]	+25°C	V		19			24		mA
IP_{VD} Supply Current (P_{VD})	+25°C	V		8			10		mA
Total Power Dissipation	Full	VI		525	650		650	800	mW
Power-Down Supply Current	Full	VI		5	10		5	10	mA
Power-Down Dissipation	Full	VI		16.5	33		16.5	33	mW
DYNAMIC PERFORMANCE									
Analog Bandwidth, Full Power	+25°C	V		300			300		MHz
Transient Response	+25°C	V		2			2		ns
Overvoltage Recovery Time	+25°C	V		1.5			1.5		ns
Signal–to–Noise Ratio (SNR)	+25°C	V		44			43		dB
(Without Harmonics)	Full	V		43			42		dB
f_{IN} = 40.7 MHz									
Crosstalk	Full	V		55			55		dBc
THERMAL CHARACTERISTICS									
0_{JC}-Junction-to-Case Thermal Resistance		V		16			16		°C/W
0_{JA}-Junction-to-Ambient Thermal Resistance		V		35			35		°C/W

NOTES
[1]VCO RANGE = 10, CHARGE PUMP CURRENT = 110, PLL DIVIDER = 1693.
[2]DATACK load = 15pF, Data load = 5pF.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9883AKST-110	0°C to +70°C	ST-80
AD9883AKST-140	0°C to +70°C	ST-80
AD9883A/PCB	+25°C	Evaluation Board

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C; guaranteed by design and characterization testing.

ABSOLUTE MAXIMUM RATINGS*

V_D ..... +3.6 V
V_{DD} ..... +3.6 V
Analog Inputs ..... V_D to 0.0 V
VREF ..... V_D to 0.0 V
Digital Inputs ..... 5V to 0.0 V
Digital Output Current ..... 20 mA
Operating Temperature ..... -25°C to +85°C
Storage Temperature ..... –65°C to +150°C
Maximum Junction Temperature ..... +175°C
Maximum Case Temperature ..... +150°C

- Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Pin Configuration

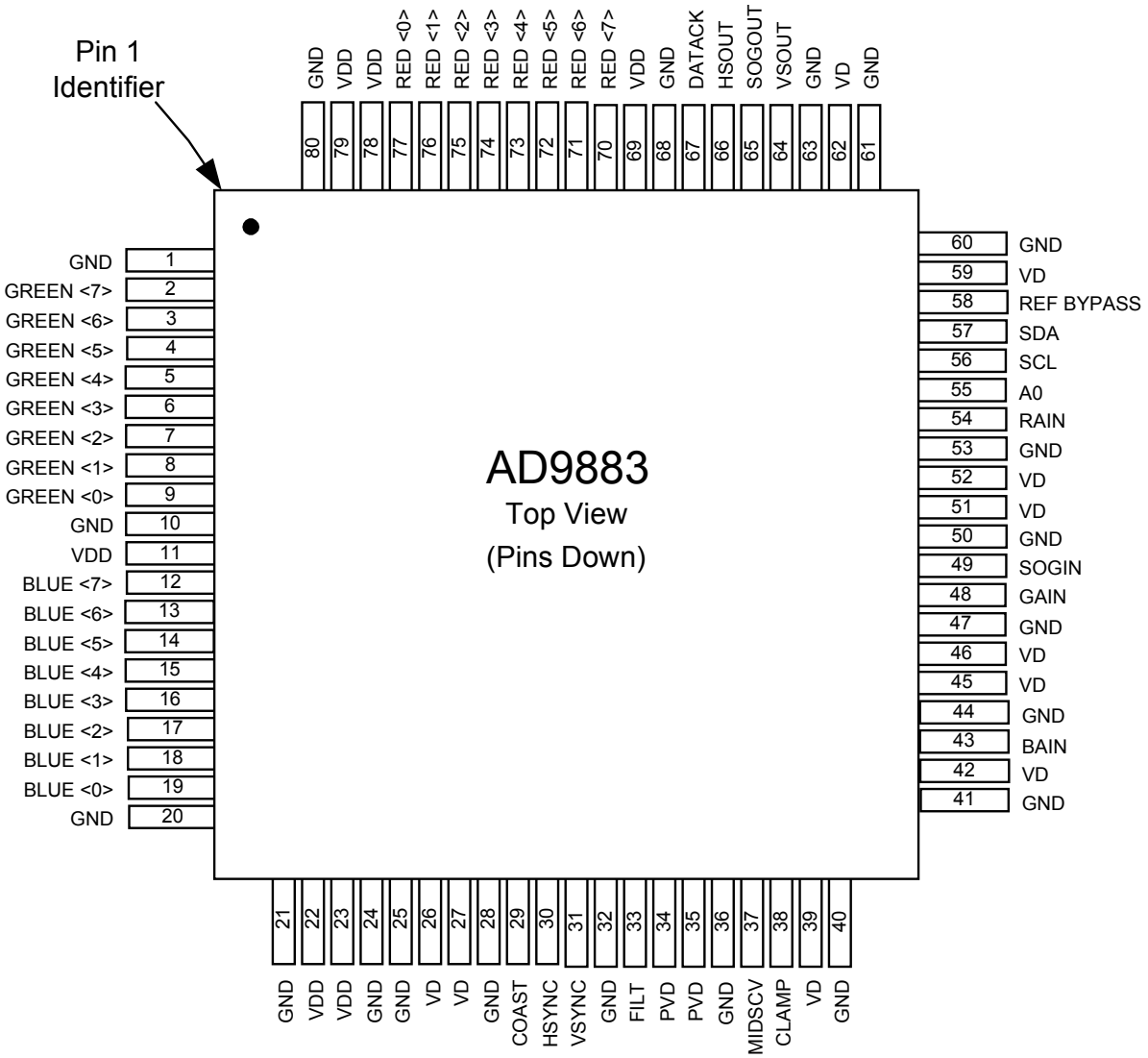


Table 1. Complete Pinout List

Pin Type	Pin Name	Function	Value	Pin Number
Inputs	R_{AIN}	Analog Input for Converter R	0.0V to 1.0V	54
	G_{AIN}	Analog Input for Converter G	0.0V to 1.0V	48
	B_{AIN}	Analog Input for Converter B	0.0V to 1.0V	43
	HSYNC	Horizontal SYNC Input	3.3V CMOS	30
	VSYNC	Vertical SYNC Input	3.3V CMOS	31
	SOGIN	Input for Sync-on-Green	0.0V to 1.0V	49
	CLAMP	Clamp Input (external CLAMP signal)	3.3V CMOS	38
	COAST	PLL COAST Signal Input	3.3V CMOS	29
Outputs	Red [7:0]	Outputs of Converter "Red", Bit 7 is the MSB.	3.3V CMOS	70-77
	Green [7:0]	Outputs of Converter "Green", Bit 7 is the MSB.	3.3V CMOS	2-9
	Blue [7:0]	Outputs of Converter "Blue", Bit 7 is the MSB.	3.3V CMOS	12-19
	DATACK	Data Output Clock	3.3V CMOS	67
	HSOUT	HSYNC Output Clock (phase-aligned with DATACK)	3.3V CMOS	66
	VSOUT	VSYNC Output Clock (phase-aligned with DATACK)	3.3V CMOS	64
	SOGOUT	Sync on Green Slicer Output	3.3V CMOS	65
References	REF BYPASS	Internal Reference Bypass	1.25V +/-	58
	MIDSCV	Internal Mid-Scale Voltage Bypass		37
	FILT	Connection for External Filter Components for Internal PLL		33
Power Supply	V_D	Analog Power Supply	3.3V +/- 10%	
	V_{DD}	Output Power Supply	2.5V to 3.6V	
	PV_D	PLL Power Supply	3.3V +/- 10%	
	GND	Ground	0V	
Control	SDA	Serial Port Data I/O	3.3V CMOS	57
	SCL	Serial Port Data Clock (100KHz maximum)	3.3V CMOS	56
	A_0	Serial Port Address Input 1	3.3V CMOS	55

Pin Function Detail

Outputs

HSOUT **Horizontal Sync Output**

A reconstructed and phase-aligned version of the Hsync input. Both the polarity and duration of this output can be programmed via serial bus registers.

By maintaining alignment with DATACK, and Data, data timing with respect to horizontal sync can always be determined.

VSOUT **Vertical Sync Output**

A reconstructed and phase-aligned version of the video Vsync. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes is set by the graphics transmitter.

SOGOUT **Sync On Green Slicer Output**

This pin outputs either the signal from the Sync-On-Green slicer comparator or an unprocessed but delayed version of the Hsync input. See the Sync Block Diagram on page 29 to view how this pin is connected.

(Note: Besides slicing off SOG, the output from this pin gets no other additional processing on the AD9883A. Vsync separation is performed via the sync separator.)

Serial Port (two-wire)

SDA **Serial Port Data I/O**
SCL **Serial Port Data Clock**
A0 **Serial Port Address Input 1**

For a full description of the two-wire serial register and how it works, refer to the Control Port section on page 27.

Data Outputs

RED **Data Output, Red Channel**
GREEN **Data Output, Green Channel**
BLUE **Data Output, Blue Channel**

The main data outputs. Bit 7 is the MSB. The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The DATACK and HSOUT outputs are also moved, so the timing relationship among the signals is maintained. For exact timing information, refer to the diagrams on page 8.

Data Clock Output

DATACK **Data Output Clock**

This is the main clock output signal used to strobe the output data and HSOUT into external logic.

It is produced by the internal clock generator and is synchronous with the internal pixel sampling clock.

When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The Data, DATACK, and HSOUT outputs are all moved, so the timing relationship among the signals is maintained.

Inputs

R_{AIN} **Analog Input for RED Channel**
G_{AIN} **Analog Input for GREEN Channel**
B_{AIN} **Analog Input for BLUE Channel**

High-impedance inputs that accepts the RED, GREEN, and BLUE channel graphics signals, respectively. (The three channels are identical, and can be used for any colors, but colors are assigned for convenient reference.)

They accommodate input signals ranging from 0.5V to 1.0V full scale. Signals should be ac coupled to these pins to support clamp operation.

Hsync **Horizontal Sync Input**

This input receives a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation.

The logic sense of this pin is controlled by serial register bit 0Eh bit 6 (Hsync Polarity). Only the leading edge of Hsync is active, the trailing edge is ignored. When Hsync Polarity = 0, the falling edge of Hsync is used. When Hsync Polarity = 1, the rising edge is active.

The input includes a Schmitt trigger for noise immunity, with a nominal input threshold of 1.5V.

Vsync **Vertical Sync Input**

This is the input for vertical sync.

SOGIN **Sync-on-Green Input**

This input is provided to assist with processing signals with embedded sync, typically on the GREEN channel. The pin is connected to a high-speed comparator with an internally generated threshold, which is set to 0.15V above the negative peak of the input signal.

When connected to an ac coupled graphics signal with embedded sync, it will produce a non-inverting digital output on SOGOUT. (This is usually a composite sync signal, containing both vertical and horizontal sync information that must be separated before passing the horizontal sync signal to Hsync.)

When not used, this input should be left unconnected. For more details on this function and how it should be configured, refer to the Sync on Green section on page 12.

CLAMP **External Clamp Input**

This logic input may be used to define the time during which the input signal is clamped to ground. It should be exercised when the reference DC level is known to be present on the analog input channels, typically during the back porch of the graphics signal. The CLAMP pin is enabled by setting control bit EXTCLMP to 1, (register 0FH, Bit 7, default is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting a delay and duration from the trailing edge of the HSYNC input. The logic sense of this pin is controlled by CLAMPOL, (register 0FH, Bit 6). When not used, this pin must be grounded and EXTCLMP programmed to 0.

COAST **Clock Generator Coast Input (optional)**

This input may be used to cause the pixel clock generator to stop synchronizing with Hsync and continue producing a clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce horizontal sync pulses during the vertical interval. The COAST signal is generally NOT required for PC-generated signals.

The logic sense of this pin is controlled by CSTPOL, (register 0FH, Bit 3).

When not used, this pin may be grounded and CSTPOL programmed to 1, or tied HIGH (to V_D through a 10K resistor) and CSTPOL programmed to 0. CSTPOL defaults to 1 at power-up.

REF BYPASS **Internal Reference BYPASS**

Bypass for the internal 1.25V bandgap reference. It should be connected to ground through a 0.1uF capacitor.

The absolute accuracy of this reference is ± 4%, and the temperature coefficient is ±50 ppm, which is adequate for most AD9883A applications. If higher accuracy is required, an external reference may be employed instead.

MIDSCV **Mid-Scale Voltage Reference BYPASS**

Bypass for the internal mid-scale voltage reference. It should be connected to ground through a 0.1uF capacitor. The exact voltage varies with the gain setting of the BLUE channel.

FILT **External Filter Connection**

For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 6 to this pin. For optimal performance, minimize noise and parasitics on this node.

Power Supply

V_D **Main Power Supply**

These pins supply power to the main elements of the circuit. They should be as quiet and filtered as possible.

V_{DD} **Digital Output Power Supply**

A large number of output pins (up to 25) switching at high speed (up to 140 MHz) generates a lot of power supply transients (noise). These supply pins are identified separately from the V_D pins so special care can be taken to minimize output noise transferred into the sensitive analog circuitry.

If the AD9883A is interfacing with lower-voltage logic, V_{DD} may be connected to a lower supply voltage (as low as 2.5V) for compatibility.

PV_D **Clock Generator Power Supply**

The most sensitive portion of the AD9883A is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide "quiet," noise-free power to these pins.

GND **Ground**

The ground return for all circuitry on chip. It is recommended that the AD9883A be assembled on a single solid ground plane, with careful attention to ground current paths.

Design Guide

General Description

The AD9883A is a fully integrated solution for capturing analog RGB signals and digitizing them for display on flat panel monitors or projectors. The circuit is ideal for providing a computer interface for HDTV monitors or as the front-end to high-performance video scan converters.

Implemented in a high-performance CMOS process, the interface can capture signals with pixel rates of up to 140 MHz.

The AD9883A includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

With a typical power dissipation of only 500mW and an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

Digital Inputs

All digital inputs on the AD9883A operate to 3.3V CMOS levels. However, all digital inputs are 5V tolerant. (Applying 5V to them will not cause any damage.)

Input Signal Handling

The AD9883A has three high-impedance analog input pins for the Red, Green, and Blue channels. They will accommodate signals ranging from 0.5V to 1.0V p-p.

Signals are typically brought onto the interface board via a DVI-I connector, a 15-pin D connector, or via BNC connectors. The AD9883A should be located as close as practical to the input connector. Signals should be routed via matched-impedance traces (normally 75Ω) to the IC input pins.

At that point the signal should be resistively terminated (75Ω to the signal ground return) and capacitively coupled to the AD9883A inputs through 47nF capacitors. These capacitors form part of the dc restoration circuit.

In an ideal world of perfectly matched impedances, the best performance can be obtained with the widest possible signal bandwidth. The ultrawide bandwidth inputs of the AD9883A (300 MHz) can track the input signal continuously as it moves from one pixel level to the next, and digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. It has been shown that a small inductor in series with the input is effective in rolling off the input bandwidth slightly, and providing a high quality signal over a wider range of conditions. Using a Fair-Rite #2508051217Z0- High-Speed Signal Chip Bead inductor in the circuit of Figure 1 gives good results in most applications.

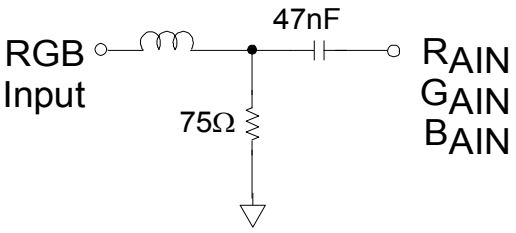


Figure 1. Analog Input Interface Circuit

Hsync, Vsync Inputs

The interface also takes a horizontal sync signal, which is used to generate the pixel clock and clamp timing. This can be either a sync signal directly from the graphics source, or a preprocessed TTL or CMOS level signal.

The Hsync input includes a Schmitt trigger buffer for immunity to noise and signals with long risetimes. In typical PC-based graphic systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. As such, no termination is required.

Serial Control Port

The serial control port is designed for 3.3V logic. If there are 5V drivers on the bus, these pins should be protected with 150 ohm series resistors placed between the pull-up resistors and the input pins.

Output Signal Handling

The digital outputs are designed and specified to operate from a 3.3V power supply (V_{DD}). They can also work with a V_{DD} as low as 2.5V for compatibility with other 2.5V logic.

Clamping

RGB clamping

To properly digitize the incoming signal, the dc offset of the input must be adjusted to fit the range of the on-board A/D converters.

Most graphics systems produce RGB signals with black at ground and white at approximately +0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground and black is at +300 mV. Then white is at approximately +1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal, which must be removed for proper capture by the AD9883A.

The key to clamping is to identify a portion (time) of the signal when the graphic system is known to be producing black. An offset is then introduced which results in the A/D converters producing a black output (code 00h) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In most pc graphics systems, black is transmitted between active video lines. With CRT displays, when the electron beam has completed writing a horizontal line on the screen (at the right side), the beam is deflected quickly to the left side of the screen (called horizontal retrace) and a black signal is provided to prevent the beam from disturbing the image.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. For obvious reasons, it is important to avoid clamping on the tip of Hsync. Fortunately, there is virtually always a period following Hsync called the back porch where a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by simply exercising the CLAMP pin at the appropriate time (with EXTCLMP = 1). The polarity of this signal is set by the Clamp Polarity bit.

A simpler method of clamp timing employs the AD9883A internal clamp timing generator. The Clamp Placement register is programmed with the number of pixel times that should pass after the trailing edge of HSYNC before clamping starts. A second register (Clamp Duration) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync because, though Hsync duration can vary widely, the back porch (black reference) always follows Hsync. A good starting point for establishing clamping is to set the clamp placement to 09h (providing 9 pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 14h (giving the clamp 20 pixel periods to reestablish the black reference).

Clamping is accomplished by placing an appropriate charge on the external input coupling capacitor. The value of this capacitor affects the performance of the clamp. If it is too small, there will be a significant amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, then it will take excessively long for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovering from a step error of 100 mV to within ½ LSB in 10 lines with a clamp duration of 20 pixel periods on a 75 Hz SXGA signal.

YUV Clamping

YUV graphic signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) can be at the midpoint of the graphics signal rather than the bottom. For these signals it can be necessary to clamp to the mid-scale range of the A/D converter range (80h) rather than bottom of the A/D converter range (00h).

Clamping to mid-scale rather than ground can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit so that they can be clamped to either mid-scale or ground independently. These bits are located in register 10h and are bits 0-2. The mid-scale reference voltage that each A/D converter clamps to is provided on the MIDSCV pin, (pin 37). This pin should be bypassed to ground with a 0.1uF capacitor, (even if mid-scale clamping is not required).

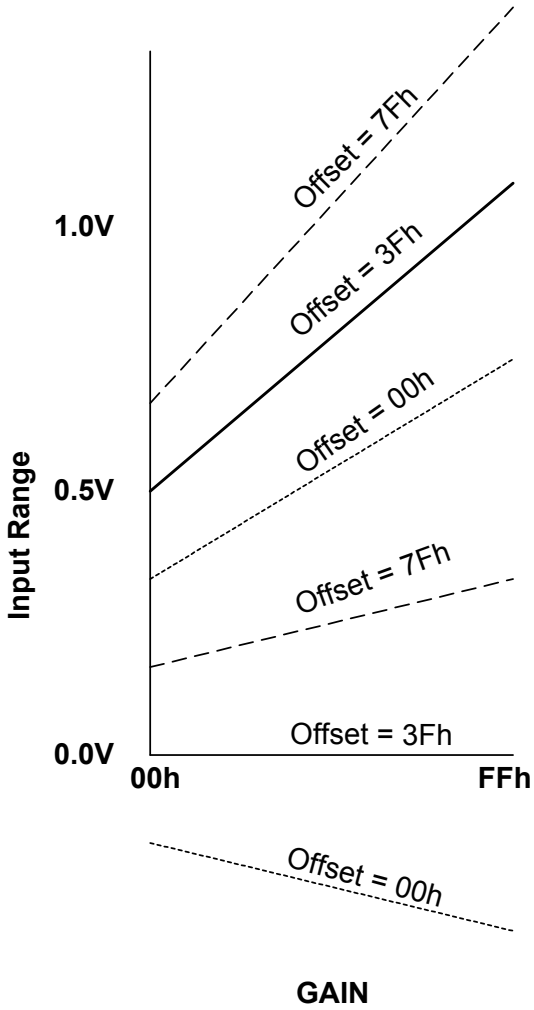


Figure 2. Gain and Offset Control

Gain and Offset Control

The AD9883A can accommodate input signals with inputs ranging from 0.5V to 1.0V full scale. The full scale range is set in three 8-bit registers (Red Gain, Green Gain, and Blue Gain).

Note that INCREASING the gain setting results in an image with LESS contrast.

The offset control shifts the entire input range, resulting in a change in image brightness. Three 7-bit registers (Red Offset, Green Offset, Blue Offset) provide independent settings for each channel.

The offset controls provide a ±63 LSB adjustment range. This range is connected with the full scale range, so if the input range is doubled (from 0.5V to 1.0V) then the offset step size is also doubled (from 2mVper step to 4 mV per step).

Figure 2 illustrates the interaction of gain and offset controls. The magnitude of an LSB in offset adjustment is proportional to the full-scale range, so changing the full-scale range also changes the offset. The change is minimal if the offset setting in near mid-scale. When changing the offset, the full-scale *range* is not affected, but the full-scale *level* is shifted by the same amount as the zero scale level.

Sync on Green

The Sync on Green input operates in two steps. First, it sets a baseline clamp level off of the incoming video signal with a negative peak detector. Second, it sets the sync trigger level to a programmable level (typically 150mV) above the negative peak. The Sync on Green input must be AC coupled to the green analog input through its own capacitor as shown below in Figure 3. The value of the capacitor must be 1 nF +/- 20%. If Sync-on-Green is not used, this connection is not required. (Note: The Sync on Green signal is always negative polarity.)

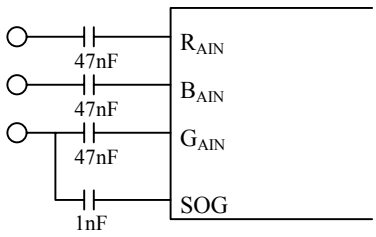


Figure 3. Typical clamp configuration

Clock Generation

A Phase Locked Loop (PLL) is employed to generate the pixel clock. In this PLL, the Hsync input provides a reference frequency. A Voltage Controlled Oscillator (VCO) generates a much higher pixel clock frequency. This pixel clock is divided by the PLL divide value (registers 01H and 02H) and phase compared with the Hsync input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is a very important element in providing the clearest and most stable image. During each pixel time, there is a period during which the signal is slewing from the old pixel amplitude and settling at its new value. Then there is a time when the input voltage is stable, before the signal must slew to a new value (Figure 4). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC and the bandwidth of the transmission system (cable and termination). It is also a function of the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, then the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter, and the stable pixel time becomes shorter as well.

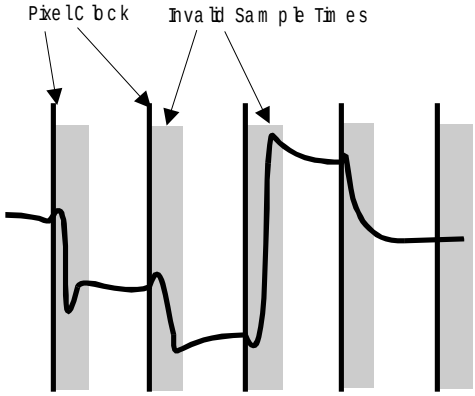


Figure 4. Pixel Sampling Times

Any jitter in the clock reduces the precision with which the sampling time can be determined, and must also be subtracted from the stable pixel time.

Considerable care has been taken in the design of the AD9883A's clock generation circuit to minimize jitter. As indicated in Figure 5, the clock jitter of the AD9883A is less than 5% of the total pixel time in all operating modes, making the reduction in the valid sampling time due to jitter negligible.

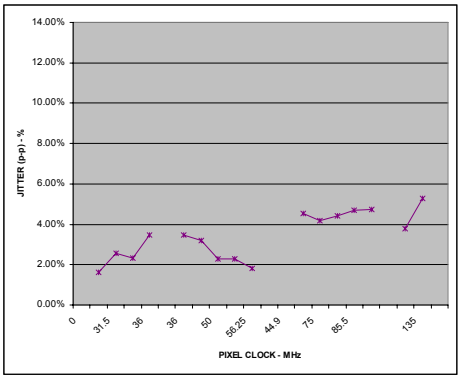


Figure 5. Pixel Clock Jitter vs. Frequency

The PLL characteristics are determined by the loop filter design, by the PLL Charge Pump Current and by the VCO range setting. The loop filter design is illustrated in Figure 6. Recommended settings of VCO range and charge pump current for VESA standard display modes are listed in Table 5.

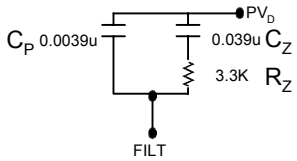


Figure 6. PLL Loop Filter Detail

Four programmable registers are provided to optimize the performance of the PLL. These registers are:

(1) The 12-bit Divisor Register. The input Hsync frequencies range from 15 kHz to 110 kHz. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 12 MHz to 140 MHz. The Divisor Register controls the exact multiplication factor. This register may be set to any value between 221 and 4095. (The divide ratio that is actually used is the programmed divide ratio plus one.)

(2) The 2-bit VCO Range Register. To improve the noise performance of the AD9883A, the VCO operating frequency range is divided into three overlapping regions. The VCO Range register sets this operating range. The frequency ranges for the lowest and highest regions are shown in Table 2.

Table 2. VCO Frequency Ranges

PV1	PV0	Pixel Clock Range (MHz)	K_{VCO} Gain (MHz/V)
0	0	12-30	150
0	1	30-60	150
1	0	60-140	150

(3) The 3-bit Charge Pump Current register. This register allows the current that drives the low pass loop filter to be varied. The possible current values are listed in Table 3.

Table 3. Charge Pump Current/Control bits

Ip2	Ip1	Ip0	Current (μA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

(4) The 5-bit Phase Adjust Register. The phase of the generated sampling clock may be shifted to locate an optimum sampling point within a clock cycle. The Phase Adjust register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin.

The COAST pin is used to allow the PLL to continue to run at the same frequency, in the absence of the incoming HSYNC signal or during disturbances in Hsync (such as equalization pulses). This may be used during the vertical sync period, or any other time that the HSYNC signal is unavailable. The polarity of the COAST signal may be set through the Coast Polarity Register. Also, the polarity of the HSYNC signal may be set through the HSYNC Polarity Register. For both HSYNC and COAST, a value of `1' is active high.

Power Management

The AD9883A uses the activity detect circuits, the active interface bits in the serial bus, the active interface override bits, and the powerdown bit to determine the correct power state. There are three power states, full-power, seek mode, and power-down. Table 4 summarizes how the AD9883A determines what power mode to be in and what circuitry is powered on/off in each of these modes. The powerdown command has priority and then the automatic circuitry.

Table 4. Powerdown Mode Descriptions

Mode	Inputs		Powered On or Comments
	Power-down[1]	Sync Detect[2]	
Full-Power	1	1	Everything
Seek Mode	1	0	Serial Bus, Sync Activity Detect, SOG, Bandgap Reference
Power-down	0	X	Serial Bus, Sync Activity Detect, SOG, Bandgap Reference

Note[1] Powerdown is controlled via bit 1 in serial bus register 0Fh.

Note[2] Sync Detect is determined by OR-ing bits 7,4, and 1 in serial bus register 14h.

Table 5. Recommended VCO Range and Charge Pump Current Settings for Standard Display Formats

Standard	Resolution	Refresh Rate	Horizontal Frequency	Pixel Rate	VCORNGE	CURRENT
VGA	640x480	60 Hz	31.5 kHz	25.175 MHz	00	101
		72 Hz	37.7 kHz	31.500 MHz	00	110
		75 Hz	37.5 kHz	31.500 MHz	00	110
		85 Hz	43.3 kHz	36.000 MHz	00	110
SVGA	800x600	56 Hz	35.1 kHz	36.000 MHz	00	110
		60 Hz	37.9 kHz	40.000 MHz	01	100
		72 Hz	48.1 kHz	50.000 MHz	01	100
		75 Hz	46.9 kHz	49.500 MHz	01	100
		85 Hz	53.7 kHz	56.250 MHz	01	101
XGA	1024x768	60 Hz	48.4 kHz	65.000 MHz	01	100
		70 Hz	56.5 kHz	75.000 MHz	10	100
		75 Hz	60.0 kHz	78.750 MHz	10	100
		80 Hz	64.0 kHz	85.500 MHz	10	100
		85 Hz	68.3 kHz	94.500 MHz	10	100
SXGA	1280x1024	60 Hz	64.0 kHz	108.000 MHz	10	110
	1280x1024	75 Hz	80.0 kHz	135.000 MHz	10	110

Timing

The following timing diagrams show the operation of the AD9883A.

The Output Data Clock signal is created so that its rising edge always occurs between data transitions, and can be used to latch the output data externally.

There is a pipeline in the AD9883A, which must be flushed before valid data becomes available. This means four data sets are presented before valid data is available.

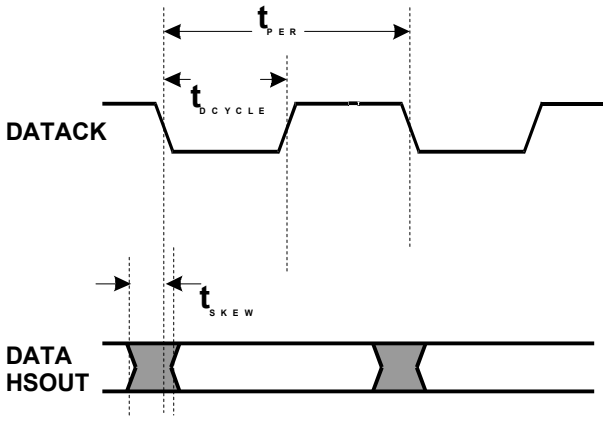


Figure 7. Output Timing

Hsync Timing

Horizontal Sync (Hsync) is processed in the AD9883A to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted, with respect to Hsync, through a full 360° in 32 steps via the Phase Adjust register (to optimize the pixel sampling time). Display systems use Hsync to align memory and display write cycles, so it is important to have a stable timing relationship between Hsync output (HSOUT) and data clock (DATACK).

Three things happen to Horizontal Sync in the AD9883A. First, the polarity of Hsync input is determined and will thus have a known output polarity. The known output polarity can be programmed either active high or active low (register 0EH, bit 5). Second, HSOUT is aligned with DATACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via register 07H. HSOUT is the sync signal that should be used to drive the rest of the display system.

Coast Timing

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the COAST input and function are unnecessary, and should not be used and the pin should be permanently connected to the inactive state.

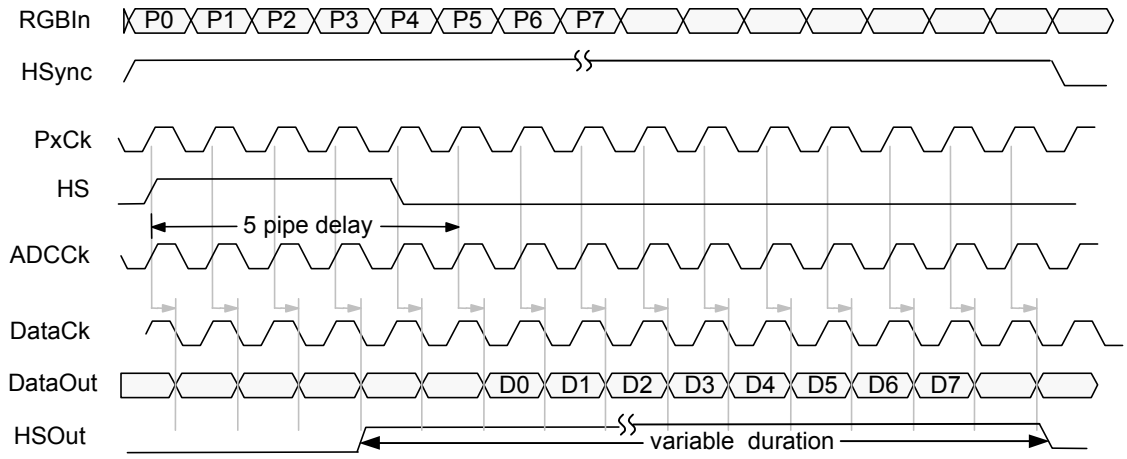
In some systems, however, Hsync is disturbed during the Vertical Sync period (Vsync). In some cases, Hsync pulses disappear. In other systems, such as those that employ Composite Sync (Csync) signals or embeded Sync-On-Green (SOG), Hsync includes equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it will attempt to lock to this new frequency, and will have changed frequency by the end of the Vsync period. It will then take a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a “tearing” of the image at the top of the display.

The COAST input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and allows the clock to free-run at its then-current frequency. The PLL can free-run for several lines without significant frequency drift.

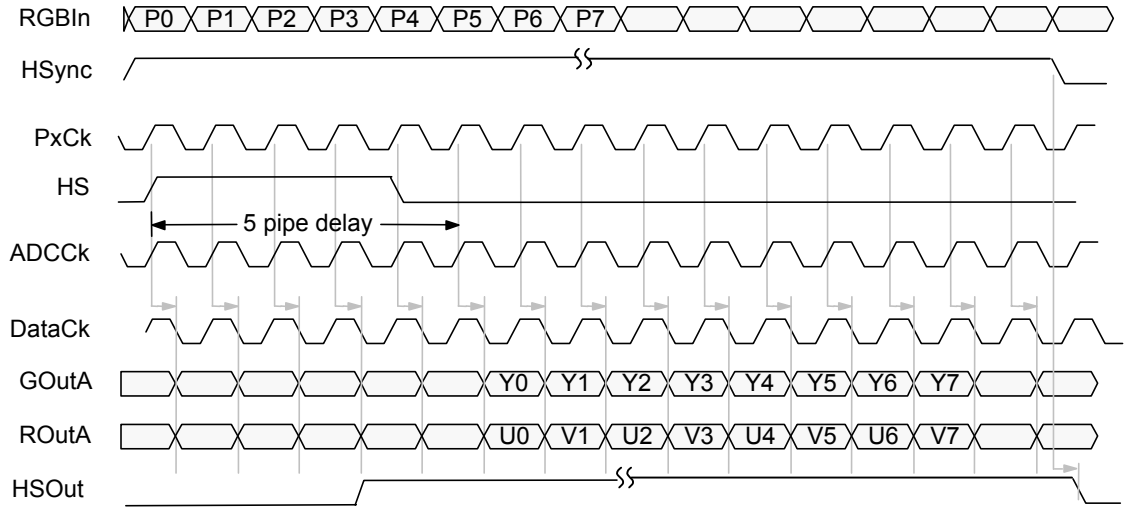
Coast can be driven directly from a Vsync input, or can be provided by the graphics controller.

Timing Diagrams

4:4:4 Mode (for RGB & YUV)



4:2:2 Mode (for YUV only)



Two-Wire Serial Register Map

The AD9883A is initialized and controlled by a set of registers, which determine the operating modes. An external controller is employed to write and read the Control Registers through the 2-wire serial interface port.

Table 6. Control Register Map

Hex Address	Write and Read or Read Only	Bits	Default Value	Register Name	Function
00H	RO	7:0	-	Chip Revision	An 8-bit register which represents the silicon revision level. Revision 0 = 0000 0000
01H	W/R	7:0	01101001	PLL Div MSB	This register is for bits [11:4] of the PLL divider. Larger values mean the PLL operates at a faster rate. This register should be loaded first whenever a change is needed (This will give the PLL more time to lock.) See Note 1
02H	W/R	7:4	1101****	PLL Div LSB	Bits [7:4] LSBs of the PLL divider word. See Note 1
03H	W/R	7:3	01*****		Bits [7:6] VCO Range. Selects VCO frequency range. (see PLL description)
			001*		Bits [5:3] Charge Pump Current. Varies the current that drives the low pass filter. (see PLL description)
04H	W/R	7:3	01000***	Phase Adjust	ADC Clock phase adjustment. Larger values mean more delay. (1LSB=T/32)
05H	W/R	7:0	10000000	Clamp Placement	Places the Clamp signal an integer number of clock periods after the trailing edge of the HSYNC signal.
06H	W/R	7:0	10000000	Clamp Duration	Number of clock periods that the Clamp signal is actively clamping.
07H	W/R	7:0	00100000	Hsync Output Pulse Width	Sets the number of pixel clocks that HSOUT will remain active.
08H	W/R	7:0	10000000	Red Gain	Controls ADC input range (Contrast) of each respective channel. Bigger values give less contrast.
09H	W/R	7:0	10000000	Green Gain	
0AH	W/R	7:0	10000000	Blue Gain	
0BH	W/R	7:1	1000000*	Red Offset	Controls DC offset (Brightness) of each respective channel. Bigger values decrease brightness.
0CH	W/R	7:1	1000000*	Green Offset	
0DH	W/R	7:1	1000000*	Blue Offset	
0EH	W/R	7:0	0*******	Sync Control	Bit 7– Hsync Polarity Override. (Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by bit 6 in register 0Eh)
			*1******		Bit 6 – Hsync Input Polarity. Indicates to the PLL the polarity of incoming HSYNC signal. (Logic 0 = active low, Logic 1 = active high)
			0***		Bit 5 – Hsync Output polarity. (Logic 0 = Logic High Sync, Logic 1 = Logic Low Sync).
			0*		Bit 4 - Active Hsync override. If set to logic 1, the user can select the Hsync to be used via bit 3. If set to logic 0, the active interface is selected via bit 6 in register 14H.
			****0***		Bit 3 - Active Hsync select. Logic 0 selects Hsync as the active sync. Logic 1 selects Sync-on-Green as the active sync. Note: The indicated Hsync will be used only if Bit 4 is set to logic 1 or if both syncs are active, (Bits 1,7 = logic 1 in register 14H).
			*****0**		Bit 2 – Vsync Output polarity. (Logic 0 = Logic High Sync, Logic 1 = Logic Low Sync).
			******0*		Bit 1 - Active Vsync override. If set to logic 1, the user can select the Vsync to be used via bit 0. If set to logic 0, the active interface is selected via bit 3 in register 14H.
			*******0		Bit 0 - Active Vsync select. Logic 0 selects Raw Vsync as the output Vsync. Logic 1 selects Sync Separated Vsync as the output Vsync. Note: The indicated Vsync will be used only if Bit 1 is set to logic 1.
0FH	W/R	7:1	0*******		Bit 7 – Clamp Function. Chooses between HSYNC for Clamp signal or another external signal to be used for clamping. (Logic 0 = HSYNC, Logic 1 = Clamp).
			*1******		Bit 6 – Clamp Polarity. Valid only with external CLAMP signal. (Logic 0 = active high, Logic 1 selects active low)

			0***		Bit 5 – Coast select. Logic 0 selects the coast input pin to be used for the PLL coast. Logic 1 selects Vsync to be used for the PLL coast.
			0*		Bit 4 – Coast Polarity Override. (Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by bit 3 in register 0Fh)
			****1***		Bit 3 – Coast Polarity. Changes polarity of external COAST signal. (Logic =0 = active low, Logic 1 = active high)
			*****1**		Bit 2 –Seek Mode Override. (Logic 1 = allow low-power mode, Logic 0 = disallow low-power mode)
			******1*		Bit 1 - PWRDN/. Full Chip Power Down, active low. (Logic 0 = Full Chip Power Down, Logic 1 = normal)
10H	W/R	7:3	10111***	Sync-on-Green Threshold	Sync-on-Green Threshold – Sets the voltage level of the Sync-on-Green slicer's comparator.
			*****0**		Bit 2 – Red Clamp Select – Logic 0 selects clamp to ground. Logic 1 selects clamp to mid-scale, (voltage at pin 37).
			******0*		Bit 1 – Green Clamp Select – Logic 0 selects clamp to ground. Logic 1 selects clamp to mid-scale, (voltage at pin 37).
			*******0		Bit 0 – Blue Clamp Select – Logic 0 selects clamp to ground. Logic 1 selects clamp to mid-scale, (voltage at pin 37).
11H	W/R	7:0	00100000	Sync Separator Threshold	Sync Separator Threshold – Sets how many internal 5MHz clock periods the sync separator will count to before toggling high or low. This should be set to some number greater than the maximum Hsync or equalization pulse width.
12H	W/R	7:0	00000000	Pre-Coast	Pre-Coast – Sets the number of Hsync periods that coast becomes active prior to Vsync.
13H	W/R	7:0	00000000	Post-Coast	Post-Coast – Sets the number of Hsync periods that coast stays active following Vsync.
14H	RO	7:0		Sync Detect	Bit 7 – Hsync detect. It is set to logic 1 if Hsync is present on the analog interface, else it is set to logic 0.
					Bit 6 – AHS: Active Hsync. This bit indicates which analog Hsync is being used. (Logic 0 = Hsync input pin, Logic 1 = Hsync from sync-on-green).
					Bit 5 – Input Hsync Polarity Detect. (Logic 0 = active low, Logic 1 = active high)
					Bit 4 – Vsync detect. It is set to logic 1 if V-sync is present on the analog interface, else it is set to logic 0.
					Bit 3 – AVS: Active Vsync. This bit indicates which analog Vsync is being used. (Logic 0 = Vsync input pin, Logic 1 = Vsync from sync separator).
					Bit 2 – Input Vsync Polarity Detect. (Logic 0 = active low, Logic 1 = active high)
					Bit 1 – Sync-on-Green detect. It is set to logic 1 if sync is present on the green video input, else it is set to 0.
					Bit 0 – Input Coast Polarity Detect. (Logic 0 = active low, Logic 1 = active high)
15H	W/R	7			Bit 7 - 4:2:2 Output Formatting Mode.
16H	W/R	7:0		Test Register	Reserved for future use
17H	RO	7:0		Test Register	Reserved for future use
18H	RO	7:0		Test Register	Reserved for future use

Note 1: The AD9883A only updates the PLL divide ratio when the LSBs are written to (register 02h).

Two-Wire Serial Control Register Detail

Chip Identification

00 7-0 Chip Revision

An 8-bit register which represents the silicon revision. Revision 0 = 0000 0000, Revision 1 = 0000 0001, Revision 2 = 0000 0010.

PLL DIVIDER CONTROL

01 7-0 PLL Divide Ratio MSBs

The 8 most significant bits of the 12-bit PLL divide ratio PLLDIV. (The operational divide ratio is PLLDIV + 1.)

The PLL derives a master clock from an incoming Hsync signal. The master clock frequency is then divided by an integer value, such that the output is phase-locked to Hsync. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of the PLL divider supports divide ratios from 2 to 4095. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed Hsync frequency.

VESA has established some standard timing specifications, which will assist in determining the value for PLLDIV as a function of horizontal and vertical display resolution and frame rate (Table 5).

However, many computer systems do not conform precisely to the recommendations, and these numbers should be use only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV will usually produce one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69h, PLLDIVL = Dxh).

The AD9883A updates the full divide ratio only when the LSBs are changed. Writing to this register by itself will not trigger an update.

02 7-4 PLL Divide Ratio LSBs

The four least significant bits of the 12-bit PLL divide ratio PLLDIV. The operational divide ratio is PLLDIV + 1.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69h, PLLDIVL = Dxh).

The AD9883A updates the full divide ratio only when this register is written to.

Clock Generator Control

03 7-6 VCO Range Select

Two bits that establish the operating range of the clock generator.

VCORNGE must be set to correspond with the desired operating frequency (incoming pixel rate).

The PLL VCO gives the best jitter performance while operating at high frequencies. For this reason, in order to output low pixel rates and still get good jitter performance, the PLL VCO actually operates at a higher frequency but then divides down the clock rate afterwards. Table 7 shows the pixel rates for each VCO range setting. The PLL output divisor is automatically selected with the VCO range setting.

Table 7. VCO Ranges

VCORNGE	Pixel Rate Range
00	12-30
01	30-60
10	60-140

The power-up default value is = 01.

03 5-3 CURRENT Charge Pump Current

Three bits that establish the current driving the loop filter in the clock generator.

Table 8. Charge Pump Currents

CURRENT	Current (μA)
000	50
001	100
010	150
011	250
100	350
101	500
110	750
111	1500

CURRENT must be set to correspond with the desired operating frequency (incoming pixel rate). See Table 5

The power-up default value is CURRENT = 001.

04 7-3 Clock Phase Adjust

A five-bit value that adjusts the sampling phase in 32 steps across one pixel time. Each step represents an 11.25° shift in sampling phase.

The power-up default value is 16.

Clamp Timing

05 7-0 Clamp Placement

An 8-bit register that sets the position of the internally generated clamp.

When EXTCLMP (Register 0Fh, Bit 7) = 0, a clamp signal is generated internally, at a position established by the clamp placement and for a duration set by the clamp duration. Clamping is started (Clamp Placement) an integral number of pixel periods after the trailing edge of Hsync. The clamp placement may be programmed to any value between 1 and 255. Values of 0,1,2,4,8,16,32,64,128 are not supported.

The clamp should be placed during a time that the input signal presents a stable black-level reference, usually the back porch period between Hsync and the image.

When EXTCLMP = 1, this register is ignored.

06 7-0 Clamp Duration

An 8-bit register that sets the duration of the internally generated clamp.

For the best results, the clamp duration should be set to include the majority of the black reference signal time that follows the Hsync signal trailing edge. Insufficient clamping time can produce brightness changes at the top of the screen, and a slow recovery from large changes in the Average Picture Level (APL), or brightness.

When EXTCLMP = 1, this register is ignored.

Hsync Output Pulsewidth

07 7-0 Hsync Output Pulse Width

An 8-bit register that sets the duration of the Hsync output pulse.

The leading edge of the Hsync output is triggered by the internally generated, phase-adjusted PLL feedback clock. The AD9883A then counts a number of pixel clocks equal to the value in this register minus one. This triggers the trailing edge of the Hsync output, which is also phase-adjusted.

Input Gain

08 7-0 Red Channel Gain Adjust

An 8-bit word that sets the gain of the RED channel. The AD9883A can accommodate input signals with a full-scale range of between 0.5V and 1.0V p-p. Setting REDGAIN to 255 corresponds to an input range of 1.0V. A REDGAIN of 0 establishes an input range of 0.5V. Note that INCREASING REDGAIN results in the picture having LESS CONTRAST (the input signal uses fewer of the available converter codes). See Figure 2.

09 7-0 Green Channel Gain Adjust

An 8-bit word that sets the gain of the GREEN channel. See REDGAIN (08).

0A 7-0 Blue Channel Gain Adjust

An 8-bit word that sets the gain of the BLUE channel. See REDGAIN (08).

Input Offset

0B 7-1 Red Channel Offset Adjust

A seven-bit offset binary word that sets the dc offset of the RED channel. One LSB of offset adjustment equals approximately one LSB change in the ADC

offset. Therefore, the absolute magnitude of the offset adjustment scales as the gain of the channel is changed. A nominal setting of 31 results in the channel nominally clamping the back porch (during the clamping interval) to code 00. An offset setting of 63 results in the channel clamping to code 31 of the ADC. An offset setting of 0 clamps to code -31 (off the bottom of the range). Increasing the value of Red Offset DECREASES the brightness of the channel.

0C 7-1 Green Channel Offset Adjust

A seven-bit offset binary word that sets the DC offset of the GREEN channel. See REDOFST (0B).

0D 7-1 Blue Channel Offset Adjust

A seven-bit offset binary word that sets the DC offset of the BLUE channel. See REDOFST (0B).

Mode Control 1

0E 7 Hsync Input Polarity Override

This register is used to override the internal circuitry that determines the polarity of the Hsync signal going into the PLL.

Table 9. Hsync Input Polarity Override Settings

Override Bit	Result
0	Hsync Polarity Determined by Chip
1	Hsync Polarity Determined by User

The default for Hsync polarity override is 0, (polarity determined by chip).

0E 6 HSPOL Hsync Input Polarity

A bit that must be set to indicate the polarity of the Hsync signal that is applied to the PLL Hsync input.

Table 10. Hsync Input Polarity Settings

HSPOL	Function
0	Active LOW
1	Active HIGH

Active LOW means the leading edge of the Hsync pulse is negative-going. All timing is based on the leading edge of Hsync, which is the FALLING edge. The rising edge has no effect.

Active HIGH means the leading edge of the Hsync pulse is positive-going. This means that timing will be based on the leading edge of Hsync, which is now the RISING edge.

The device will operate if this bit is set incorrectly, but the internally generated clamp position, as established by Clamp Placement (Register 05h), will not be placed as expected, which may generate clamping errors.

The power-up default value is HSPOL = 1.

0E 5 Hsync Output Polarity

One bit that determines the polarity of the Hsync output and the SOG output. Table 11 shows the effect of this option. SYNC indicates the logic state of the sync pulse.

Table 11. Hsync Output Polarity Settings

Setting	SYNC
0	Logic 1 (Positive Polarity)
1	Logic 0 (Negative Polarity)

The default setting for this register is 0.

0E 4 Active Hsync Override

This bit is used to override the automatic Hsync selection. To override, set this bit to logic 1. When overriding, the active Hsync is set via bit 3 in this register.

Table 12. Active Hsync Override Settings

Override	Result
0	Auto determine the active interface
1	Override, bit 3 determines the active interface.

The default for this register is 0.

0E 3 Active Hsync Select

This bit is used under two conditions. It is used to select the active Hsync when the override bit is set, (bit 4). Alternately, it is used to determine the active Hsync when not overriding but both Hsyncs are detected.

Table 13. Active Hsync Select Settings

Select	Result
0	Hsync input
1	Sync-on-green input

The default for this register is 0.

0E 2 Vsync Output Polarity

One bit that determines the polarity of the Vsync output. Table 14 shows the effect of this option. SYNC indicates the logic state of the sync pulse.

Table 14. Vsync Output Polarity Settings

Setting	SYNC
1	Logic 1 (Positive Polarity)
0	Logic 0 (Negative Polarity)

The default setting for this register is 0.

0E 1 Active Vsync Override

This bit is used to override the automatic Vsync selection. To override, set this bit to logic 1. When overriding, the active interface is set via bit 0 in this register.

Table 15. Active Vsync Override Settings

Override	Result
0	Auto determine the active Vsync
1	Override, bit 0 determines the active Vsync.

The default for this register is 0.

0E 0 Active Vsync Select

This bit is used to select the active Vsync when the override bit is set, (bit 1).

Table 16. Active Vsync Select Settings

Select	Result
0	Vsync input
1	Sync separator output

The default for this register is 0.

0F 7 Clamp Input Signal Source

A bit that determines the source of clamp timing.

Table 17. Clamp Input Signal Source Settings

EXTCLMP	Function
0	Internally generated clamp.
1	Externally-provided clamp signal

A 0 enables the clamp timing circuitry controlled by clamp placement and clamp duration. The clamp position and duration is counted from the leading edge of Hsync.

A 1 enables the external CLAMP input pin. The three channels are clamped when the CLAMP signal is active. The polarity of CLAMP is determined by the Clamp Polarity bit (Register 0Fh, Bit 6).

The power-up default value is EXTCLMP= 0.

0F 6 Clamp Input Signal Polarity

A bit that determines the polarity of the externally provided CLAMP signal.

Table 18. Clamp Input Signal Polarity Settings

EXTCLMP	Function
1	Active HIGH
0	Active LOW

A logic 1 means that the circuit will clamp when CLAMP is HIGH, and it will pass the signal to the ADC when CLAMP is LOW.

A logic 0 means that the circuit will clamp when CLAMP is LOW, and it will pass the signal to the ADC when CLAMP is HIGH.

The power-up default value is CLAMPOL= 1.

0F 5 Coast Select

This bit is used to select the active coast source. The choices are the coast input pin or Vsync. If Vsync is selected the additional decision of using the Vsync input pin or the output from the sync separator needs to be made, (register 0E, bits 1,0).

Select	Result
0	Coast input pin
1	Vsync (see above text)

The default for this register is 0.

0F 4 Coast Input Polarity Override

This register is used to override the internal circuitry that determines the polarity of the coast signal going into the PLL.

Table 19. Coast Input Polarity Override Settings

Override Bit	Result
0	Coast Polarity Determined by Chip
1	Coast Polarity Determined by User

The default for coast polarity override is 0.

0F 3 Coast Input Polarity

A bit to indicate the polarity of the COAST signal that is applied to the PLL COAST input.

Table 20. Coast Input Polarity Settings

CSTPOL	Function
0	Active LOW
1	Active HIGH

Active LOW means that the clock generator will ignore Hsync inputs when COAST is LOW, and continue operating at the same nominal frequency until COAST goes HIGH.

Active HIGH means that the clock generator will ignore Hsync inputs when COAST is HIGH, and continue operating at the same nominal frequency until COAST goes LOW.

This function needs to be used along with the COAST polarity override bit, (bit 4).

The power-up default value is CSTPOL= 1.

0F 2 Seek Mode Override

This bit is used to either allow or dis-allow the low-power mode. The low-power mode (seek mode) occurs when there are no signals on any of the Sync inputs.

Table 21. Seek Mode Override Settings

Select	Result
1	Allow Seek Mode
0	Disallow Seek Mode

The default for this register is 1.

0F 1 PWRDN

This bit is used to put the chip in full powerdown. See the section on power management for details of which blocks are actually powered down.

Table 22. Powerdown Settings

Select	Result
0	Powerdown
1	Normal operation

The default for this register is 1.

10 7-3 Sync-on-Green Slicer Threshold

This register allows the comparator threshold of the Sync-on-Green slicer to be adjusted. This register adjusts it in steps of TBD mV, with the minimum setting equaling TBD mV and the maximum setting equaling TBD mV.

The default setting is 23 and corresponds to a threshold value of 0.15V.

10 2 Red Clamp Select

A bit that determines whether the red channel is clamped to ground or to midscale. For RGB video, all three channels are referenced to ground. For YcbCr (or YUV), the Y channel is referenced to ground, but the CbCr channels are referenced to midscale. Clamping to mid-scale actually clamps to pin 37.

Table 23. Red Clamp Select Settings

Clamp	Function
0	Clamp to ground
1	Clamp to midscale, (pin 37)

The default setting for this register is 0.

10 1 Green Clamp Select

A bit that determines whether the green channel is clamped to ground or to mid-scale.

Table 24. Green Clamp Select Settings

Clamp	Function
0	Clamp to ground
1	Clamp to midscale, (pin 37)

The default setting for this register is 0.

10 0 Blue Clamp Select

A bit that determines whether the blue channel is clamped to ground or to mid-scale.

Table 25. Blue Clamp Select Settings

Clamp	Function
0	Clamp to ground
1	Clamp to midscale, (pin 37)

The default setting for this register is 0.

11 7:0 Sync Separator Threshold

This register is used to set the responsiveness of the sync separator. It sets how many internal 5MHz clock periods the sync separator must count to before toggling high or low. It works like a low-pass filter to ignore Hsync pulses in order to extract the Vsync signal. This register should be set to some number greater than the maximum Hsync pulse width. Note: the sync separator threshold uses an internal dedicated clock with a frequency of approximately 5MHz.

The default for this register is 32.

12 7-0 Pre-Coast

This register allows the coast signal to be applied prior to the Vsync signal. This is necessary in cases where pre-equalization pulses are present. The step size for this control is one Hsync period.

The default is 0.

13 7-0 Post-Coast

This register allows the coast signal to be applied following to the Vsync signal. This is necessary in cases where post-equalization pulses are present. The step size for this control is one Hsync period.

The default is 0.

14 7 Hsync Detect

This bit is used to indicate when activity is detected on the Hsync input pin, (pin 30). If Hsync is held high or low, activity will not be detected.

Table 26. Hsync Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The sync processing block diagram on page 29 shows where this function is implemented.

14 6 AHS – Active Hsync

This bit indicates which Hsync input source is being used by the PLL (Hsync input or sync-on-green). Bits 7 and 1 in this register are what determine which source is used. If both Hsync and SOG are detected the user can determine which has priority via bit 3 in register 0EH. The user can override this function via bit 4 in register 0EH. If the override bit is set to logic 1, then this bit will be forced to whatever the state of bit 3 in register 0EH is set to.

Table 27. Active Hsync Results

Bit 7 (Hsync Detect)	Bit 1 (SOG Detect)	Bit 4, Reg 0EH (Override)	AHS
0	0	0	Bit 3 in 0EH
0	1	0	1
1	0	0	0
1	1	0	Bit 3 in 0EH
X	X	1	Bit 3 in 0EH

AHS = 0 means use the Hsync pin input for Hsync

AHS = 1 means use the SOG pin input for Hsync

The override bit is in register 0EH, bit 4

14 5 Detected Hsync Input Polarity Status

This bit reports the status of the Hsync input polarity detection circuit. It can be used to determine the polarity of the Hsync input. The detection circuit's location is shown in the Sync Processing Block Diagram, (Page 29).

Table 28. Detected Hsync Input Polarity Status

Hsync Polarity Status	Result
0	Hsync Polarity is Negative
1	Hsync Polarity is Positive

14 4 Vsync Detect

This bit is used to indicate when activity is detected on the Vsync input pin, (pin 31). If Vsync is held high or low, activity will not be detected.

Table 29. Vsync Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The sync processing block diagram on page 29 shows where this function is implemented.

14 3 AVS – Active Vsync

This bit indicates which Vsync source is being used; the Vsync input or output from the sync separator. Bit 4 in this register is what determines which is active. If both Vsync and SOG are detected the user can determine which has priority via bit 0 in register 0EH. The user can override this function via bit 1 in register 0EH. If the override bit is set to logic 1, then this bit will be forced to whatever the state of bit 0 in register 0EH is set to.

Table 30. Active Vsync Results

Bit 5 (Vsync Detect)	Override	AVS
0	0	0
1	0	1
X	1	Bit 0 in 0EH

AVS = 0 means Sync separator

AVS = 1 means Vsync input

The override bit is in register 0EH, bit 1

14 2 Detected Vsync Input Polarity Status

This bit reports the status of the Vsync input polarity detection circuit. It can be used to determine the polarity of the Vsync input. The detection circuit's location is shown in the Sync Processing Block Diagram, (Page 29).

Table 31. Detected Vsync Input Polarity Status

Vsync Polarity Status	Result
0	Vsync Polarity is Active High
1	Vsync Polarity is Active Low

14 1 Sync-on-Green Detect

This bit is used to indicate when sync activity is detected on the sync-on-green input pin, (pin 49).

Table 32. Sync-on-Green Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The sync processing block diagram on page 29 shows where this function is implemented.

14 0 Detected COAST Polarity Status

This bit reports the status of the coast input polarity detection circuit. It can be used to determine the polarity of the coast input. The detection circuit's location is shown in the Sync Processing Block Diagram, (Page 29).

Table 33. Detected Coast Input Polarity Status

Hsync Polarity Status	Result
0	Coast Polarity is Negative
1	Coast Polarity is Positive

15 7 4:2:2 Output Mode Select

A bit that configures the output data in 4:2:2 mode This mode can be used to reduce the number of data lines used from 24 down to 16 for applications using YUV, YCbCr, or YPbPr graphics signals. . A timing diagram for this mode is shown on page 17. Recommended input and output configurations are shown in Table 35. In 4:2:2 mode, the red and blue channels can be interchanged to help satisfy board layout or timing requirements, but the green channel must be configured for Y.

Table 34. 4:2:2 Output Mode Select

Select	Output Mode
0	4:4:4
1	4:2:2

Table 35. 4:2:2 Input/Output Configuration

Channel	Input Connection	Output Format
Red	V	U/V
Green	Y	Y
Blue	U	High Impedance

Two-Wire Serial Control Port

A two-wire serial interface control interface is provided. Up to four AD9883A devices may be connected to the two-wire serial interface, with each device having a unique address.

The two-wire serial interface comprises a clock (SCL) and a bi-directional data (SDA) pin. The Analog Flat Panel Interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is LOW. If SDA changes state while SCL is HIGH, the serial interface interprets that action as a start or stop sequence.

There are six components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL and SDA are HIGH) communications are initiated by sending a start signal. The start signal is a HIGH-to-LOW transition on SDA while SCL is HIGH. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprising a seven bit slave address (the first seven bits) and a single R/W\ bit (the eighth bit). The R/W\ bit indicates the direction of data transfer, read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA_{1-0} input pins in *Table 36*), the AD9883A acknowledges by bringing SDA LOW on the 9th SCL pulse. If the addresses do not match, the AD9883A does not acknowledge.

Table 36. Serial Port Addresses

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
A_6 (MSB)	A_5	A_4	A_3	A_2	A_1	A_0
1	0	0	1	1	0	0
1	0	0	1	1	0	1

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the AD9883A does not acknowledge the master device during a write sequence, the SDA remains HIGH so the master can generate a stop signal. If the master device does not acknowledge the AD9883A during a read sequence, the AD9883A interprets this as "end of data." The SDA remains HIGH so the master can generate a stop signal.

Writing data to specific control registers of the AD9883A requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 14h. Any base address higher than 14h will not produce an ACKnowledge signal.

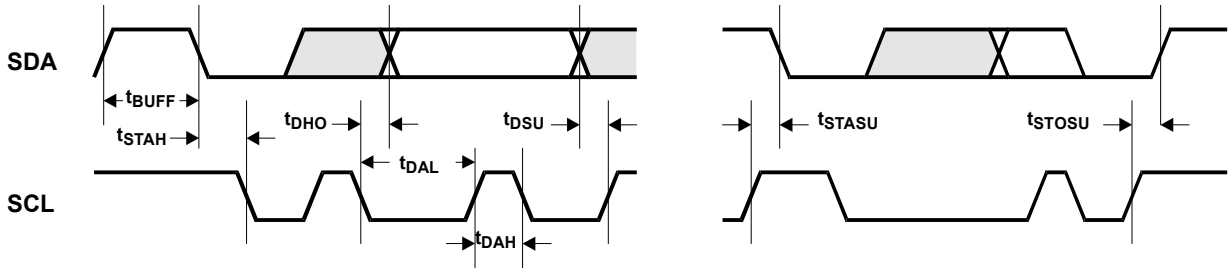


Figure 8. Serial Port Read/Write Timing

Data are read from the control registers of the AD9883A in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W\ bit of the slave address byte LOW to set up a sequential read operation.

Reading (the R/W\ bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the AD9883A, a stop signal must be sent. A stop signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Write to one control register
- Start signal
- Slave Address byte (R/W\ bit = LOW)
- Base Address byte
- Data byte to base address
- Stop signal

Write to four consecutive control registers
- Start signal
- Slave Address byte (R/W\ bit = LOW)
- Base Address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

Read from one control register
- Start signal
- Slave Address byte (R/W\ bit = LOW)
- Base Address byte
- Start signal
- Slave Address byte (R/W\ bit = HIGH)
- Data byte from base address
- Stop signal

Read from four consecutive control registers
- Start signal
- Slave Address byte (R/W\ bit = LOW)
- Base Address byte
- Start signal
- Slave Address byte (R/W\ bit = HIGH)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

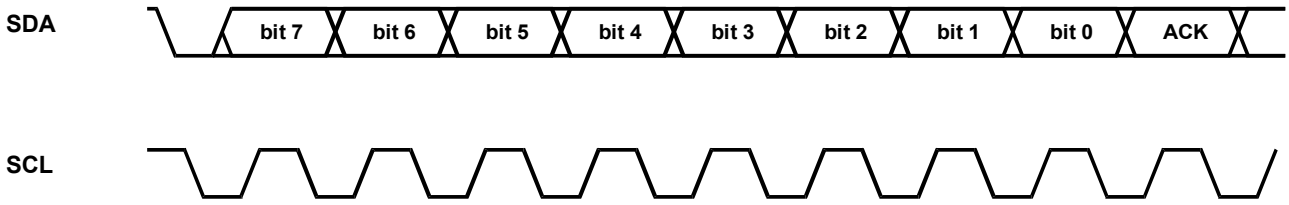


Figure 9. Serial Interface - Typical Byte Transfer

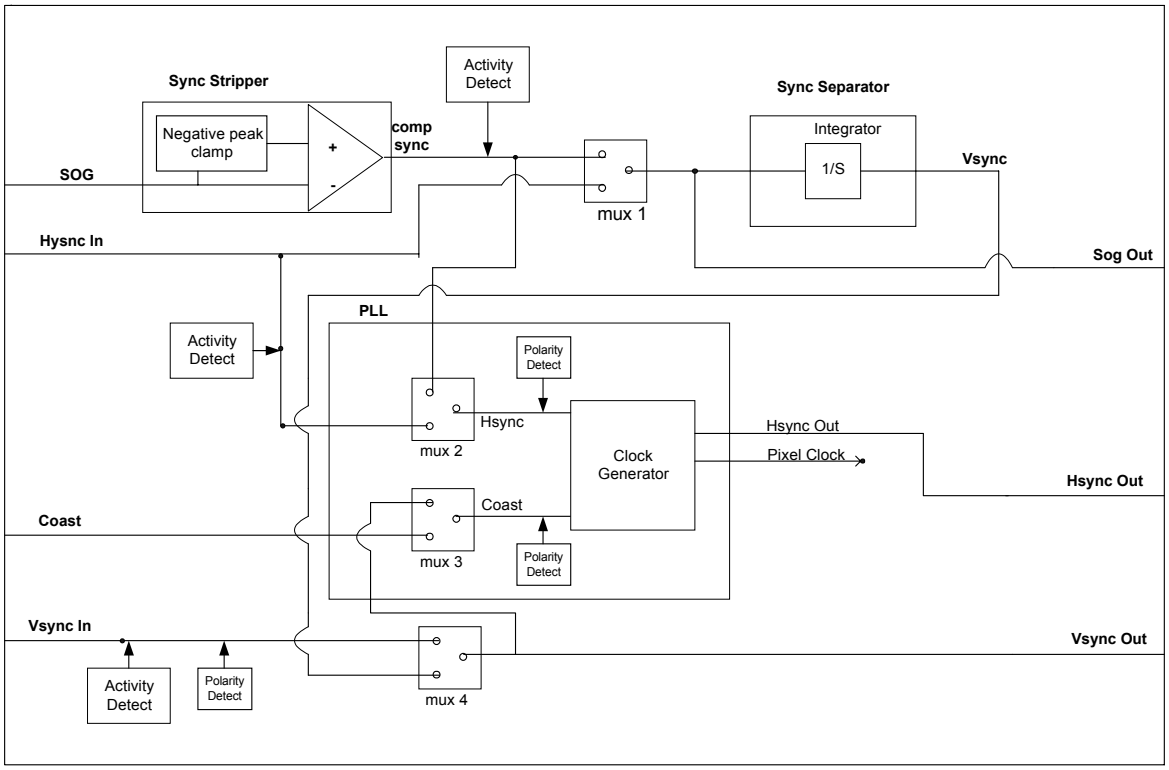


Figure 10. Sync Processing Block Diagram

Mux Number(s)	Serial Bus Control Bit	Control Bit State	Result
1 and 2	0EH: Bit 3	0	Pass Hsync
		1	Pass Sync-on-green
3	0FH: Bit 5	0	Pass Coast
		1	Pass Vsync
4	0EH: Bit 0	0	Pass Vsync
		1	Pass Sync Separator Signal

Table 37. Control of the Sync Block Muxes via the Serial Register

Sync Slicer

The purpose of the sync slicer is to extract the sync signal from the green graphics channel. A sync signal is not present on all graphics systems, only those with "sync-on-green". The sync signal is extracted from the green channel in a two step process. First, the SOG input is clamped to its negative peak, (typically 0.3V below the black level). Next, the signal goes to a comparator with a variable trigger level, nominally 0.15V above the clamped level. The "sliced" sync is typically a composite sync signal containing both Hsync and Vsync.

Sync Separator

A sync separator extracts the Vsync signal from a composite sync signal. It does this through a low pass filter-like or integrator-like operation. It works on the idea that the Vsync signal stays active for a much longer time than the Hsync signal. So, it rejects any signal shorter than a threshold value, which is somewhere between an Hsync pulse width and a Vsync pulse width.

The sync separator on the AD9883A is simply an 8-bit digital counter with a 5MHz clock. It works independently of the polarity of the composite sync signal. (Polarities are determined elsewhere on the chip.) The basic idea is that the counter counts up when Hsync pulses are present. But since Hsync pulses are relatively short in width, the counter only reaches a value of N before the pulse ends. It then starts counting down eventually reaching 0 before the next Hsync pulse arrives. The specific value of N will vary for different video modes, but will always be less than 255. For example with a 1uS width Hsync, the counter will only reach 5 (1us/200nS = 5). Now, when Vsync is present on the composite sync the counter will also count up. However, since the Vsync signal is much longer, it will count to a higher number M. For most video modes, M will be at least 255. So, Vsync can be detected on the composite sync signal by detecting when the counter counts to higher than N. The specific count that triggers detection (T) can be programmed through the serial register (0fh).

Once Vsync has been detected, there is a similar process to detect when it goes inactive. At detection, the counter first resets to 0, then starts counting up when Vsync goes away. Similar to the previous case, it will detect the absence of Vsync when the counter reaches the threshold count (T). In this way, it will reject noise and/or serration pulses. Once Vsync is detected to be absent, the counter resets to 0 and begins the cycle again

PCB LAYOUT RECOMMENDATIONS

The AD9883A is a high-precision, high-speed analog device. In order to achieve the maximum performance out of the part it is important to have a well laid-out board. The following is a guide for designing a board using the AD9883A.

Analog Interface Inputs

Using the following layout techniques on the graphics inputs is extremely important:

Minimize the trace length running into the graphics inputs. This is accomplished by placing the AD9883A as close as possible to the graphics VGA connector. Long input trace lengths are undesirable because they will pick up more noise from the board and other external sources.

Place the 75 ohm termination resistors (see Figure 1) as close to the AD9883A chip as possible. Any additional trace length between the termination resistors and the input of the AD9883A increases the magnitude of reflections, which will corrupt the graphics signal.

Use 75 ohm matched impedance traces. Trace impedances other than 75 ohms will also increase the chance of reflections.

The AD9883A has very high input bandwidth, (300MHz). While this is desirable for acquiring a high resolution PC graphics signal with fast edges, it means that it will also capture any high frequency noise present. Therefore, it is important to reduce the amount of noise that gets coupled to the inputs. Avoid running any digital traces near the analog inputs.

Due to the high bandwidth of the AD9883A, sometimes low-pass filtering the analog inputs can help to reduce noise. (For many applications, filtering is unnecessary.) Experiments have shown that placing a series ferrite bead prior to the 75 ohm termination resistor is helpful in filtering out excess noise. Specifically, the part used was the # 2508051217Z0 from Fair-Rite, but each application may work best with a different bead value. Alternately, placing a 100 to 120 ohm resistor between the 75 ohm termination resistor and the input coupling capacitor can also benefit.

Power Supply Bypassing

It is recommended to bypass each power supply pin with a 0.1uF capacitor. The exception is in the case where two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is only necessary to have one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board

from the AD9883A, as that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane => capacitor => power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of PVd (the clock generator supply). Abrupt changes in PVd can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (Vd and PVd).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PVd, from a different, cleaner, power source (for example, from a +12V supply).

It is also recommend to use a single ground plane for the entire board. Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases, it is recommend to at least place a single ground plane under the AD9883A. The location of the split should be at the receiver of the digital outputs. For this case it is even more important to place components wisely because the current loops will be much longer, (current takes the path of least resistance). An example of a current loop: power plane => AD9883A => digital output trace => digital data receiver => digital ground plane => analog ground plane.

PLL

Place the PLL loop filter components as close to the FILT pin as possible.

Do not place any digital or other high frequency traces near these components.

Use the values suggested in the datasheet with 10% tolerances or less.

Outputs (both data and clocks)

Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance, which require more current that causes more internal digital noise.

Shorter traces reduce the possibility of reflections.

Adding a series resistor of value 50-200 ohms can suppress reflections, reduce EMI, and reduce the current spikes inside of the AD9883A. If series resistors are used, place them as close to the AD9883A pins as possible, (although try not to add vias or extra length to the output trace in order to get the resistors closer).

If possible, limit the capacitance that each of the digital outputs drives to less than 10pF. This can easily be accomplished by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance will increase the current transients inside of the AD9883A creating more digital noise on its power supplies.

Digital Inputs

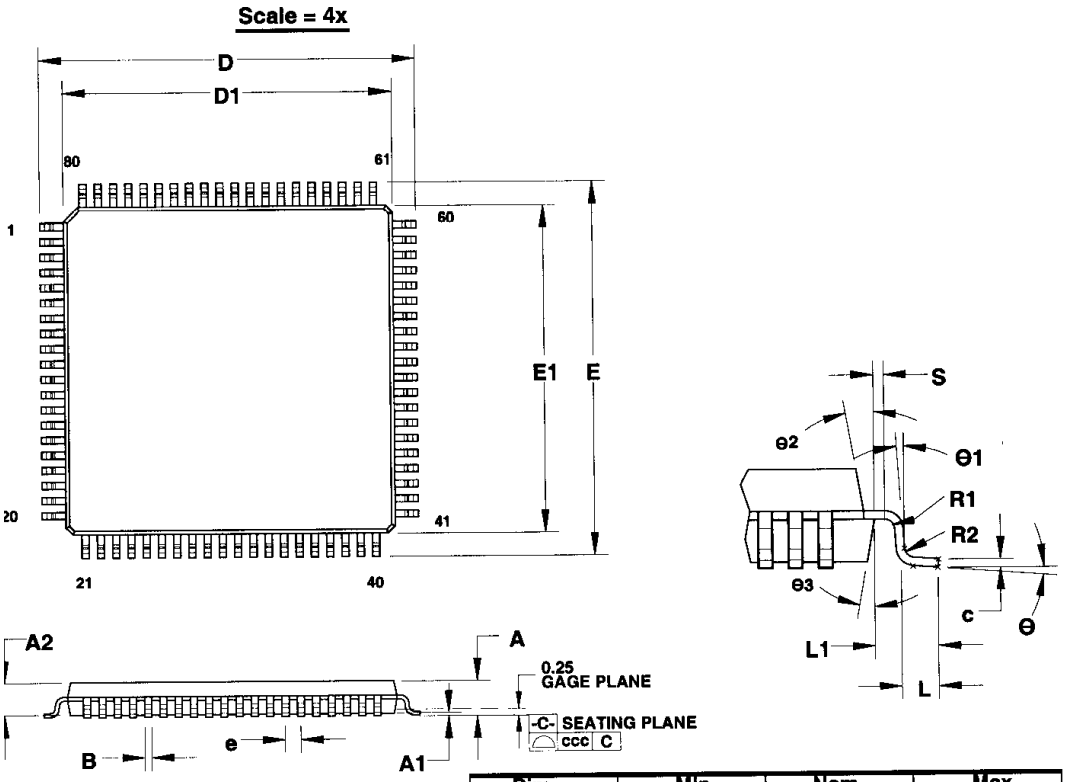
The digital inputs on the AD9883A were designed to work with 3.3V signals, but are tolerant of 5.0V signals. So, no extra components need to be added if using 5.0V logic .

Any noise that gets onto the Hsync input trace will add jitter to the system. Therefore, minimize the trace length and do not run any digital or other high frequency traces near it.

Voltage Reference

Bypass with a 0.1uF capacitor. Place as close to the AD9883A pin as possible. Make the ground connection as short as possible.

Package Drawing



Dim	Min.	Nom.	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
D		16.00 BSC	
D1		14.00 BSC	
E		16.00 BSC	
E1		14.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
B	0.22	0.32	0.38
e		0.65 BSC	
θ	0°	3.5°	7°
θ1	0°		
θ2	11°	12°	13°
θ3	11°	12°	13°
R1	0.08		
R2	0.08		0.20
c	0.09		0.20
S	0.20		
ccc			0.10

ES:

Dimensions per JEDEC Standards MO-136-BQ
ntrolling Dimensions are in mm.

80 LEAD TQFP
14 x 14 x 1.4 mm
Package Outline
Customer