NCP81162

Current Balancing Phase Doubler

The NCP81162 is a current balancing, 3−level PWM input, phase doubler. The part is intended to double the number of phases directly controlled by ON Semiconductor PWM controllers that have 3−level PWM output signals. The NCP81162 monitors the current of two phases to determine which of those two phases should receive the next PWM pulse output sent by the controller. This maintains effective current balance even during dynamic loading of the output.

Features

- Works with Controllers having 3−level PWM Outputs
- Reproduces 3−level PWM Signals to Drivers
- Very Short Delay
- Doubles Single−phase to 2−phase
- Multiple Doublers can Double N Phases to 2 x N Phases
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Current Multiphase Applications
- Expand the Single−phase Rail of a Dual Rail Controller to 2 Phases

ON Semiconductor®

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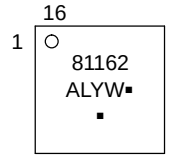
QFN16
MN SUFFIX
CASE 485AE

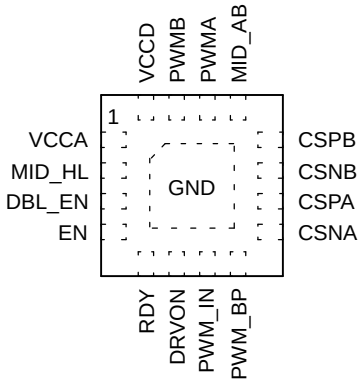
MARKING DIAGRAM



81162 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN DESCRIPTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81162MNR2G	QFN16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

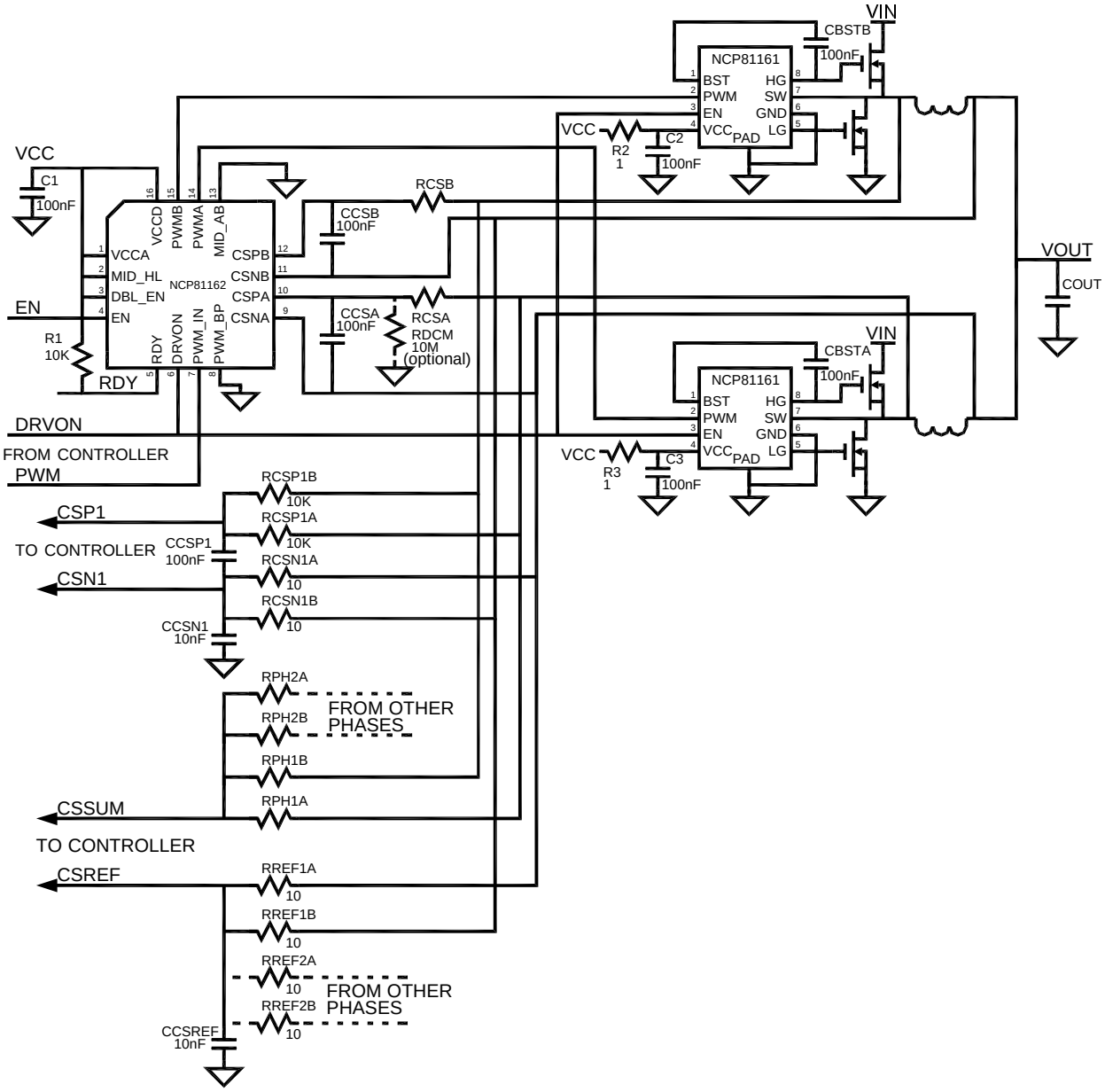


Figure 1. Application Schematic

Table 1. PIN LIST DESCRIPTION

Pin No.	Symbol	Description
1	VCCA	5 V Analog Supply
2	MID_HL	Logic input. When high, the PWMA and PWMB mid−state output voltages are higher.
3	DBL_EN	Logic input. When high, PWM_IN pulses are distributed to the phase with lower output current. When low, all PWM_IN pulses are sent to the PWMA output and the PWMB output is held at mid−state.
4	EN	Logic input. Once EN & DRVON are simultaneously high, the NCP81162 is enabled.
5	RDY	Open collector output. When a pullup resistor is attached, a high output indicates PWMA & PWMB will respond to the PWM_IN input.
6	DRVON	Logic input. After enabling, PWMA & PWMB outputs are active when DRVON is high.
7	PWM_IN	Logic input. The controller PWM output which will actively control PWMA & PWMB
8	PWM_BP	Logic input. When high, both PWMA and PWMB follow PWM_IN.
9	CSNA	Phase A negative differential current sense input
10	CSPA	Phase A positive differential current sense input
11	CSNB	Phase B negative differential current sense input
12	CSPB	Phase B positive differential current sense input
13	MID_AB	Logic input. If high, the doubler PWM output that is low when PWM_IN is high will not transition to mid−state upon the first PWM_IN H→MID transition.
14	PWMA	3−level doubler PWM output A
15	PWMB	3−level doubler PWM output B
16	VCCD	Power supply input for PWMA & PWMB outputs and internal digital circuitry
FLAG	GND	Power supply return (QFN Flag)

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range (Note 1)			
Maximum Junction Temperature	$T_{J(max)}$	125	°C
Storage Temperature Range	T_{STG}	−40 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to MAXIMUM ELECTRICAL RATINGS.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. MAXIMUM ELECTRICAL RATINGS

Pin Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
VCCA, VCCD	6.5 V	−0.3 V	N/A	N/A
PWMA PWMB	N/A	N/A	10 mA	10 mA
RDY	6.5 V	−0.3 V	NA	10 mA
All Other Pins	VCCA + 0.3 V	−0.3 V	N/A	N/A

*All signals referenced to GND unless noted otherwise.

Table 4. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, QFN16, 3 x 3 mm (Note 4) Thermal Resistance, Junction−to−Air (Note 5) Thermal Resistance, Junction−to−Lead (Note 5)	 $R_{\theta JA}$ $R\psi_{JL}$	 107 42	°C/W

4. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM.
5. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

Table 5. ELECTRICAL CHARACTERISTICS:
Unless otherwise stated: −40°C < T_A < 125°C; 4.75 V < VCCA & VCCD < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Condition	Min	Typ	Max	Units
BIAS SUPPLY					
VCCA + VCCD Quiescent Current	EN = high, PWM_IN freq = 500 kHz, PWMA/B load 20 pF		1.6	2.0	mA
	EN = low		10		μA
VCCA UVLO					
VCCA UVLO Threshold	VCCA rising		3.7	3.95	V
	VCCA falling	3.3	3.5		V
VCCA UVLO Hysteresis			200		mV
Power ON Reset Release Delay	EN = H; Time from rising VCCA UVLO clearing to when PWMA & PWMB go to Mid−state		85		μs
EN INPUT					
Enable High Input Leakage Current	External 1K pull−up to 3.3 V	−		1.0	μA
Upper Threshold	V_{UPPER}			0.8	V
Lower Threshold	V_{LOWER}	0.4			V
Total Hysteresis	$V_{UPPER} - V_{LOWER}$		100		mV
Power On Reset Release Delay	From EN → H to PWMA/PWMB = Mid−state		85		μs
Calibration Time	From EN → H to RDY = Open		250	500	μs
	DRVON = H; From EN → H to PWMA/PWMB follow PWM_IN		250	500	μs
Disable Delay	DRVON = L; From EN → L to RDY = L & PWMA/PWMB = Open		380		ns
RDY OUTPUT					
Output Low Saturation Voltage	EN = DRVON = L; I_{VR_RDY} = 3 mA	−	−	0.3	V
Output High Leakage	EN = H; V_{RDY} = VCC	−	−	1	μA
DRVON INPUT					
Threshold			VCCD/2		V
Hysteresis			313		mV
PWMA & PWMB Response Delay	DRVON rising		244		ns
	DRVON falling		44		ns
PWM_IN INPUT					
Input Bias Current				400	nA
Rising High Threshold				3.4	V
Falling High MID State Threshold		2.7			V
Rising Low MID State Threshold				1.3	V
Falling Low Threshold		0.7			V
Rise & Fall Times				12	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. ELECTRICAL CHARACTERISTICS:
Unless otherwise stated: −40°C < T_A < 125°C; 4.75 V < VCCA & VCCD < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Condition	Min	Typ	Max	Units
PWMA PWMB OUTPUTS					
Output High Voltage	Sourcing 500 μA	VCCD−0.2	VCCD		V
Output Low Voltage	Sinking 500 μA		GND	0.2	V
Output MID−State Voltage	MID_HL = GND	1.4		1.6	V
	MID_HL = VCCA	1.9		2.1	V
10% to 90% Rise and Fall Time (not tested in production)	CL (PCB) = 20 pF, ΔVo = GND to VCCA			10	ns
PWM_IN Response Delay	PWM_IN L → H or H → L		15	50	ns
	PWM_IN X → Mid		37		ns
	PWM_IN Mid → X		24		ns
Pulsewidth Difference from PWM_IN	PWM_IN pulsewidth > 15 ns		2		ns
DIFFERENTIAL CURRENT SENSE COMPARATOR					
CSP Input Voltage Range		−0.3	−	2.0	V
CSN Input Voltage Range		−0.3	−	2.0	V
Offset Accuracy		−1.25		1.25	mV
Input Bias Current		−400	−	400	nA
PWM_BP INPUT					
Threshold			VCCD/2		V
Hysteresis			250		mV
PWMA/PWMB Response Delay			14		ns
MID_HL & MID_AB INPUTS					
Threshold			VCCD/2		V
Hysteresis			220		mV
DBL_EN					
Threshold			1.95		V
Hysteresis			100		mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. LOGIC TABLE

Inputs							Outputs		
VCC	**MID_AB**	**DBL_EN**	**EN**	**DRVON**	**PWM_IN**	**PWM_BP**	**RDY**	**PWMA**	**PWMB**
L	X	X	X	X	X	X	L	OPEN	OPEN
X	X	X	L	L	X	X	L	OPEN	OPEN
H	X	X	H	L	X	X		MID (Note 6)	MID (Note 6)
H	X	X	H	X	X	X	OPEN (Note 7)		
H	X	L	X (Note 8)	H	H	L		H	MID
H	X	L	X (Note 8)	H	MID	L		MID	MID
H	X	L	X (Note 8)	H	L	L		L	MID
H	X	H	X (Note 8)	H	X−>>H	L		H (Note 9)	H (Note 10)
H	L	H	X (Note 8)	H	H−>>MID	L		MID	MID
H	H	H	X (Note 8)	H	H−>>MID	L		MID (Note 11)	MID (Note 11)
H	X	H	X (Note 8)	H	L−>>MID	L		MID	MID
H	X	H	X (Note 8)	H	L	L		L	L
H	X	H	X (Note 8)	H	H	H		H	H
H	X	H	X (Note 8)	H	MID	H		MID	MID
H	X	H	X (Note 8)	H	L	H		L	L

6. Following Power−on−reset release delay after VCC & EN are both high
7. Following calibration delay after VCC & EN are both high
8. EN and DRVON never both L after both simultaneously H
9. If CSPA−CSNA < CSPB−CSNB; otherwise: previous state (MID or L)
10. If CSPB−CSNB < CSPA−CSNA; otherwise: previous state (MID or L)
11. If was H; otherwise: previous state (MID or L)

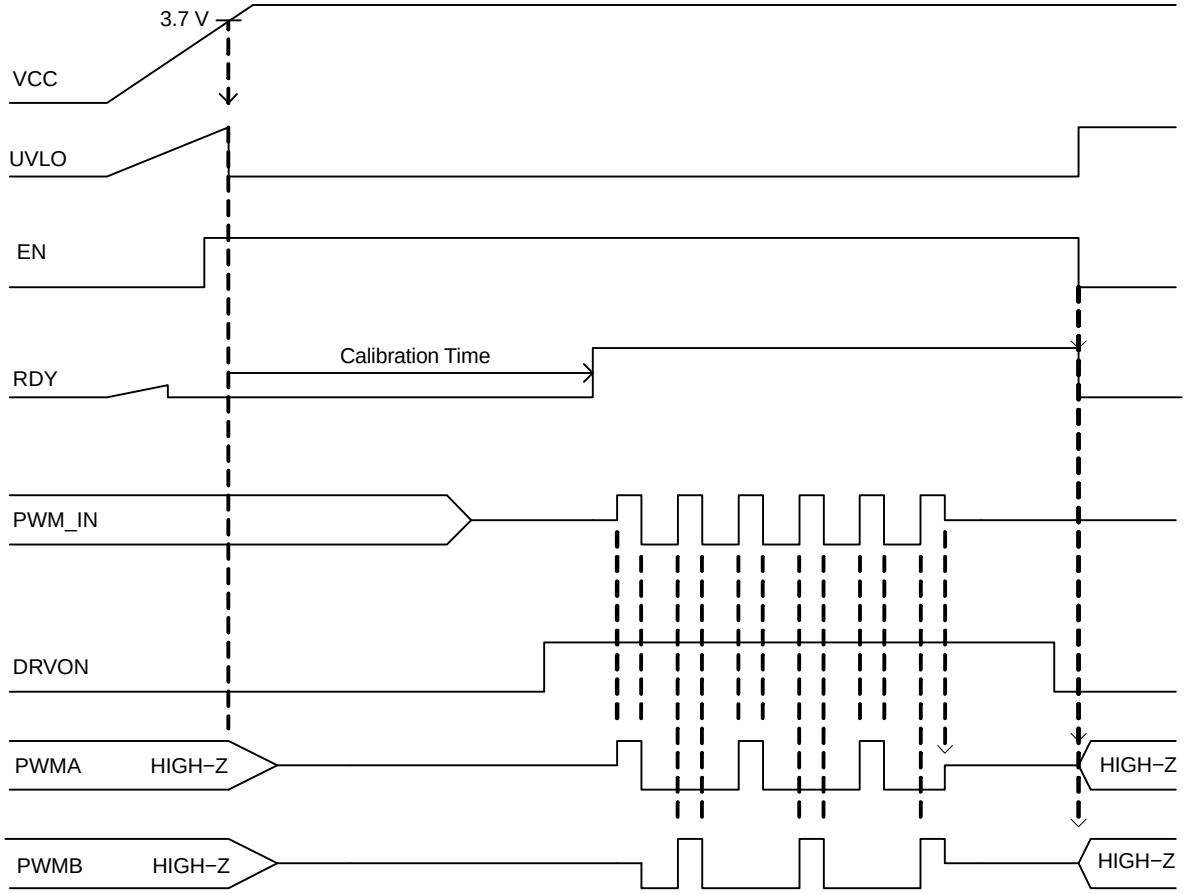


Figure 2. Startup Timing Diagram

General

The NCP81162 is a phase doubler IC specifically designed to distribute a 3−level PWM signal output from a controller to two phases. The doubler allocates the PWM pulses between the phases based on current feedback, in order to maintain cycle−by−cycle current balance.

PWM Doubling Function

The NCP81162 steers an incoming PWM pulse from the controller to the phase with lower current, in order to maintain current balance. During steady state loading, every second input pulse is usually allocated to the same one of the two doubler PWM outputs. This alternating allocation is produced by monitoring the instantaneous current of both inductors, and reproducing the entire PWM input pulse at the PWM output having lower current at the moment the PWM input rises. Alternating of PWM output pulses stops, in order to swap the phase order, if the current in the phase receiving the last pulse is still less than the current in the other phase at the moment the next PWM input pulse arrives. During both steady state and dynamic loading, the current is thereby balanced on a pulse by pulse basis.

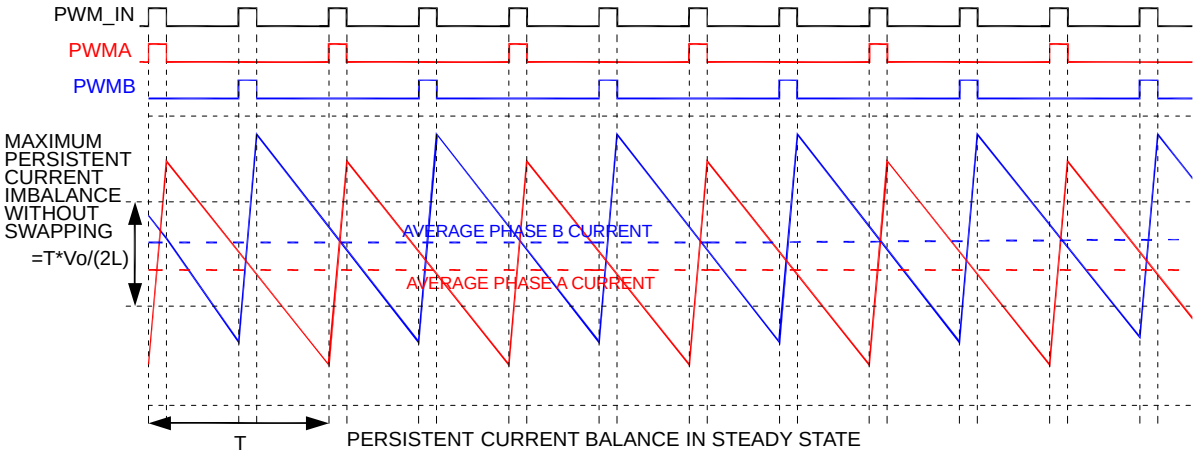


Figure 3. Persistent Current Balance in Steady State

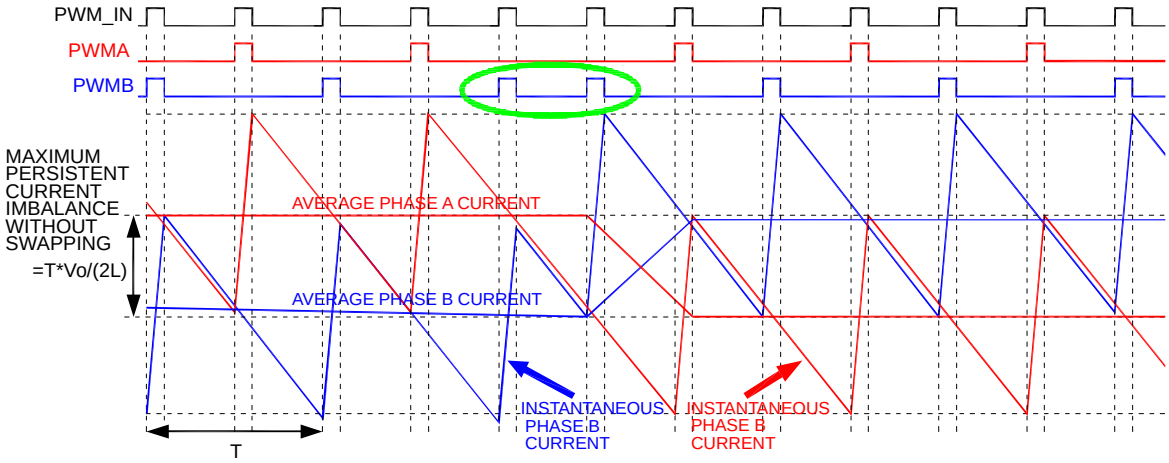


Figure 4. Gradual Change of Current Balance Past Limit

If current gradually becomes unbalanced due to slight differences in phase resistance, duty cycle, or some other cause, the instantaneous current of the phase that received the last PWM pulse may eventually not have risen above the current of the other phase during the on time. Since the NCP81162 continues to steer each incoming PWM pulse to the phase with lowest instantaneous current (in this case, the same phase that received the last pulse), two consecutive PWM_IN pulses will be steered to the same phase (see Figure 4). Although current balance is changed in the proper direction, the resulting new current balance may be close to the opposite limit of imbalance, and additional current balance changes may occur.

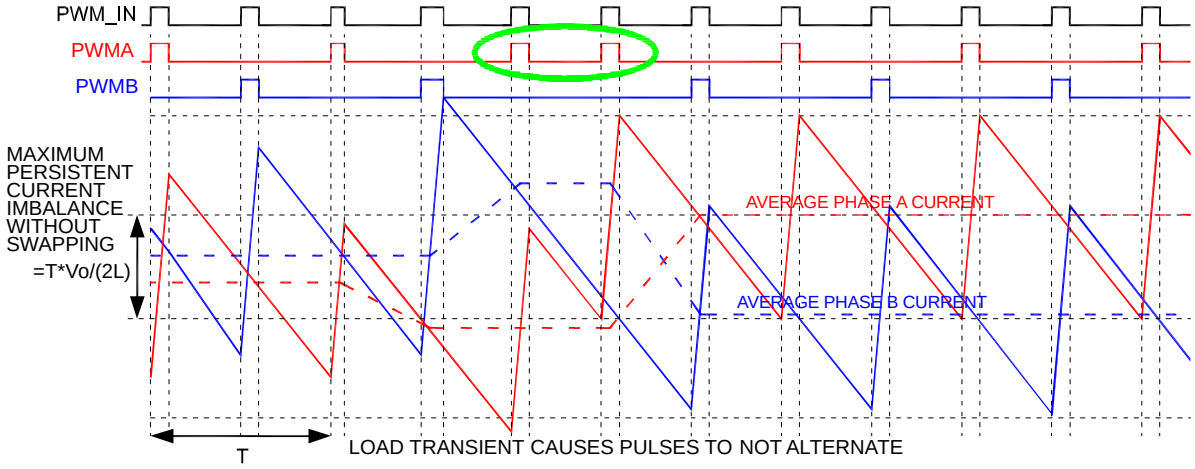


Figure 5. Sudden Change of Current Balance Past Limit

When a sudden change in either load current or input voltage occurs, phase currents can quickly become unbalanced. The NCP81162 immediately responds to an imbalance if it is enough that the current of one phase never exceeds the other (See Figure 5).

If the system is operating in a DCM mode, PWM allocation will continue to be based on the current sense feedback. If the current in both phases is zero when the PWM pulse arrives at the doubler, the phase which receives it may be randomly selected or have a tendency to favor one phase, based on the input offset of the current comparator.

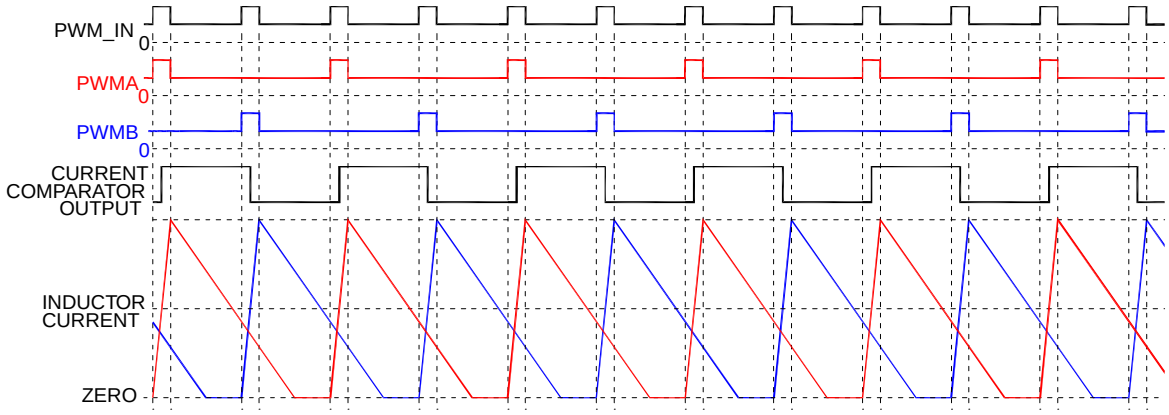


Figure 6. Discontinuous Current with Phase Current Overlap

When the PWM_IN input signal transitions only between mid−level and high, the PWMA and PWMB outputs also only transition between mid−level and high. This allows inductor current to become discontinuous (DCM) if the power stage synchronous rectifier is controlled by a driver with Zero Current Detection (ZCD), or Diode Emulation capability. If DCM operation is required, the controller must not implement the ZCD function. This is because phase currents are summed at the controller CS input − preventing it from sensing zero current until the sum of the currents is zero, which for 180° out of phase currents does not occur until average current is below zero.

By splitting current into 2 phases, DCM and the associated increased efficiency will occur at a higher load current than a single phase operating at the same frequency. This is because the current in each phase is lower when load current is shared between 2 phases and each phase achieves DCM independently.

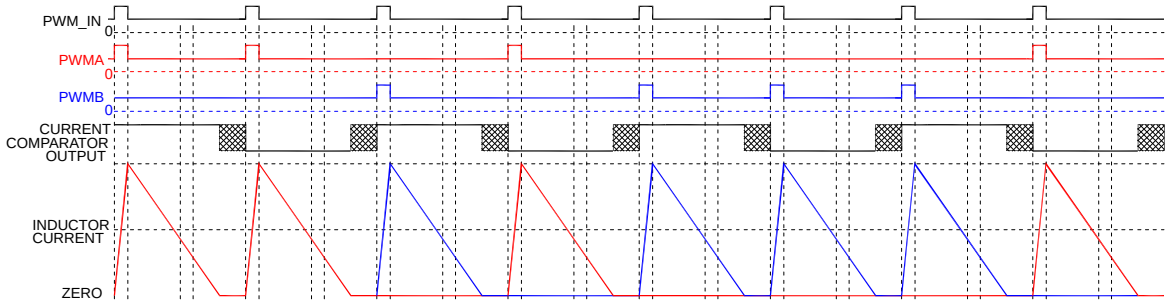


Figure 7. Discontinuous Current with no Phase Current Overlap – No CS Biasing

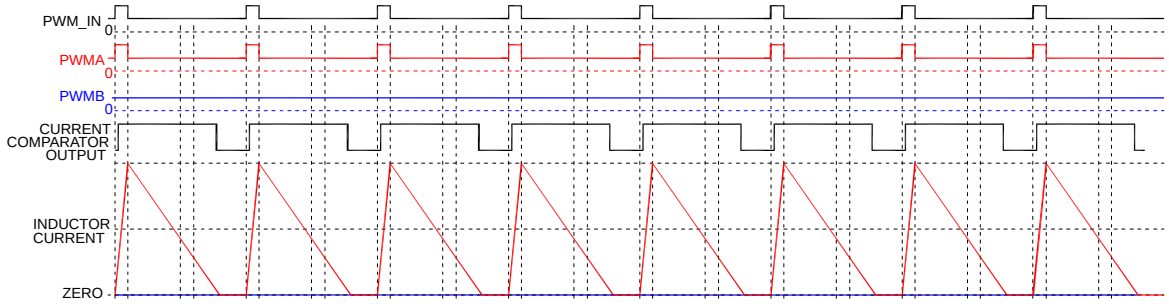


Figure 8. Discontinuous Current with no Phase Current Overlap − CS Biasing

If activation of only 1 phase is desired when DCM phase currents do not overlap, a small offset can be introduced into the NCP81162 current sense network by use of RDCM shown in Figure 1. This resistor should be the highest value that reliably forces off one phase during DCM, since the slight current imbalance thereby created will also exist at higher load currents. Sufficient offset should result from a RDCM value of Vout x RCSA/0.0004.

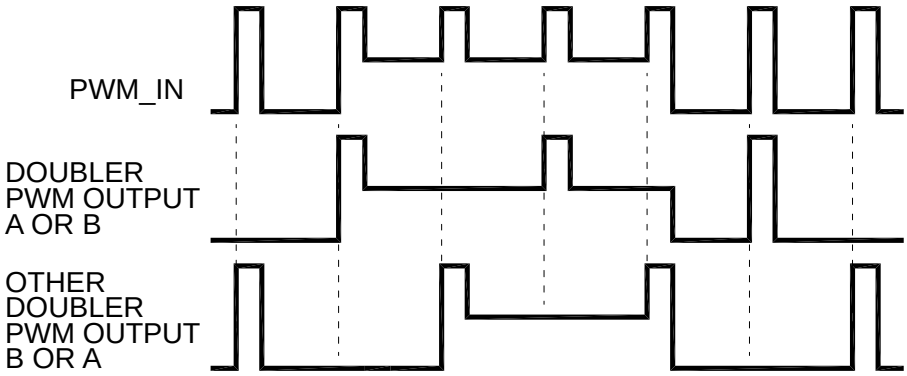


Figure 9. Response to PWM_IN High to Mid when MID_AB is High

When MID_AB is High, only the high PWM output responds to a PWM_IN high−to−mid transition. When MID_AB is high, the low PWM output does not respond to a PWM_IN high−to−mid transition.

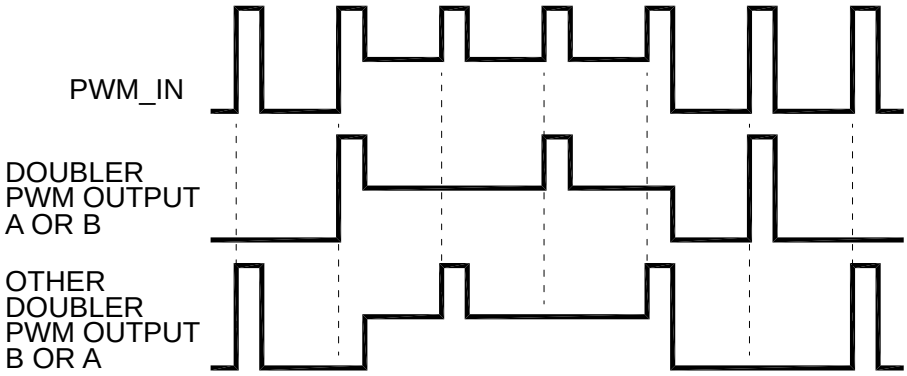


Figure 10. Response to PWM_IN High to Mid when MID_AB is Low

When MID_AB is Low, both PWMA and PWMB outputs respond to a PWM_IN high−to−mid transition. Only when MID_AB is low does the low PWM output respond to a PWM_IN high−to−mid transition by going to mid−level.

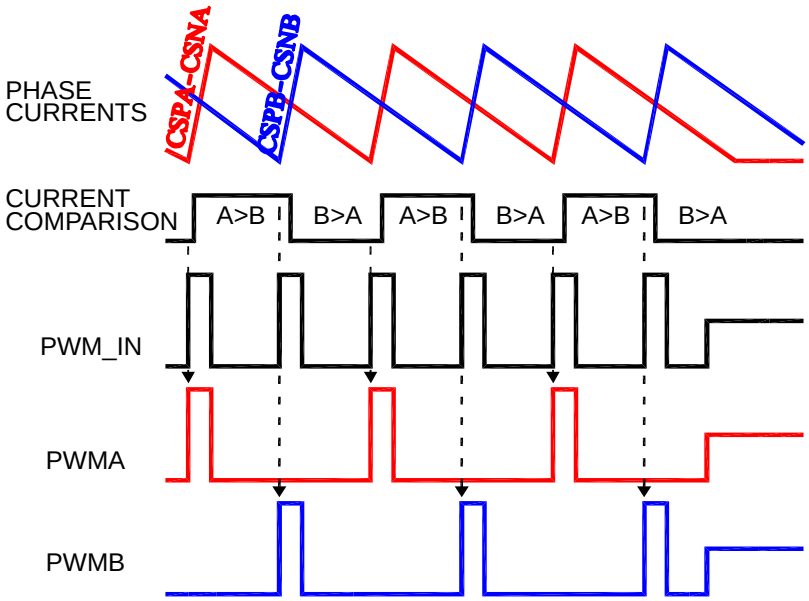


Figure 11. PWMA and PWMB Responses to PWM_IN Low to Mid Transition

In some cases, such as overcurrent, the controller must shut off all power stages by setting the PWM to the mid−level. Both PWM output always follow a PWM_IN Low−to−Mid level transition. Current in each phase is prevented from going negative by the ZCD or Diode Emulation function of the gate driver.

EN Input

The EN input should be connected to the controller Enable input so that the NCP81162 autocalibration ends and is ready to receive PWM pulses before the controller starts to send them. If the DRVON input is low when EN goes high, NCP81162 autocalibration is initiated, and the NCP81162 will stop pulling down the RDY output when autocalibration is finished. If the DRVON input is high when EN goes high, the PWMA and PWMB outputs respond to PWM_IN as soon as autocalibration is finished.

After both EN and DRVON have been high simultaneously, both EN and DRVON must simultaneously be low in order to completely power down the NCP81162.

DRVON Input

DRVON low keeps PWMA and PWMB in the mid−state if EN is high. After both EN and DRVON have been high simultaneously, both EN and DRVON must simultaneously be low in order to completely power down the NCP81162.

DBL_EN input

Connecting the DBL_EN input to VCC enables the doubling function. Connecting DBL_EN to ground will cause PWMA to follow every PWM_IN transition.

DBL_EN connected to ground causes PWMB to be held at mid−state.

PWM_BP Input

When the PWM_BP input is high, both PWMA and PWMB to follow every PWM_IN input transition. When PWM_BP is low, the PWM_IN signal appears only at the PWM output of the low current phase.

MID_HL Input

When the MID_HL input is connected to VCC, the mid−level voltage of both PWMA and PWMB is compatible with gate drivers having input thresholds optimized for 5 V, 3−level PWM signals. When the MID_HL input is connected to ground, the mid−level voltage of both PWMA and PWMB is compatible with gate drivers having input thresholds optimized for 3.3 V, 3−level PWM signals.

MID_AB Input

When the MID_AB input is connected to VCC, only the PWM output that is high will go to mid−level when PWM_IN transitions from high to mid−level. When the MID_AB input is connected to ground, both PWM outputs will go to mid−level when PWM_IN transitions from high to mid−level.

Input Under−Voltage Protection

The doubler is protected against under−voltage on the VCCA pin. The VCCA and VCCD pins should be tied together on the Printed Circuit Board.

Dual−Input Differential Current Comparator

The NCP81162 has a low offset differential comparator to compare the instantaneous phase currents for the purpose of balancing their currents. The incoming PWM pulse is routed to the phase having lower current at the instant of PWM_IN low to high transition.

When using inductor current sensing, the output of a correctly designed RC network will reproduce both the AC and DC components of the phase current, which is applied to the doubler CSP and CSN pins corresponding to the doubler PWM output controlling that phase. Select the CSN capacitor to maintain the value of RCSN in the range of 3k to10k. Select the C based on the equation CCSN = L/(DCR*RCSN).

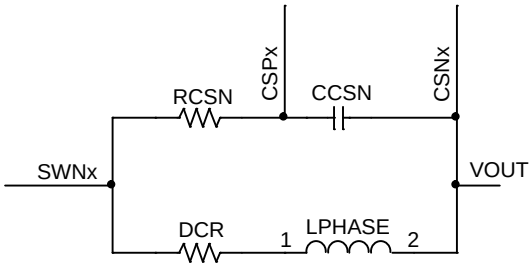


Figure 12.

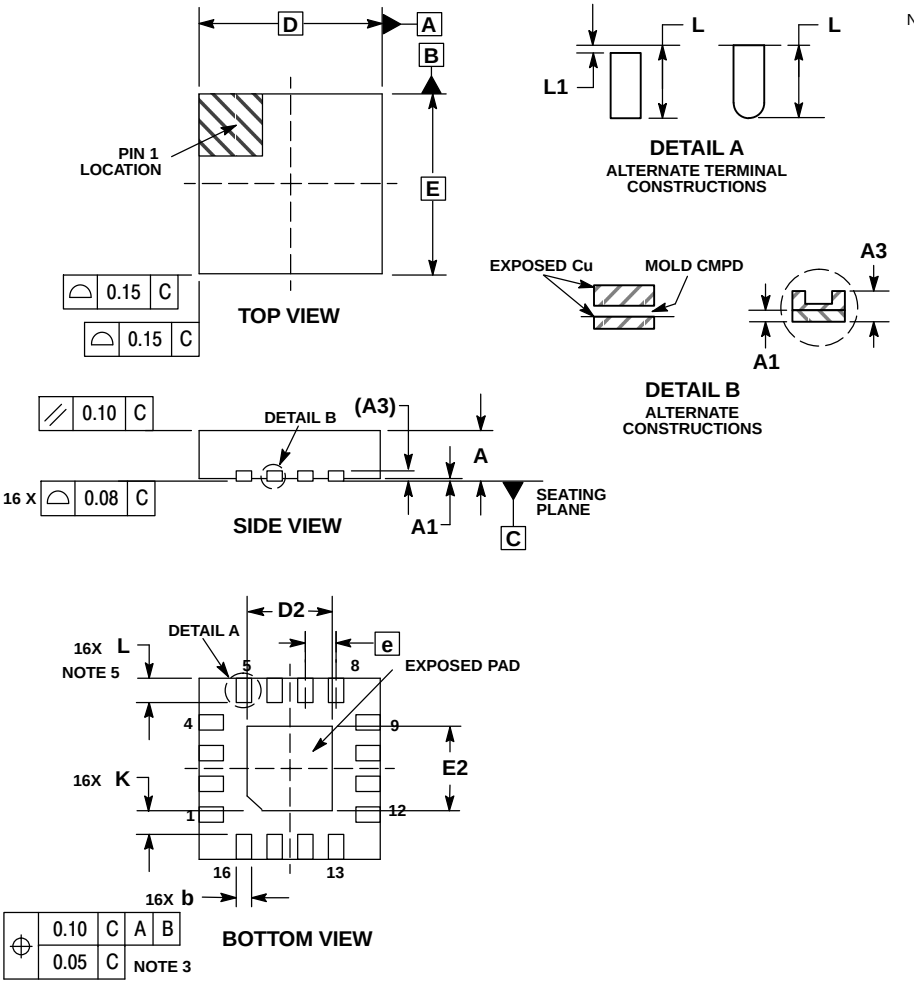
Layout Notes

The NCP81162 has differential current monitoring. This improves signal integrity and reduces noise issues related to layout for easy design use. To insure proper function there are some general rules to follow. Always place the inductor current sense RC filters as close to the doubler CSN and CSP pins as possible. Place the VCC decoupling caps as close as possible to the doubler VCC pins. Avoid routing the PWMA and PWMB signals next to the SWNA and SWNB signals.

It is important that the layout of the A and B power channels match well to help maximize the steady state current sharing accuracy. The doubling function will swap the phase angles when necessary to improve current balance.

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485AE−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. OUTLINE MEETS JEDEC DIMENSIONS PER MO−220, VARIATION VEED−6.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D		3.00 BSC	
D2	1.25	1.40	1.55
E		3.00 BSC	
E2	1.25	1.40	1.55
e		0.50 BSC	
K	0.20	−−−	−−−
L	0.30	0.40	0.50
L1	0.00	−−−	0.15

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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