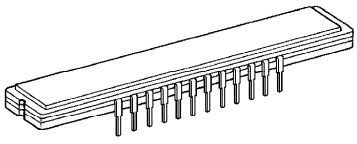
TOSHIBA CCD IMAGE SENSOR CCD (Charge Coupled Device)

TCD2555D

The TCD2555D is a high sensitive and low dark current 5348 elements × 3 line CCD color image sensor which includes CCD drive circuit, clamp circuit and sample and hold circuit.
The sensor is designed for scanner. The device contains a row of 5348 elements × 3 line photodiodes which provide a 24 lines / mm (600DPI) across a A4 size paper. The device is operated by 5V pulse, and 12V power supply.



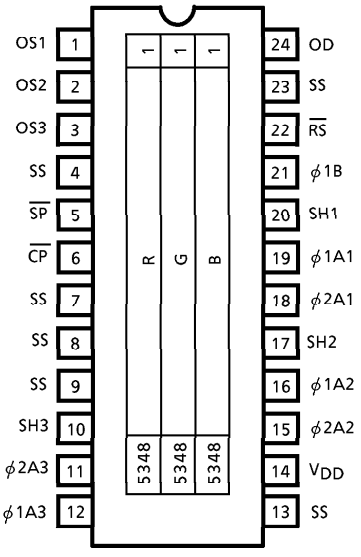
WDIP24-G-400-2.54A (B)

Weight : 5.0 g (Typ.)

FEATURES

- Number of Image Sensing Elements : 5348 elements × 3 line
- Image Sensing Element Size : 8μm by 8μm on 8μm centers
- Photo Sensing Region : High sensitive and low dark current PN photodiode
- Distanced Between Photodiode Array : 32μm (4 Lines)
- Clock : 2 phase (5V)
- Power Supply : 12V Power supply voltage
- Internal Circuit : Sample and Hold circuit, Clamp circuit
- Package : 24 pin CERDIP package
- Color Filter : Red, Green, Blue

PIN CONNECTION



(TOP VIEW)

MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	V_{ϕ}	−0.3~8	V
Shift Pulse Voltage	V_{SH}		V
Reset Pulse Voltage	$V_{\overline{RS}}$		V
Clamp Pulse Voltage	$V_{\overline{CP}}$		V
Sample and Hold Voltage	$V_{\overline{SP}}$		V
Power Supply	V_{OD}	−0.3~15	V
Digital Power Supply	V_{DD}		V
Operating Temperature	T_{opr}	0~60	°C
Storage Temperature	T_{stg}	−25~85	°C

(Note 1) All voltage are with respect to SS terminals (Ground).

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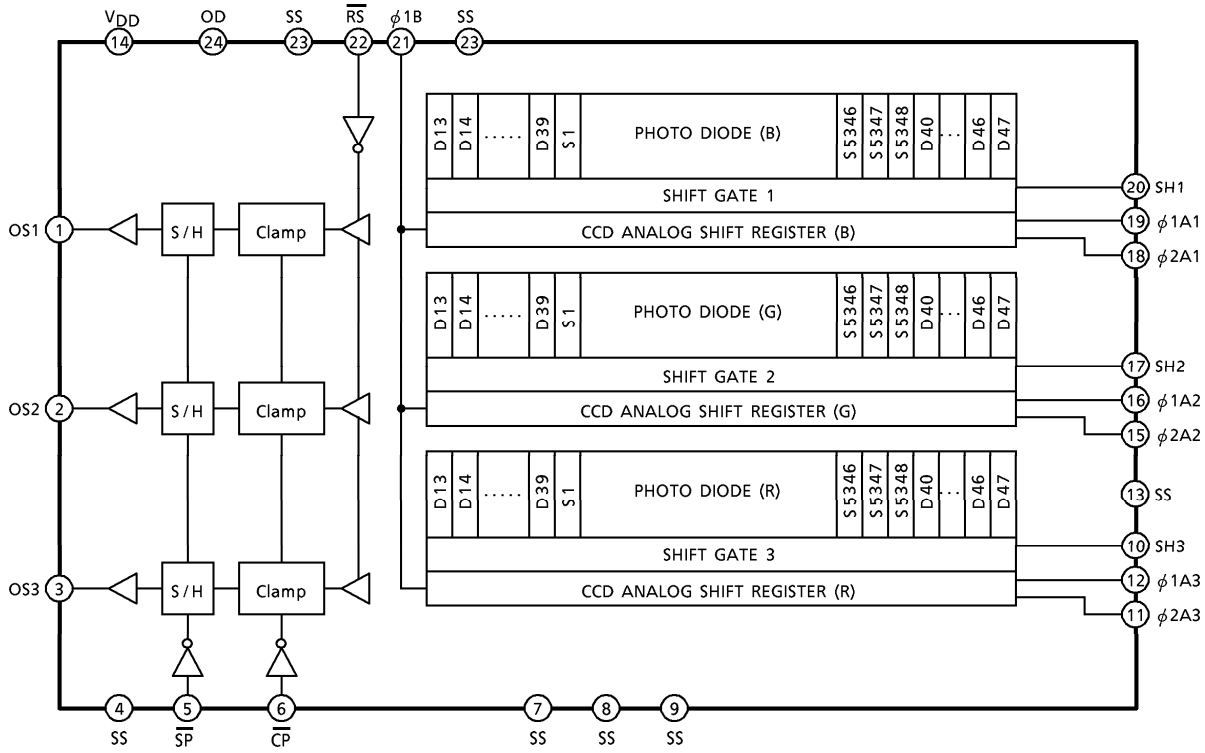
CIRCUIT DIAGRAM



PIN NAMES

PIN No.	SYMBOL	NAME	PIN No.	SYMBOL	NAME
1	OS1	Signal Output 1 (Blue)	13	SS	Ground
2	OS2	Signal Output 2 (Green)	14	V_{DD}	Power (Digital)
3	OS3	Signal Output 3 (Red)	15	ϕ2A2	Clock 2 (Phase 2)
4	SS	Ground	16	ϕ1A2	Clock 2 (Phase 1)
5	$\overline{SP}$	Sample and Hold Gate	17	SH2	Shift Gate 2
6	$\overline{CP}$	Clamp Gate	18	ϕ2A1	Clock 1 (Phase 2)
7	SS	Ground	19	ϕ1A1	Clock 1 (Phase 1)
8	SS	Ground	20	SH1	Shift Gate 1
9	SS	Ground	21	ϕ1B	Final Stage Clock (Phase 1)
10	SH3	Shift Gate 3	22	$\overline{RS}$	Reset Gate
11	ϕ2A3	Clock 3 (Phase 2)	23	SS	Ground
12	ϕ1A3	Clock 3 (Phase 1)	24	OD	Power (Analog)

OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, $V_{OD} = V_{DD} = 12V$, $V\phi = V_{SH} = V_{RS} = 5V$ (PULSE), $f\phi = 1MHz$, $f_{RS} = 1MHz$, $t_{INT} = 10ms$, LIGHT SOURCE = A LIGHT SOURCE + CM500S FILTER (t = 1mm), LOAD RESISTANCE = 100kΩ)

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Responsivity	Red	$R_{(R)}$	5.6	8.1	10.5	V / lx·s	(Note 2)
	Green	$R_{(G)}$	6.9	9.9	12.9		
	Blue	$R_{(B)}$	3.6	5.2	6.8		
Photo Response Non Uniformity		PRNU (1)	—	10	20	%	(Note 3)
		PRNU (3)	—	3	12	mV	(Note 4)
Image Lag		IL	—	10	—	%	(Note 5)
Saturation Output Voltage		V_{SAT}	2	2.5	—	V	(Note 6)
Saturation Exposure		SE	—		—		(Note 7)
Dark Signal Voltage		V_{DRK}	—	1	2	mV	(Note 8)
Dark Signal Non Uniformity		DSNU	—	2	3	mV	(Note 8)
DC Power Dissipation		P_D	—	200	300	mW	
Total Transfer Efficiency		TTE	92	—	—	%	
Output Impedance		Z_O	—	—	1	kΩ	
DC Compensation Output Voltage		V_{OS}	3	5	7	V	(Note 9)
Random Noise		$N_{D\sigma}$	—	0.8	—	mV	(Note 10)
Reset Noise		V_{RSN}	—	200	—	mV	(Note 9)

(Note 2) Responsivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

(Note 3) PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

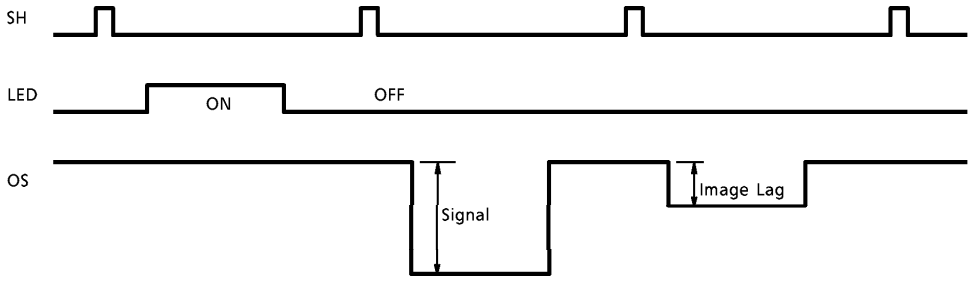
$$PRNU\ (1) = \frac{\Delta\chi}{\overline{\chi}} \times 100\ (\%)$$

When $\overline{\chi}$ is average of total signal output and $\Delta\chi$ is the maximum deviation from $\overline{\chi}$.
The amount of incident light is shown below.

Red = 1 / 2 · SE
Green = 1 / 2 · SE
Bule = 1 / 4 · SE

(Note 4) PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.).

(Note 5) Image Lag is defined as follows.

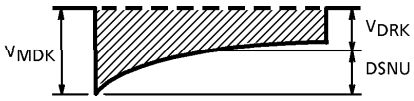


(Note 6) V_{SAT} is defined as minimum saturation output voltage of all effective pixels.

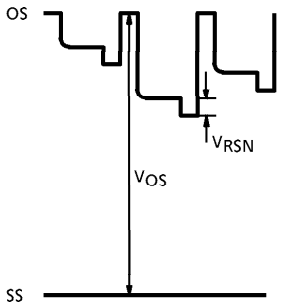
(Note 7) Definition of SE

$$SE = \frac{V_{SAT}}{R_G} \text{ (lx·s)}$$

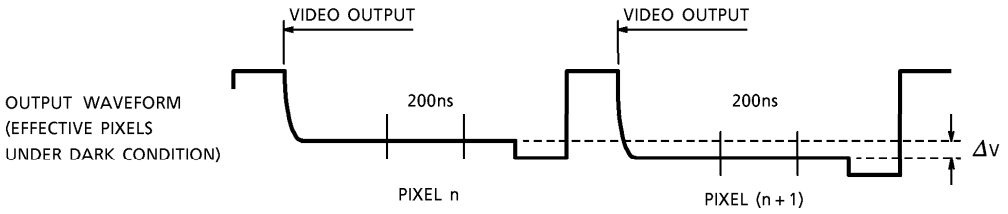
(Note 8) V_{DRK} is defined as average dark signal voltage of all effective pixels.
DSNU is defined as different voltage between V_{DRK} and V_{MDK}, when V_{MDK} is maximum dark signal voltage.



(Note 9) DC signal output voltage is defined as follows.
Reset Noise Voltage is defined as follows.



(Note 10) Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure.



1) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.
2) Each of the output level at video output periods averaged over 200ns period to get Vn and V (n + 1).
3) V (n + 1) is subtracted from Vn to get ΔV.

$$\Delta V = Vn - V(n+1)$$

4) The standard deviation of ΔV is calculated after procedure 2) and 3) are repeated 30 times (30 readings).

$$\overline{\Delta V} = \frac{1}{30}\sum_{i=1}^{30} |\Delta Vi| \qquad \sigma = \sqrt{\frac{1}{30}\sum_{i=1}^{30} (|\Delta Vi| - \overline{\Delta V})^2}$$

5) Procedure 2), 3) and 4) are repeated 10 times to get sigma value.
6) 10 sigma values are averaged.

$$\overline{\sigma} = \frac{1}{10}\sum_{j=1}^{10} \sigma j$$

7) $\overline{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify random noise as follows.

$$\text{ND } \sigma = \frac{1}{\sqrt{2}}\overline{\sigma}$$

OPERATING CONDITION

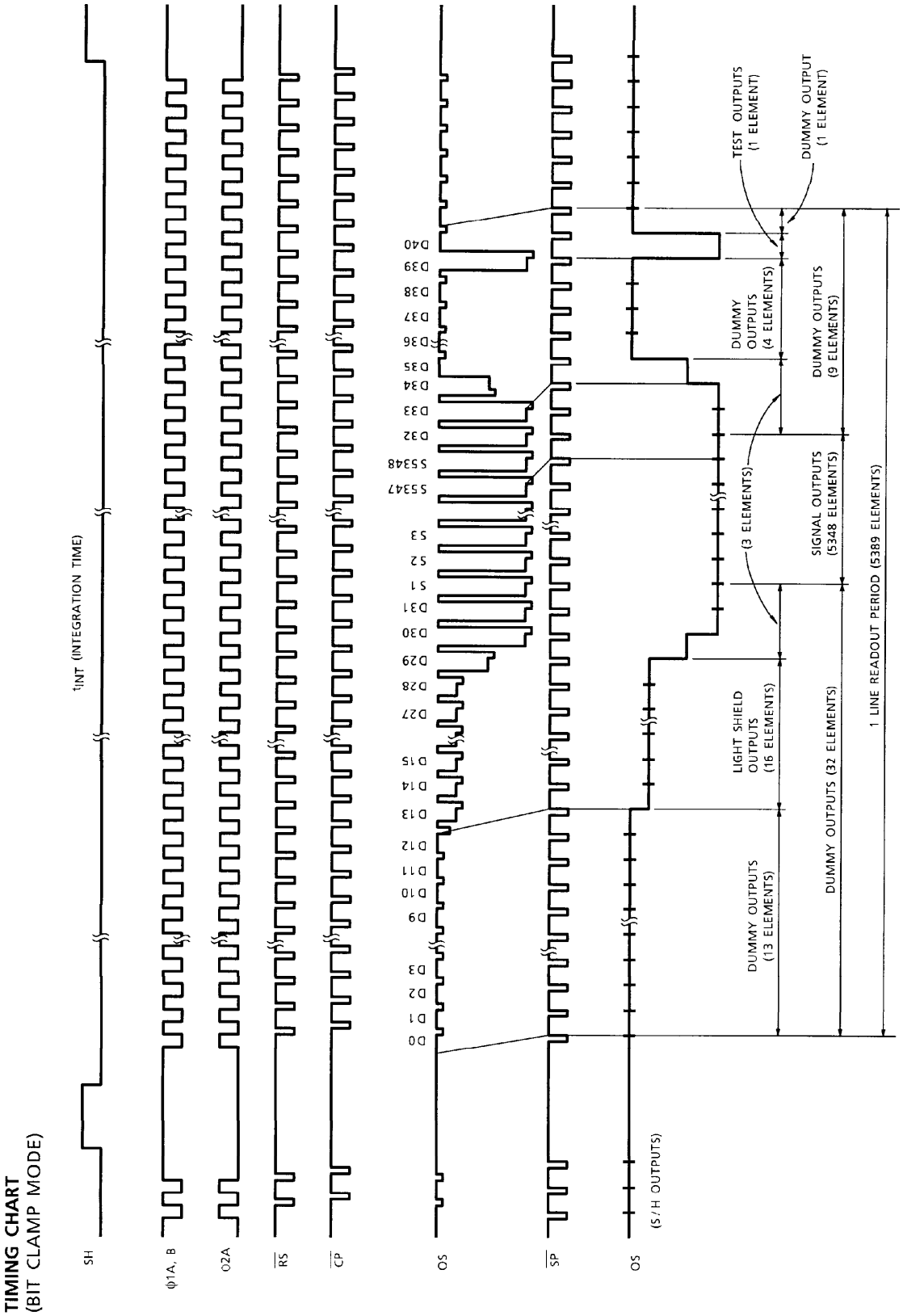
CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Pulse Voltage	"H" Level	$V\phi A$	4.7	5.0	5.5	V	
	"L" Level		0	0	0.3		
Shift Pulse Voltage	"H" Level	V_{SH}	4.5	5.0	5.5	V	(Note 11)
	"L" Level		0	0	0.3		
Reset Pulse Voltage	"H" Level	$V_{\overline{RS}}$	4.5	5.0	5.5	V	
	"L" Level		0	0	0.3		
Clamp Pulse Voltage	"H" Level	$V_{\overline{CP}}$	4.5	5.0	5.5	V	
	"L" Level		0	0	0.3		
Sample and Hold Pulse Voltage	"H" Level	$V_{\overline{SP}}$	4.5	5.0	5.5	V	(Note 12)
	"L" Level		0	0.	0.3		
Ditital Power Supply		V_{OD}	11.4	12.0	13.0	V	
Power Supply		V_{DD}	11.4	12.0	13.0	V	

(Note 11) $V\phi A$"H" means the high level voltage of $V\phi A$ when SH pulse is high level.
(Note 12) Supply "L" Level to $\overline{SP}$ terminal when sample and hold circuitry is not used.

CLOCK CHARACTERISTICS (Ta = 25°C)

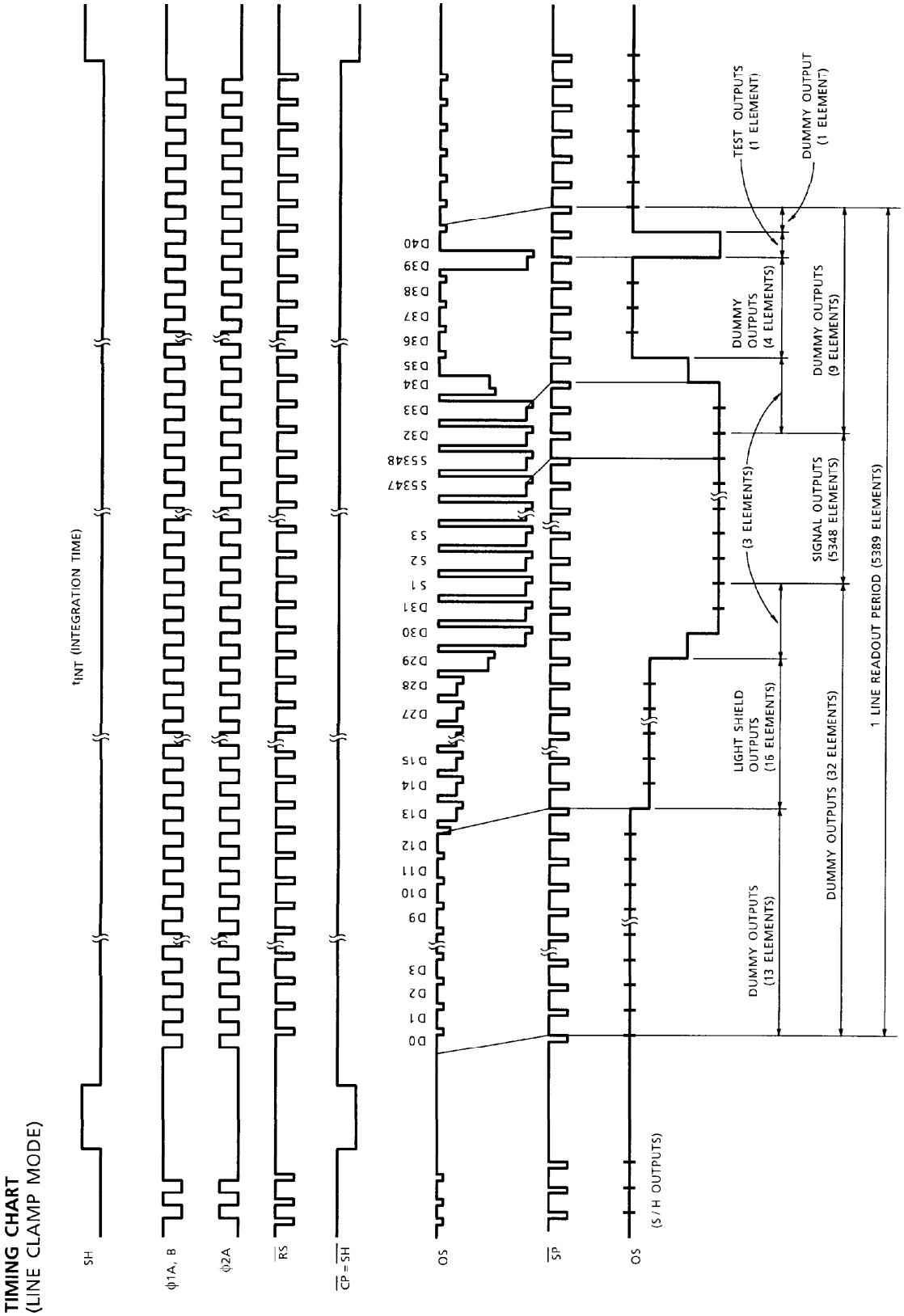
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	$f\phi A$	0.3	1	5	MHz
Reset Pulse Frequency	$f_{\overline{RS}}$	0.3	1	5	MHz
Sample and Hold Pulse Frequency	$f_{\overline{SP}}$	0.3	1	5	MHz
Clock Capacitance	$C_{\phi A}$	—	400	550	pF
Final Stage Clock Capacitance	$C_{\phi B}$	—	15	30	pF
Shift Gate Capacitance	C_{SH}	—	20	30	pF
Reset Gate Capacitance	$C_{\overline{RS}}$	—	20	30	pF
Clamp Gate Capacitance	$C_{\overline{CP}}$	—	20	30	pF
Sample and Hold Gate Capacitance	$C_{\overline{SP}}$	—	20	30	pF

TIMING CHART
(BIT CLAMP MODE)



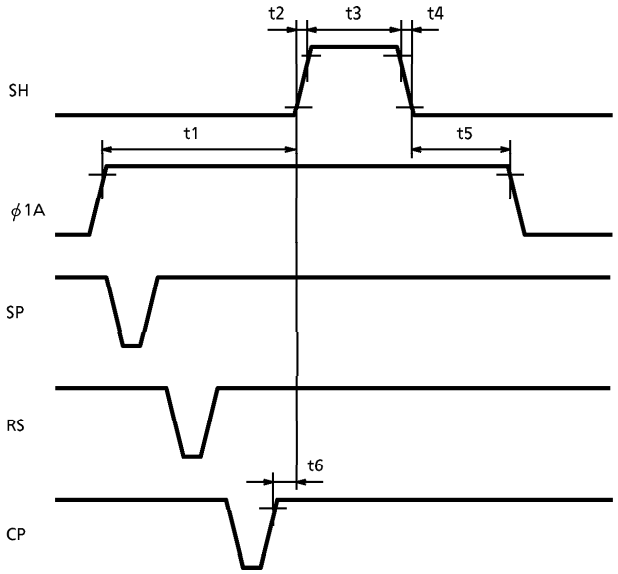
TCD2555D–7

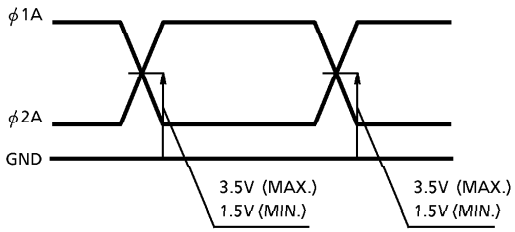
TIMING CHART
(LINE CLAMP MODE)

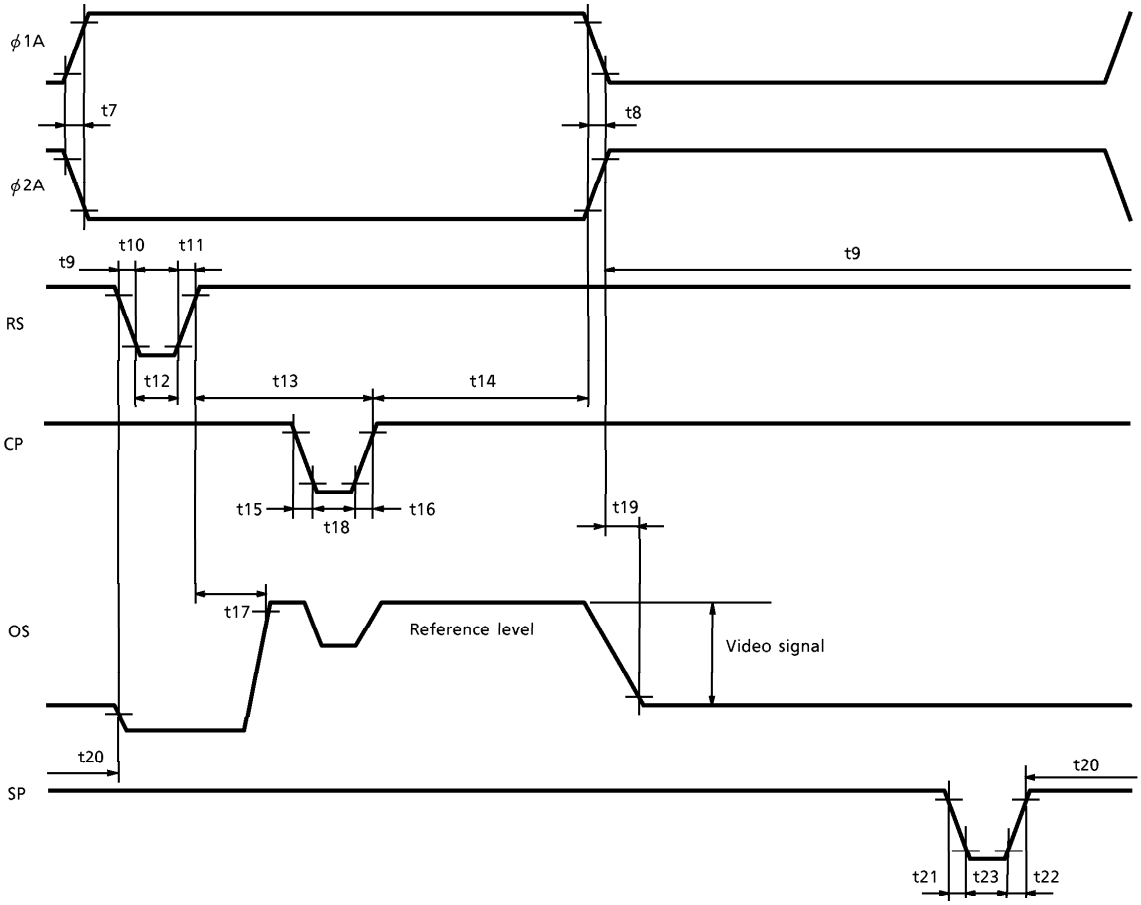


TCD2555D—8

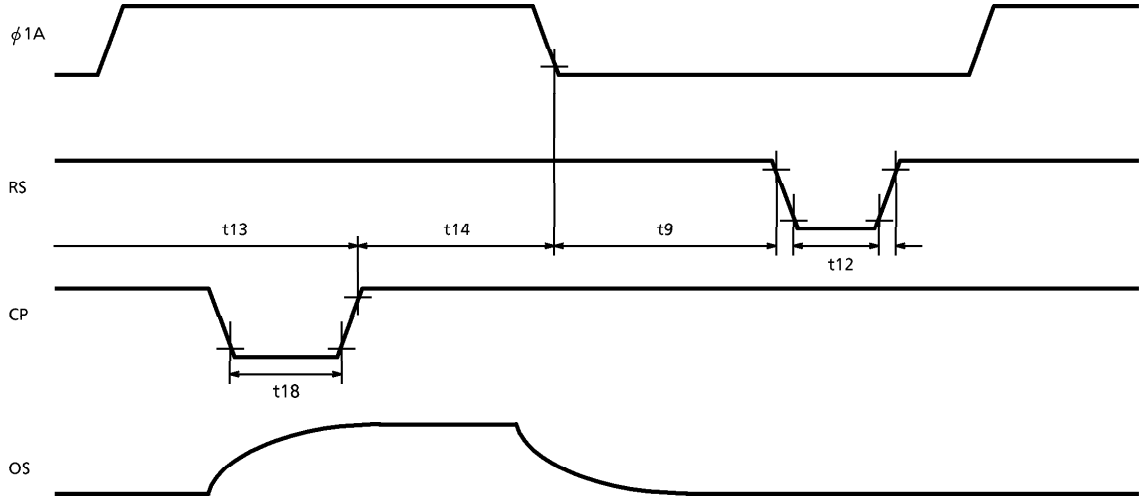
TIMING REQUIREMENTS







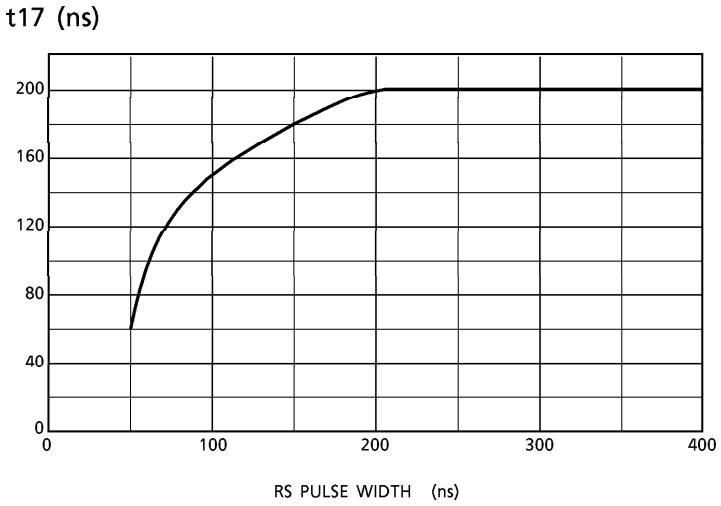
TIMING REQUIREMENTS



CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 13)	MAX.	UNIT
Pulse Timing of SH and φ1A	t1	120	1000	—	ns
	t5	800	1000	—	
SH Pulse Rise Time, Fall Time	t2, t4	0	50	—	ns
SH Pulse Width	t3	3000	5000	—	ns
Pulse Timing of SH and CP	t6	0	500	—	ns
φ1A, φ2A Pulse Rise Time, Fall Time	t7, t8	0	50	—	ns
Pulse Timing of φ1A and RS	t9	50	—	—	ns
RS Pulse Rise Time, Fall Time	t10, t11	0	20	—	ns
RS Pulse Width	t12	40	100	—	ns
CP Pulse Rise Time, Fall Time	t15, t16	0	20	—	ns
Pulse Timing of RS and CP	t13	80	200	—	ns
Pulse Timing of φ1A, φ2A and CP	t14	10	50	—	ns
Pulse Timing of RS and RS-noise	t17	(Note 15)	—	—	ns
CP Pulse Width	t18	40	100	—	ns
SP Pulse Rise Time, Fall Time	t21, t22	—	20	—	ns
SP Pulse Width	t23	40	100	—	ns
Pulse Timing of RS and SP	t20	0	20	—	ns
Video Data Delay Time (Note 14)	t19	—	80	—	ns

(Note 13) TYP. is the case of f_{RS} = 1.0MHz.
(Note 14) Load Resistance is 100kΩ.

(Note 15)

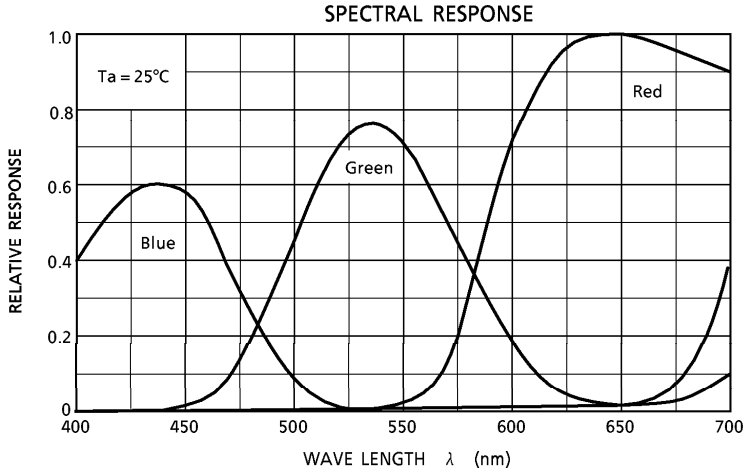


APPLICATION NOTE

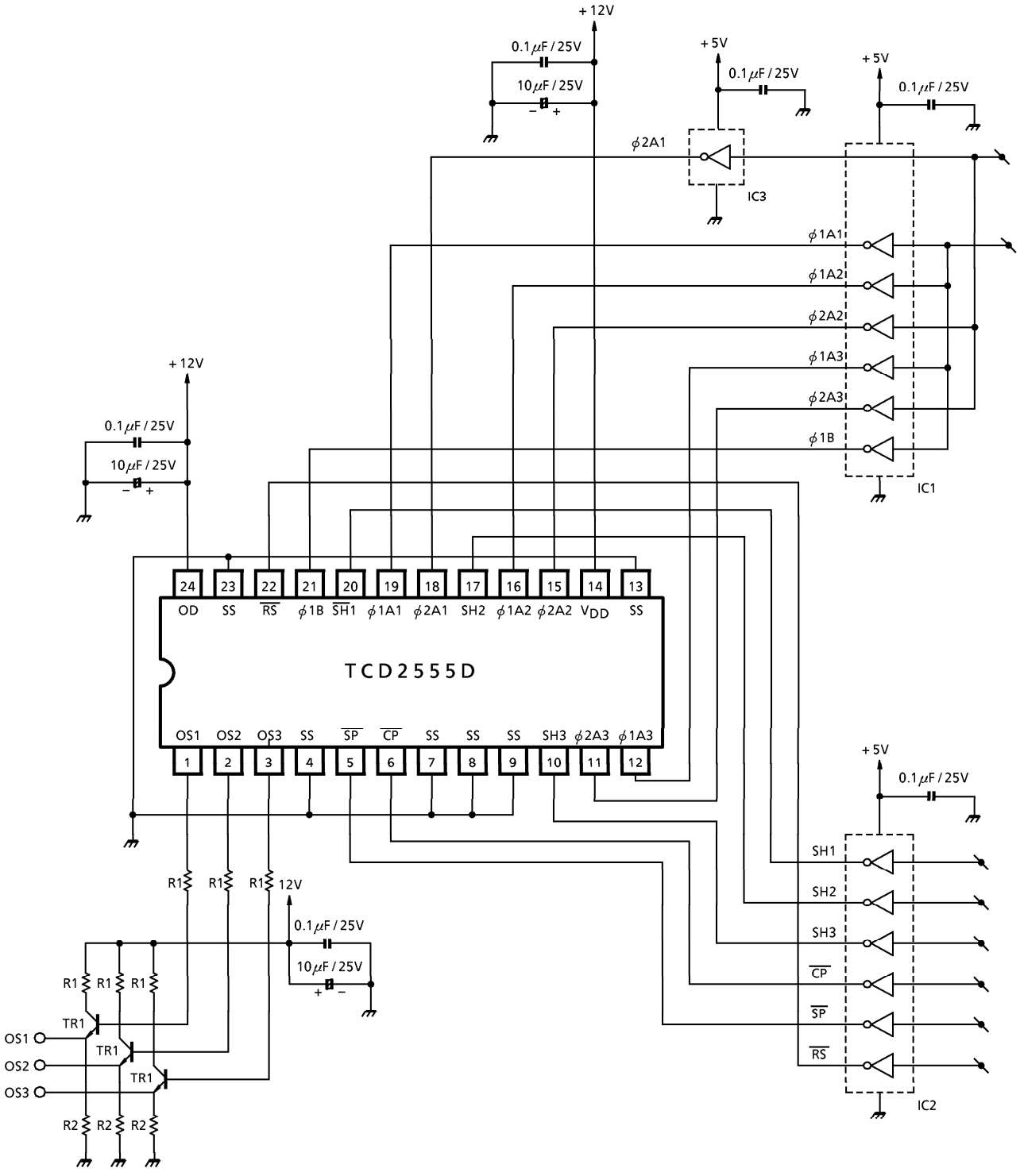
Mode Select

Sample and Hold	ON SP Pulse	OFF SP = Low
Clamp Mode	Bit Clamp CP Pulse	Line Clamp CP = $\overline{SH}$

TYPICAL SPECTRAL RESPONSE



TYPICAL DRIVE CIRCUIT



IC1, 2, 3 : TC74HC04AP
TR1 : 2SC1815-Y
R1 : 150Ω
R2 : 1500Ω

CAUTION

1. Window Glass

   The dust and stain on the glass window of the package degrade optical performance of CCD sensor.
   Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N_2.
   Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

   Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

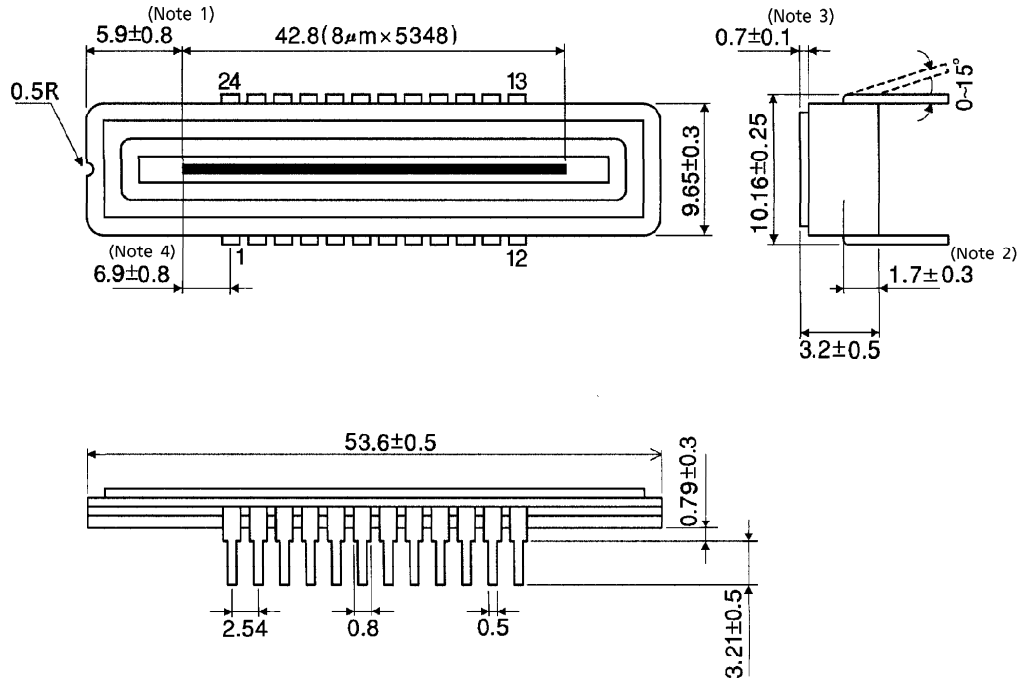
   CCD sensor is sensitive to infrared light.
   Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Lead Frame Forming

   Since this package is not strong against mechanical stress, you should not reform the lead frame.
   We recommend to use a IC-inserter when you assemble to PCB.

OUTLINE DRAWING

WDIP24-G-400-2.54A (B) Unit : mm



(Note 1) No.1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
(Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
(Note 3) GLASS THICKNESS (n = 1.5)
(Note 4) No.1 SENSOR ELEMENT (S1) TO EDGE OF No.1 PIN.

Weight : 5.0 g (Typ.)