

SN74ALS994, SN74ALS995 10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

D2856, OCTOBER 1984—REVISED JANUARY 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic
'ALS994 . . . True Outputs
'ALS995 . . . Inverting Outputs
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

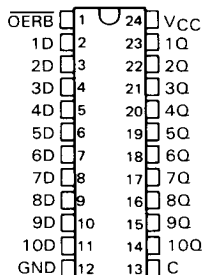
These 10-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus.

The ten latches of the 'ALS994 and 'ALS995 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS994 will follow the data (D) inputs. For the 'ALS995, the Q outputs will provide the inverse of what is applied to its data (D) inputs.

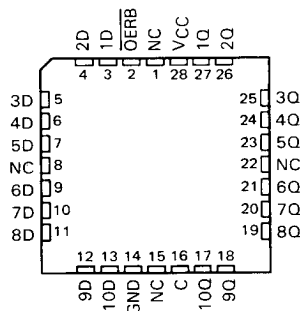
Read-back is provided through the read-back control input ($\overline{\text{OERB}}$). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a bus-conflict situation.

The SN74ALS994 and SN74ALS995 are characterized for operation from 0°C to 70°C.

SN74ALS994 . . . DW OR NT PACKAGE
(TOP VIEW)



SN74ALS994 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection.

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ALS and AS Circuits

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

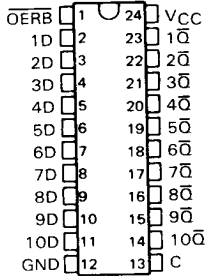
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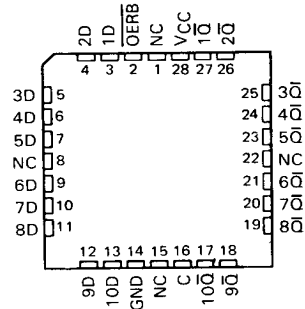
SN74ALS994, SN74ALS995 10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

SN74ALS995 . . . DW OR NT PACKAGE
(TOP VIEW)



NC—No internal connection

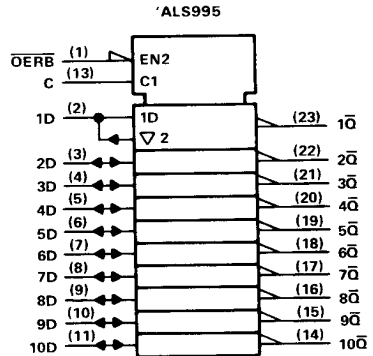
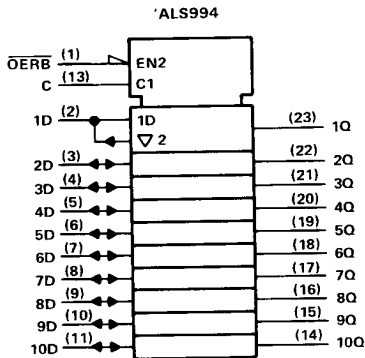
SN74ALS995 . . . FN PACKAGE
(TOP VIEW)



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ALS and AS Circuits

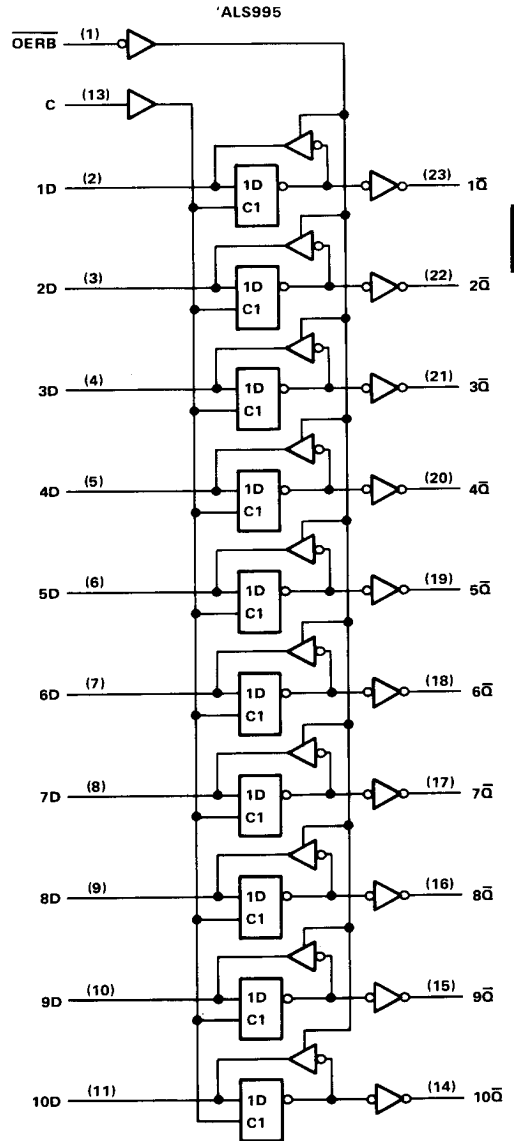
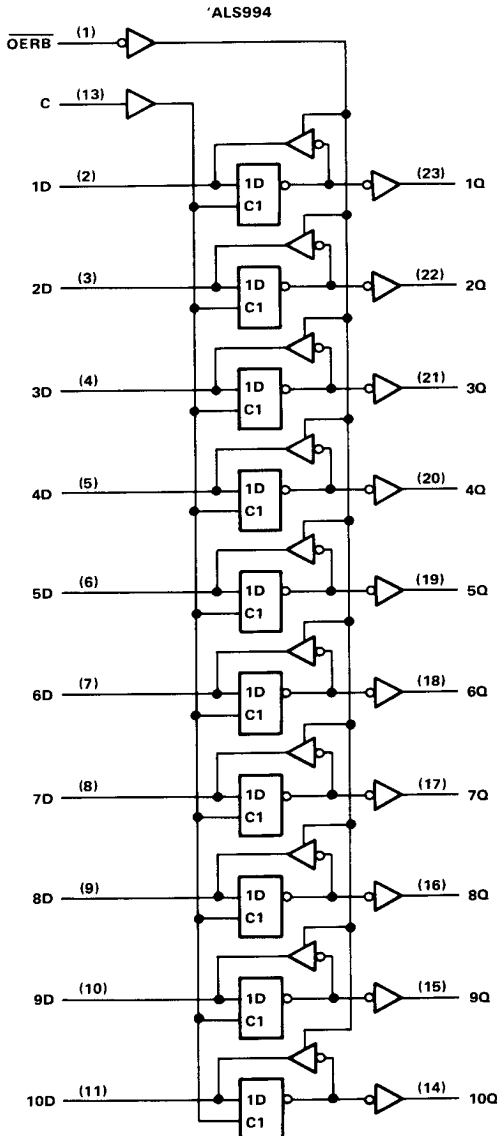
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW and NT packages.

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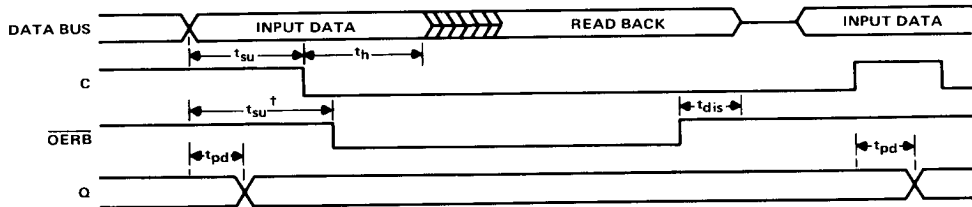
logic diagrams (positive logic)



Pin numbers shown are for DW and NT packages.

SN74ALS994, SN74ALS995 10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

timing diagram



† This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage ($\overline{OERB}$ and C)	7 V
Voltage applied to D inputs	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-2.6	mA
	D			-0.4	
I_{OL}	Low-level output current			24	mA
	D			8	
t_w	Pulse duration, enable C high	10			ns
t_{su}	Setup time	10			ns
	Data before C↓	10			
	Data before $\overline{OERB}↓$ †	10			
t_h	Hold time	5			ns
	Input data after C↓	5			
T_A	Operating free-air temperature	0		70	°C

† This setup time ensures the readback circuit will not create a conflict on the input data bus.

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10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA				-1.2	V
V _{OH}	All outputs	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} - 2			V
	Q or Q̄	V _{CC} = 4.5 V, I _{OH} = -2.6 mA		2.4	3.2		
V _{OL}	D	V _{CC} = 4.5 V, I _{OL} = 4 mA		0.25		0.4	V
		V _{CC} = 4.5 V, I _{OL} = 8 mA		0.35		0.5	
	Q or Q̄	V _{CC} = 4.5 V, I _{OL} = 12 mA		0.25		0.4	
		V _{CC} = 4.5 V, I _{OL} = 24 mA		0.35		0.5	
I _I	ÖERB, C	V _{CC} = 5.5 V, V _I = 7 V				0.1	mA
	D inputs	V _{CC} = 5.5 V, V _I = 5.5 V				0.1	
I _{IH}	ÖERB, C	V _{CC} = 5.5 V, V _I = 2.7 V				20	µA
	D inputs‡					20	
I _{IL}	ÖERB, C	V _{CC} = 5.5 V, V _I = 0.4 V				-0.1	mA
	D inputs‡					-0.1	
I _O §		V _{CC} = 5.5 V, V _O = 2.25 V		-30		-112	mA
I _{CC}	'ALS994	V _{CC} = 5.5 V, ÖERB high	Q outputs high		30	50	mA
			Q outputs low		52	82	
	'ALS995		Q̄ outputs high		30	50	
			Q̄ outputs low		55	85	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit output current, I_{OS} .

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10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

ALS994 switching characteristics (see Figure 1)

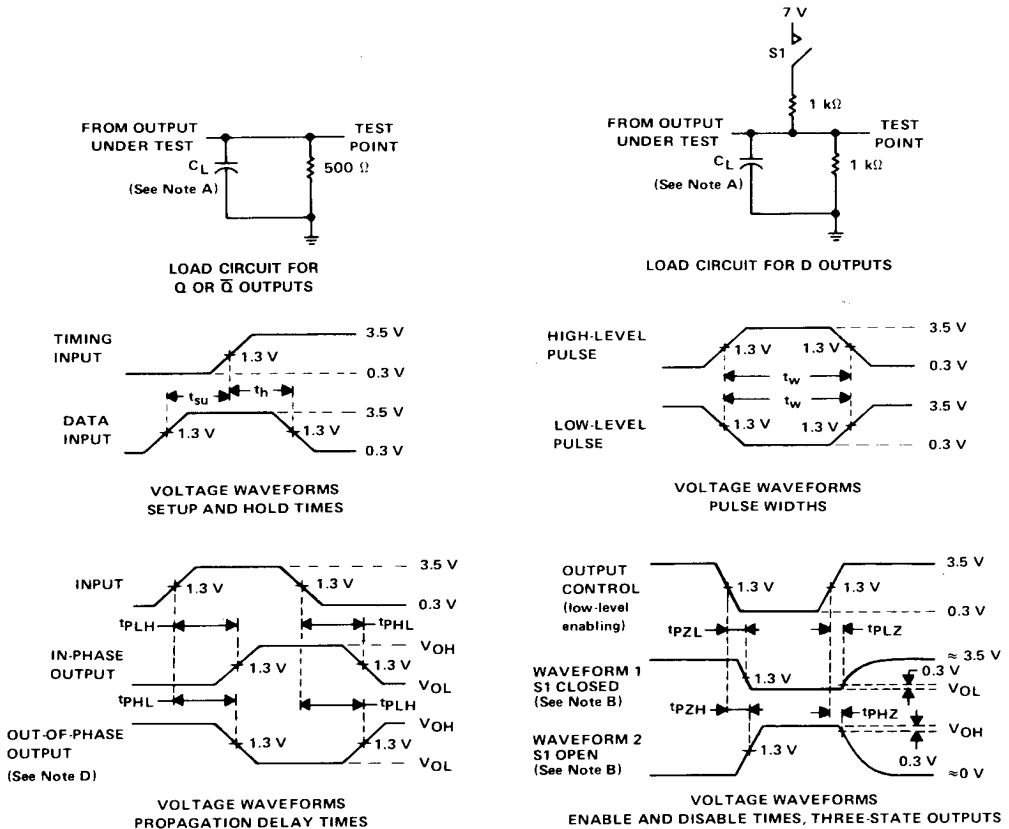
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25 °C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = 0 °C to 70 °C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	D	Q		7	10	3	14	ns
t _{PHL}				11	15	4	18	
t _{PLH}	C	Q		12	16	6	21	ns
t _{PHL}				16	21	8	27	
t _{en}	OERB	D		11	17	4	21	ns
t _{dis}				9	13	2	16	

ALS995 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25 °C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, T _A = 0 °C to 70 °C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t _{PLH}	D	$\overline{Q}$	12	16	6	20	ns	
t _{PHL}			9	12	4	15		
t _{PLH}	C	$\overline{Q}$	17	23	9	28	ns	
t _{PHL}			14	19	7	22		
t _{en}	$\overline{OERB}$	D	12	18	4	21	ns	
t _{dis}			8	12	2	15		

t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1