



STN1N20

N-channel 200 V, 1.2 Ω , 1 A, SOT-223
MESH OVERLAY™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STN1N20	200 V	< 1.5 Ω	1 A

- 100% avalanche tested

Application

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the latest high voltage MESH OVERLAY™ process. The new patented STrip layout coupled with the company's proprietary edge termination structure, makes it suitable in converters for lighting applications.

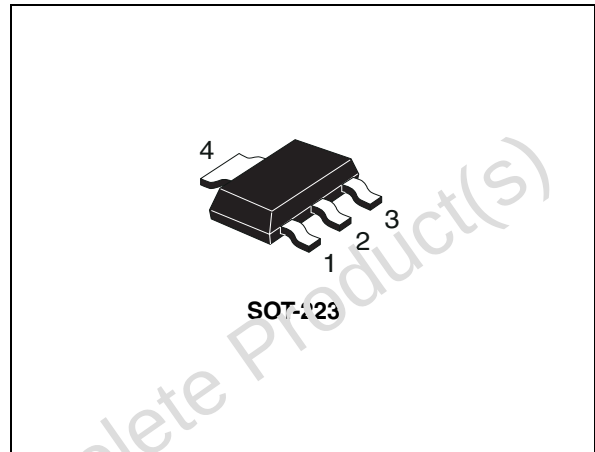
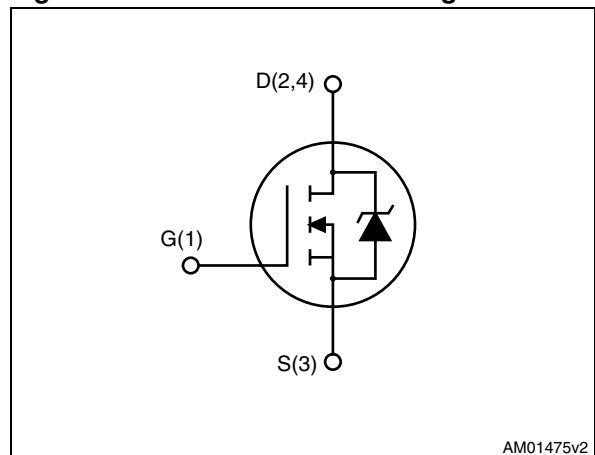


Figure 1. Internal schematic diagram



AM01475v2

Table 1. Device summary

Order code	Marking	Package	Packaging
STN1N20	N1N20	SOT-223	Tape and reel

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Obsolete Product(s) - Obsolete Product(s)



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	200	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	1	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	0.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	4	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	2.9	W
	Derating factor	0.023	W/ $^{\circ}\text{C}$
dv/dt	Peak diode recovery voltage slope	3	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}$	Thermal resistance junction-pcb max	43	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	60	$^{\circ}\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	260	$^{\circ}\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	1	A
E_{AS}	Single pulse avalanche energy ⁽¹⁾	10	mJ

1. Starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 250 \mu A$	200			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, T_C = 125^\circ C$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 0.5 A$		1.2	1.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $I_D = 0.5 A$	-	2.7		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 V, f = 1 MHz,$ $V_{GS} = 0$	-	206 40 15		pF pF pF
Q_g C_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 160 V, I_D = 4 A,$ $V_{GS} = 10 V$ (see Figure 14)	-	11 2.8 4	15.7	nC nC nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 160 V, I_D = 4 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (see Figure 13)	-	9	-	ns
t_r	Rise time			10		ns
$t_{d(off)}$	Turn-off delay time			25		ns
t_f	Fall time			6		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		1	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		4	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	124		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 30\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$	-	446		nC
I_{RRM}	Reverse recovery current	(see Figure 18)		7.2		A

1. Pulse width limited by safe operating area.

2. Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

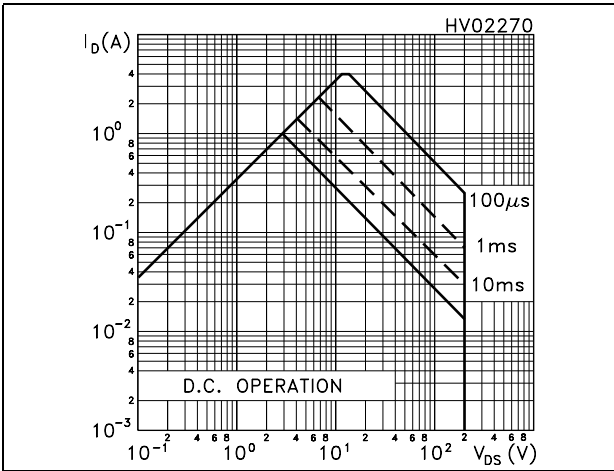


Figure 3. Thermal impedance

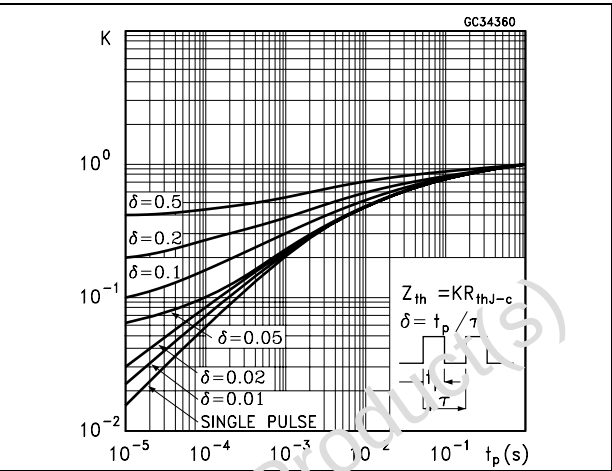


Figure 4. Output characteristics

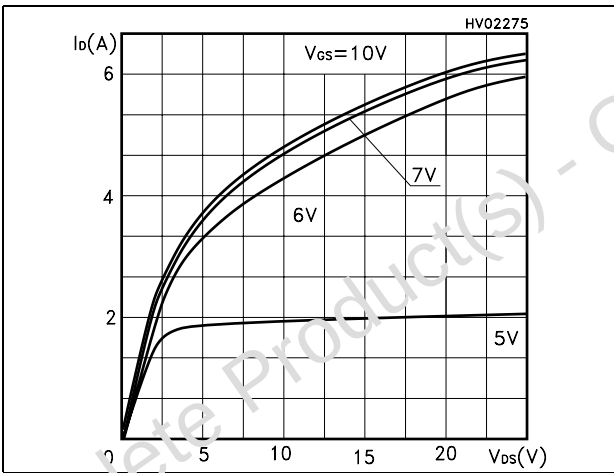


Figure 5. Transfer characteristics

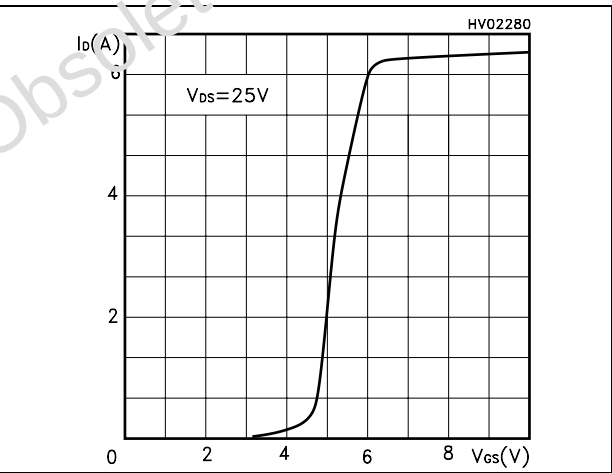


Figure 6. Transconductance

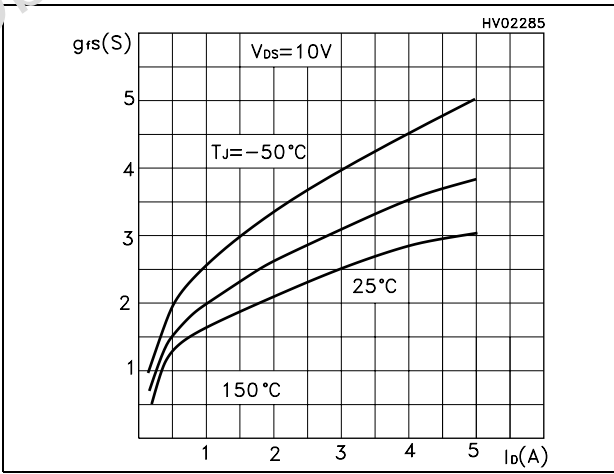


Figure 7. Static drain-source on resistance

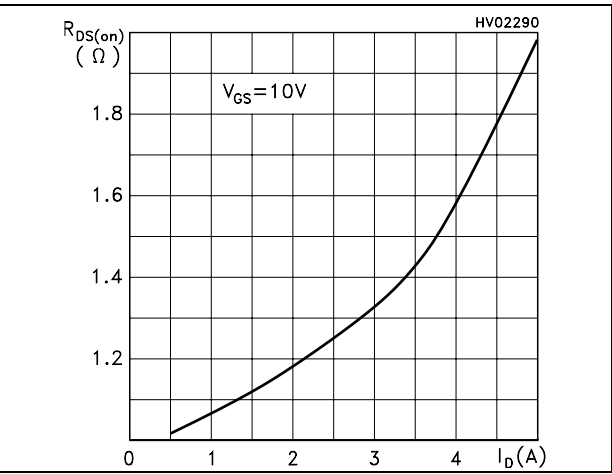


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

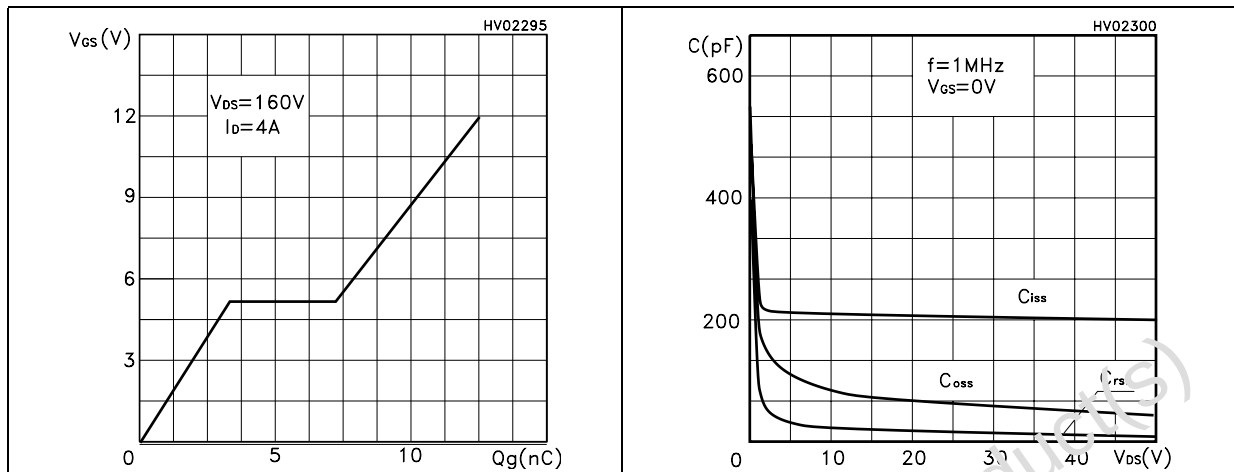


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

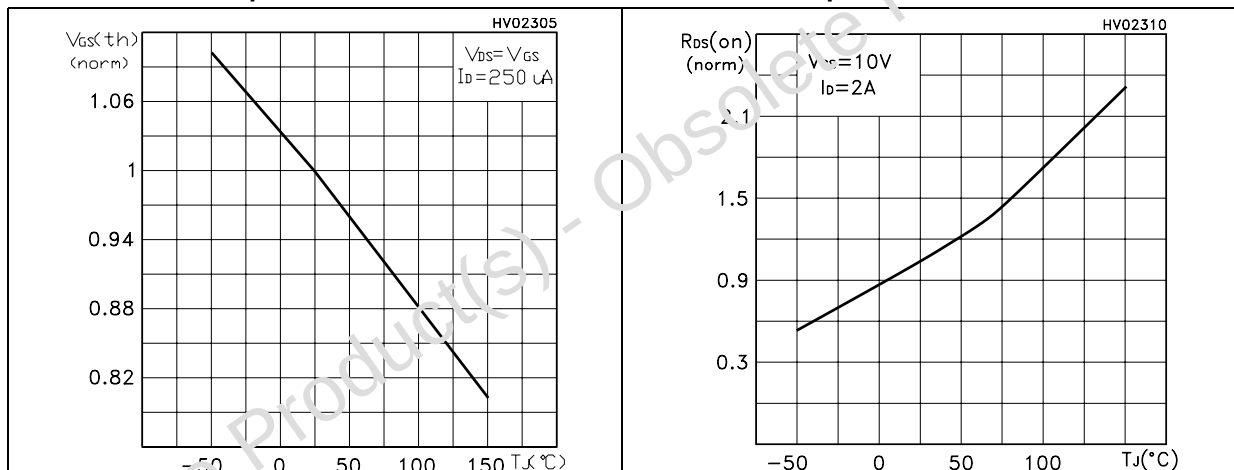
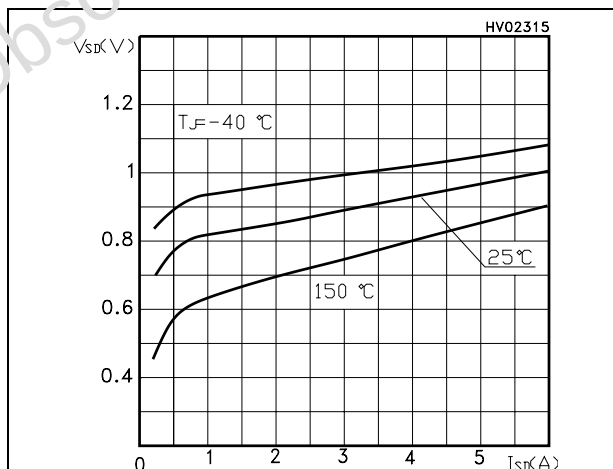


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

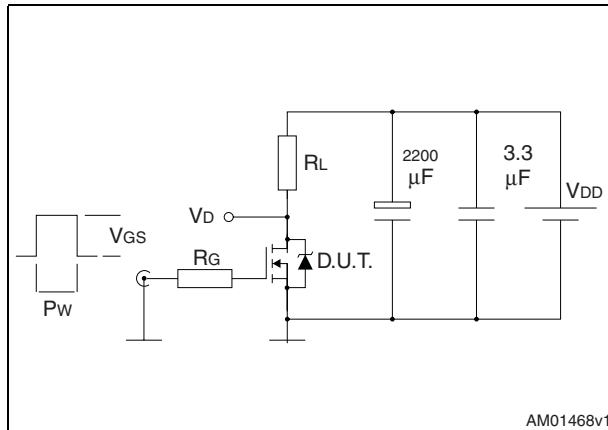


Figure 14. Gate charge test circuit

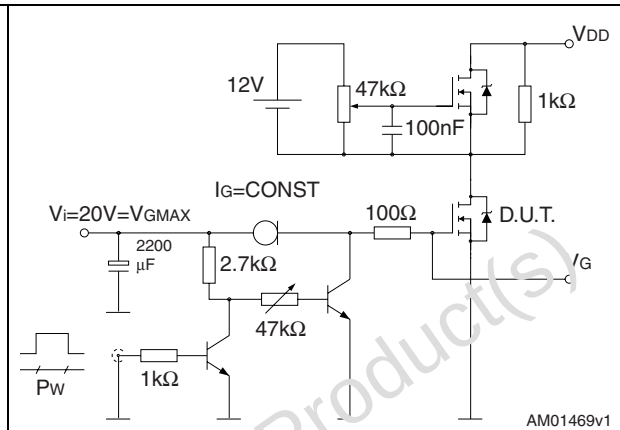


Figure 15. Test circuit for inductive load switching and diode recovery times

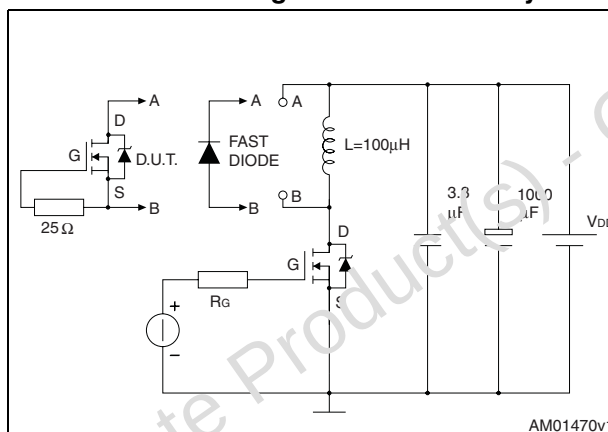


Figure 16. Uncamped inductive load test circuit

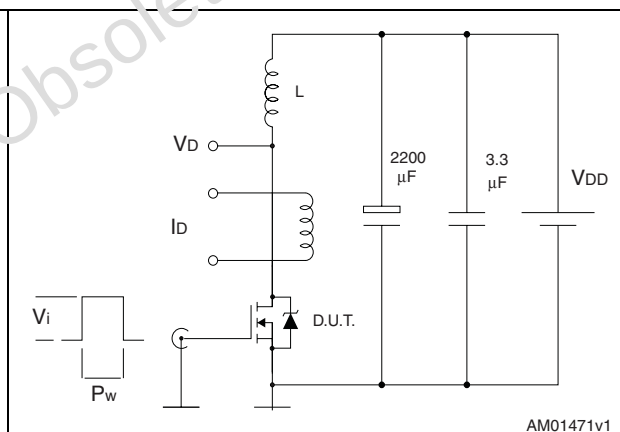


Figure 17. Unclamped inductive waveform

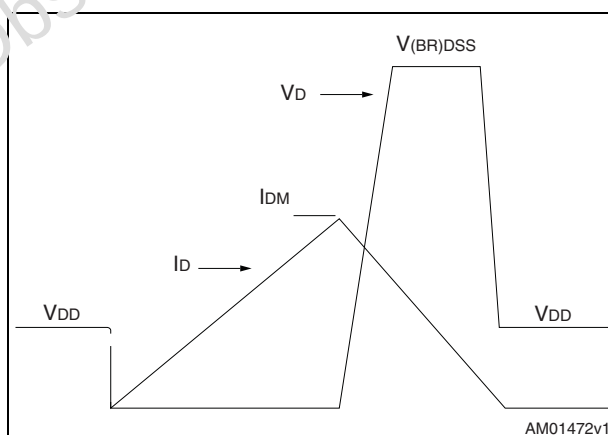
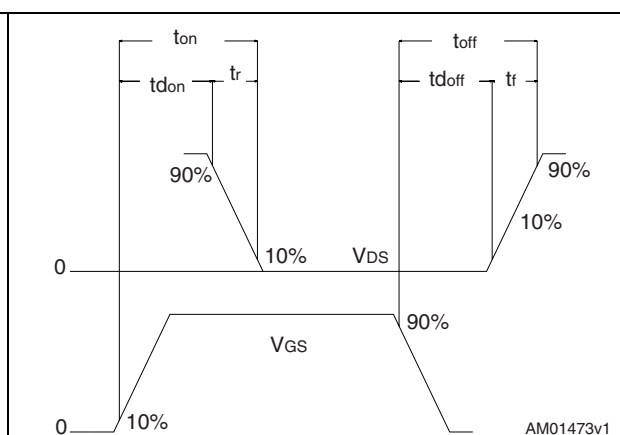


Figure 18. Switching time waveform



4 Package mechanical data

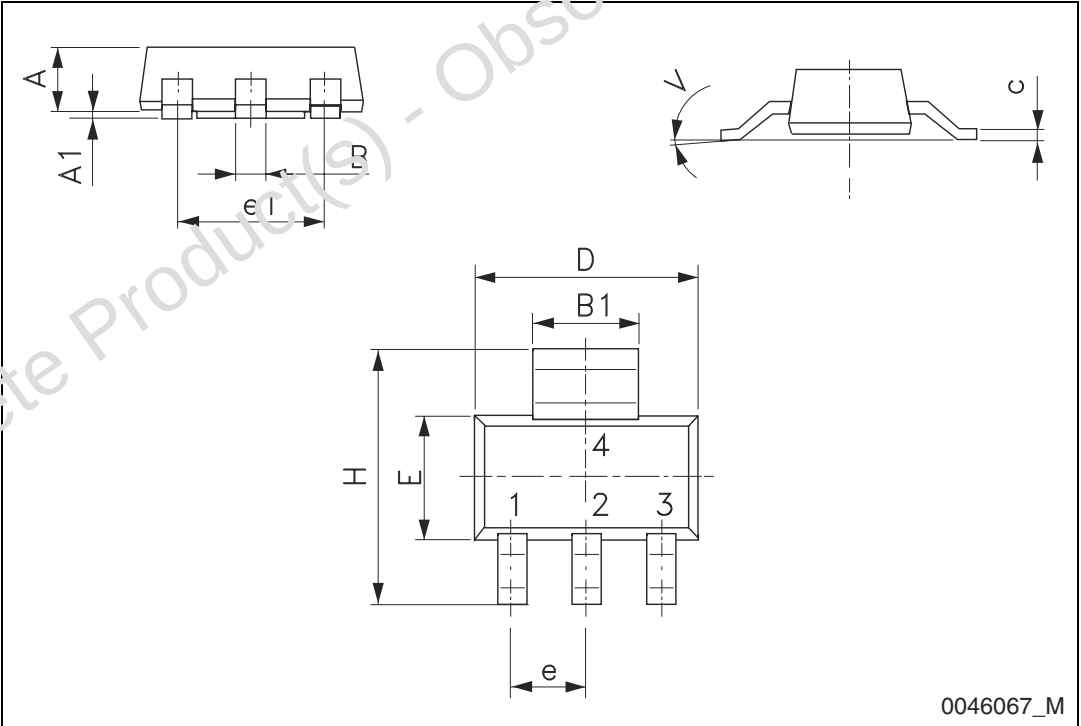
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Obsolete Product(s) - Obsolete Product(s)

Table 9. SOT-223 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.80
A1	0.02		0.1
B	0.60	0.70	0.85
B1	2.90	3.00	3.15
c	0.24	0.26	0.35
D	6.30	6.50	6.70
e		2.30	
e1		4.60	
E	3.30	3.50	3.70
H	6.70	7.00	7.30
V			10°

Figure 19. SOT-223 mechanical data drawing



0046067_M

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
21-Jun-2004	1	First release.
31-Mar-2009	2	Document status promoted from preliminary data to datasheet.
27-Jun-2011	3	Updated gate threshold voltage values on Table 5 and the package mechanical data Section 4 .

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