

SN54AHCT574, SN74AHCT574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS245J – OCTOBER 1995 – REVISED JANUARY 2000

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

description

The 'AHCT574 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

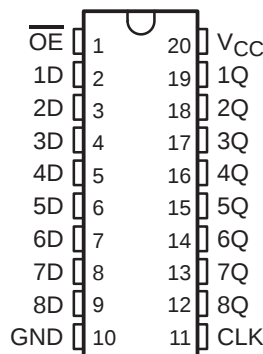
A buffered output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

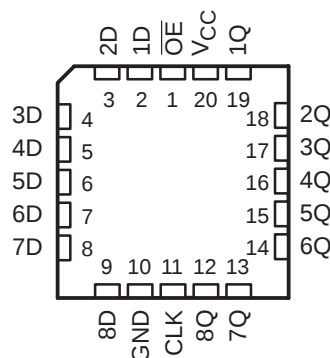
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHCT574 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHCT574 is characterized for operation from -40°C to 85°C .

SN54AHCT574 . . . J OR W PACKAGE
SN74AHCT574 . . . DB, DGV, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT574 . . . FK PACKAGE
(TOP VIEW)



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**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

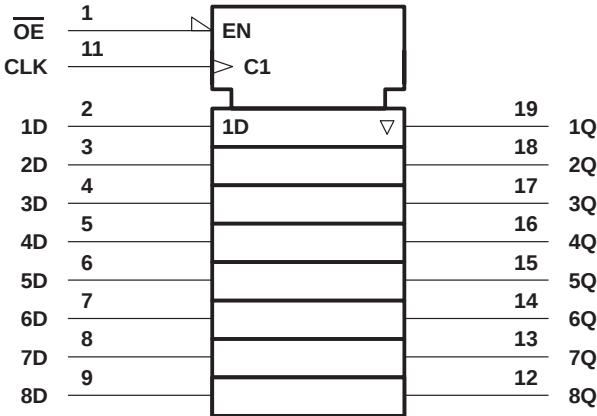
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FUNCTION TABLE
(each flip-flop)

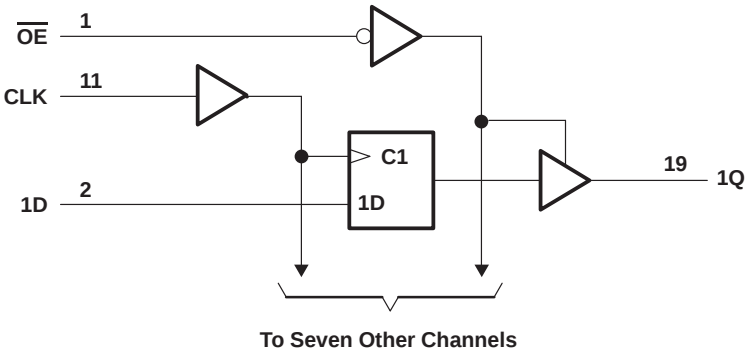
INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Output voltage range, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	−20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
N package	69°C/W
PW package	83°C/W
Storage temperature range, T_{sta}	−65°C to 150°C

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51.

		SN54AHCT574		SN74AHCT574		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		−8		−8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT574		SN74AHCT574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4	4.5		4.4		4.4		V
	I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
	I _{OL} = 8 mA				0.36		0.44		0.44	
I _I	V _I = V _{CC} or GND	0 V to 5.5 V			±0.1		±1*		±1	µA
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		±2.5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40	µA
ΔI _{CC} [†]	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C _i	V _I = V _{CC} or GND	5 V		3	10				10	pF
C _o	V _O = V _{CC} or GND	5 V		3						pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54AHCT574		SN74AHCT574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, CLK high or low	5		5.5		5.5		ns
t _{su}	Setup time, data before CLK↑	3		3.5		3.5		ns
t _h	Hold time, data after CLK↑	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHCT574		SN74AHCT574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	130**	180**		110**		110		MHz
			C _L = 50 pF	85	115		75		75		
t _{PLH}	CLK	Q	C _L = 15 pF		5.5**	8.6**	1**	10**	1	10	ns
t _{PHL}					5.5**	8.6**	1**	10**	1	10	
t _{PZH}	$\overline{\text{OE}}$	Q	C _L = 15 pF		5**	9**	1**	10.5**	1	10.5	ns
t _{PZL}					5**	9**	1**	10.5**	1	10.5	
t _{PHZ}	$\overline{\text{OE}}$	Q	C _L = 15 pF		5.5**	9**	1**	10.5**	1	10.5	ns
t _{PLZ}					5.5**	9**	1**	10.5**	1	10.5	
t _{PLH}	CLK	Q	C _L = 50 pF		7	10.6	1	12	1	12	ns
t _{PHL}					7	10.6	1	12	1	12	
t _{PZH}	$\overline{\text{OE}}$	Q	C _L = 50 pF		6	11	1	12.5	1	12.5	ns
t _{PZL}					6	11	1	12.5	1	12.5	
t _{PHZ}	$\overline{\text{OE}}$	Q	C _L = 50 pF		7	10.1	1	11.5	1	11.5	ns
t _{PLZ}					7	10.1	1	11.5	1	11.5	
t _{sk(o)}			C _L = 50 pF			1***				1	ns

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

*** On products compliant to MIL-PRF-38535, this parameter does not apply.



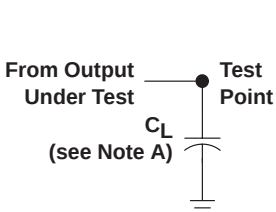
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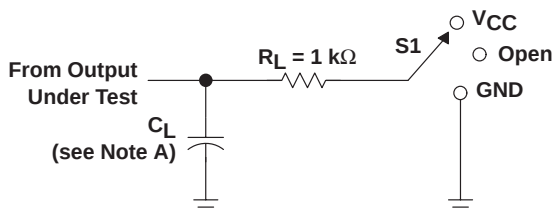
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	28	pF

PARAMETER MEASUREMENT INFORMATION

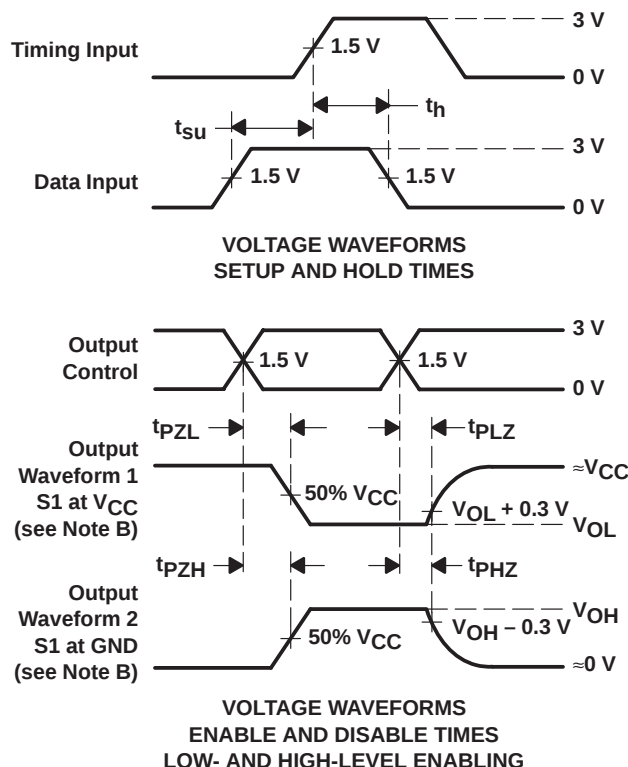
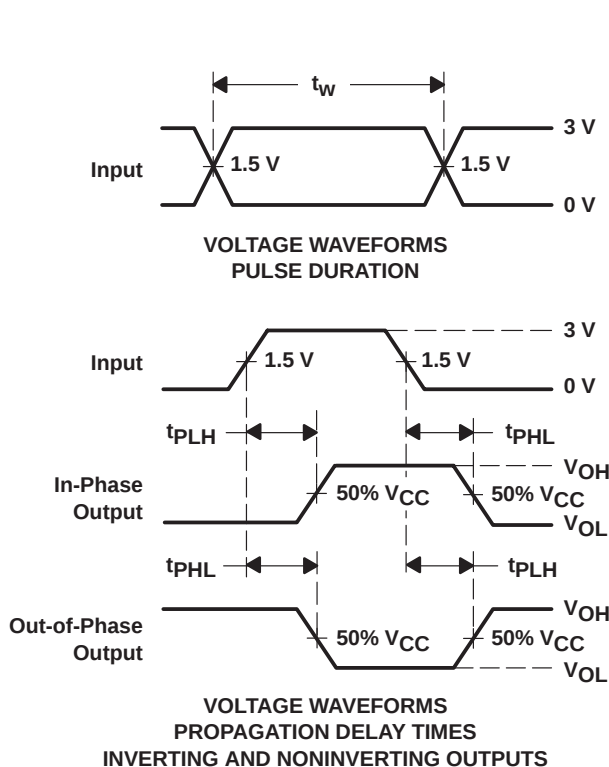


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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