

# FQU20N06L

## N-Channel QFET® MOSFET

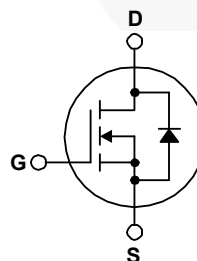
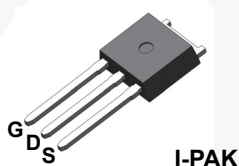
60 V, 17.2 A, 42 mΩ

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### Features

- 17.2 A, 60 V,  $R_{DS(on)} = 42 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 8.6 \text{ A}$
- Low Gate Charge (Typ. 9.5 nC)
- Low  $C_{rss}$  (Typ. 35 pF)
- 100% Avalanche Tested
- Low Level Gate Drive Requirements Allowing Direct Operation Form Logic Drivers



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQU20N06LTU	Unit
$V_{DSS}$	Drain-Source Voltage	60	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	17.2	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	10.9	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	68.8	A
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	170	mJ
$I_{AR}$	Avalanche Current (Note 1)	17.2	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	3.8	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	7.0	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	38	W
	- Derate above $25^\circ\text{C}$	0.30	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering, 1/8" from case for 5 seconds.	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQU20N06LTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.28	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	50	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQU20N06LTU	FQU20N06L	IPAK	Tube	N/A	N/A	70 units

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.06	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 48\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	--	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 8.6\text{ A}$	--	0.046	0.06	$\Omega$
		$V_{GS} = 5\text{ V}, I_D = 8.6\text{ A}$	--	0.057	0.075	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 25\text{ V}, I_D = 8.6\text{ A}$	--	11	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	480	630	pF
$C_{oss}$	Output Capacitance		--	175	230	pF
$C_{rss}$	Reverse Transfer Capacitance		--	35	45	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 10.5\text{ A},$ $R_G = 25\text{ }\Omega$	--	10	30	ns
$t_r$	Turn-On Rise Time		--	165	340	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	80	ns
$t_f$	Turn-Off Fall Time	(Note 4)	--	70	150	ns
$Q_g$	Total Gate Charge	$V_{DS} = 48\text{ V}, I_D = 21\text{ A},$ $V_{GS} = 5\text{ V}$	--	9.5	13	nC
$Q_{gs}$	Gate-Source Charge		--	2.5	--	nC
$Q_{gd}$	Gate-Drain Charge		--	5.5	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	--	--	17.2	A		
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current	--	--	68.8	A		
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 17.2 A		--	--	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>F</sub> = 21 A, dI <sub>F</sub> / dt = 100 A/μs		--	54	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge			--	75	--	nC

#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2.  $L = 670\text{ }\mu\text{H}$ ,  $I_{AS} = 17.2\text{ A}$ ,  $V_{DD} = 25\text{ V}$ ,  $R_G = 25\text{ }\Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 21\text{ A}$ ,  $dI/dt \leq 300\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Characteristics

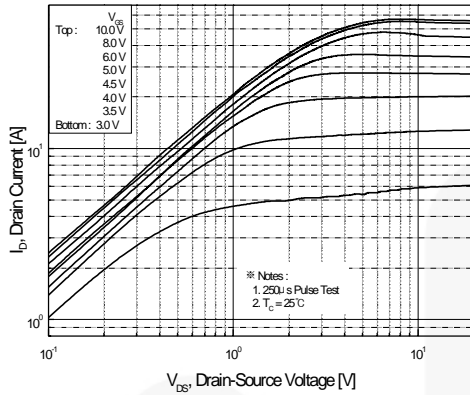


Figure 1. On-Region Characteristics

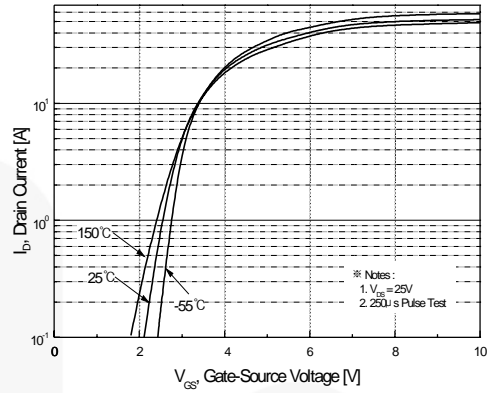


Figure 2. Transfer Characteristics

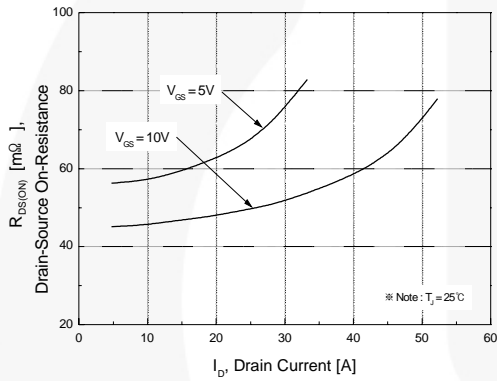


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

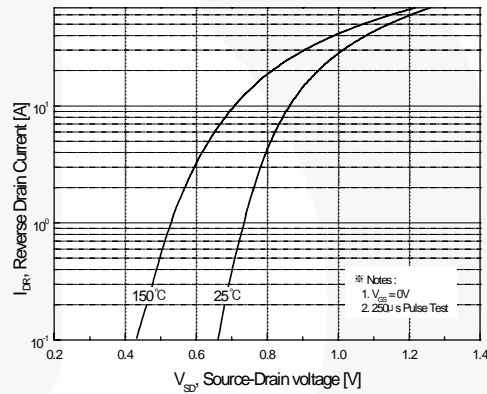


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

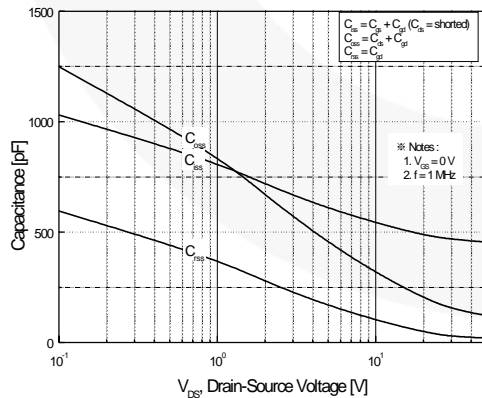


Figure 5. Capacitance Characteristics

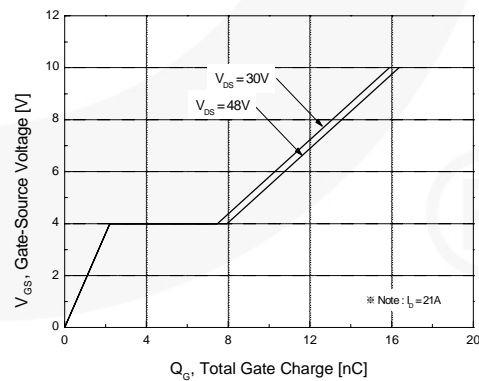


Figure 6. Gate Charge Characteristics

## Typical Characteristics (Continued)

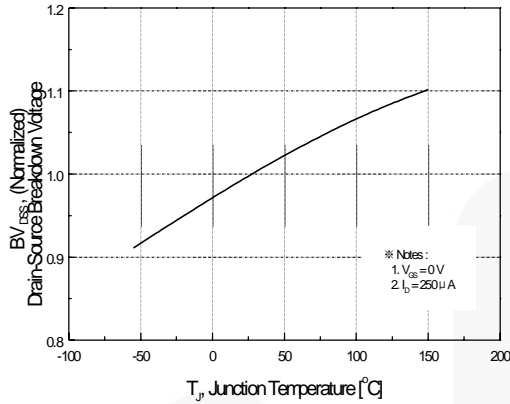


Figure 7. Breakdown Voltage Variation vs. Temperature

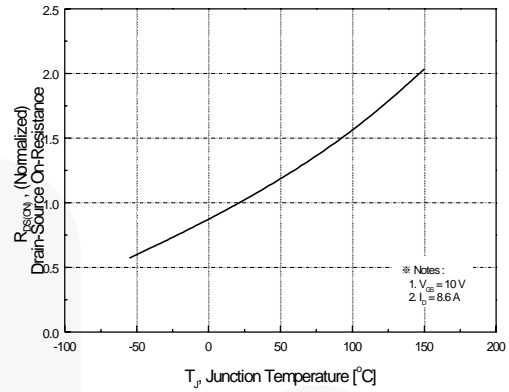


Figure 8. On-Resistance Variation vs. Temperature

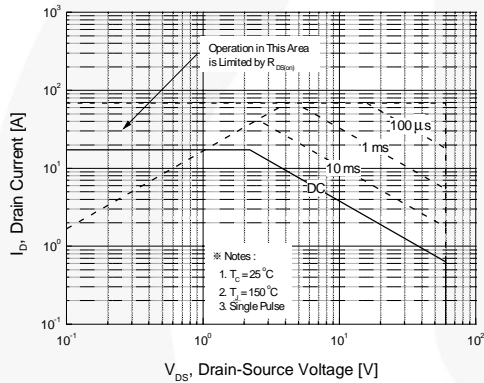


Figure 9. Maximum Safe Operating Area

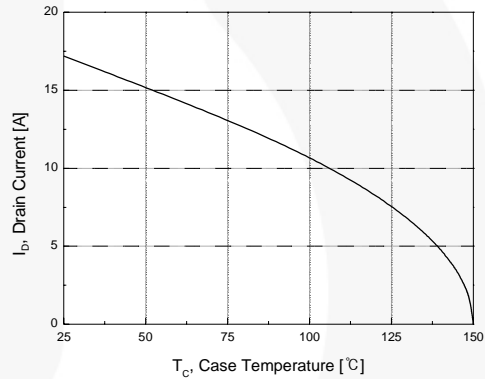


Figure 10. Maximum Drain Current vs. Case Temperature

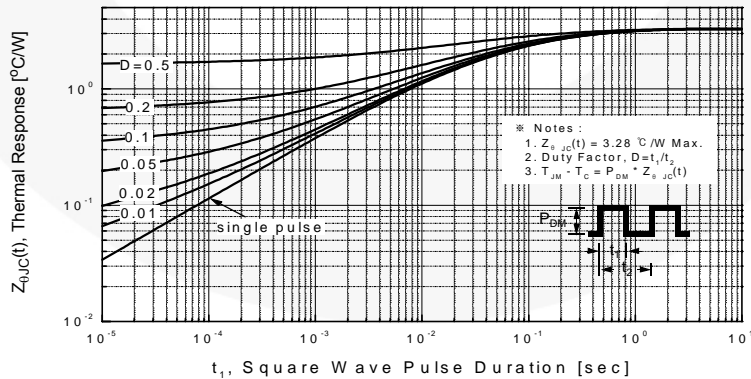


Figure 11. Transient Thermal Response Curve

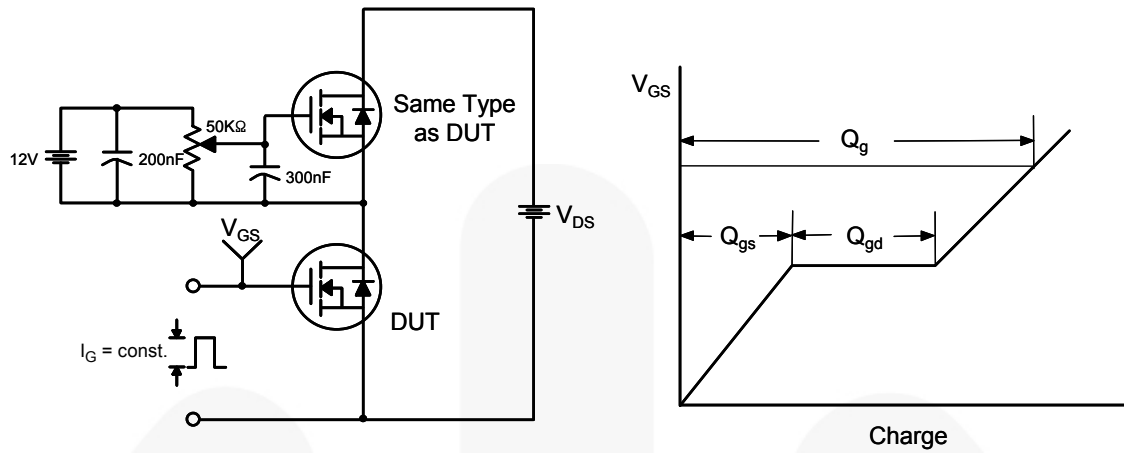


Figure 12. Gate Charge Test Circuit & Waveform

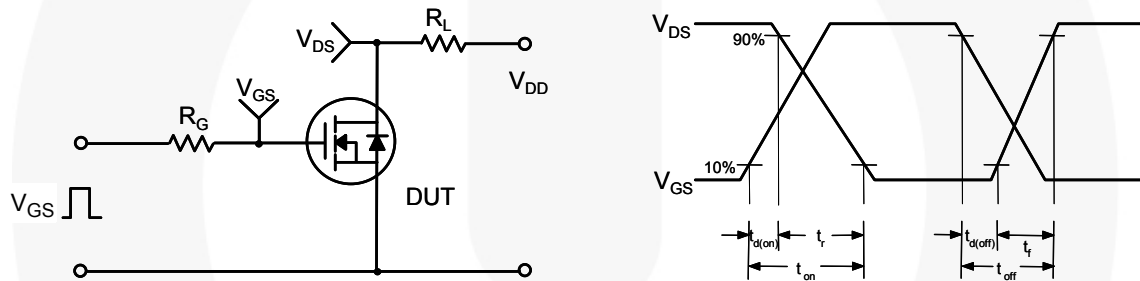


Figure 13. Resistive Switching Test Circuit & Waveforms

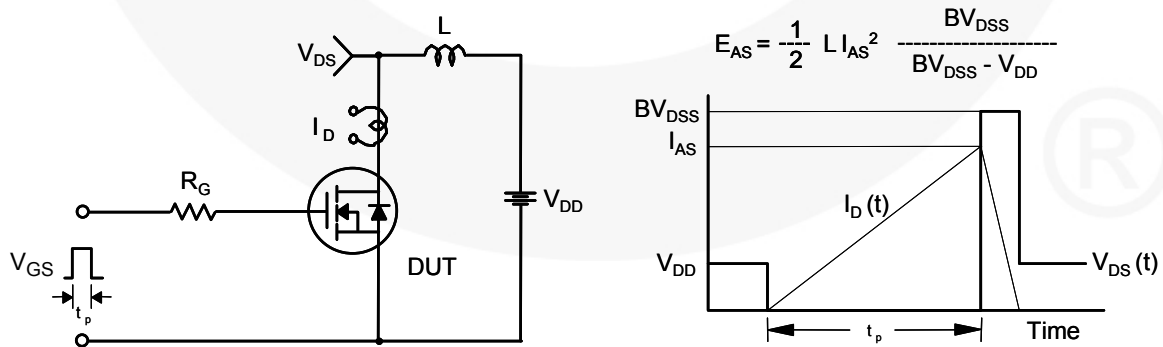


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

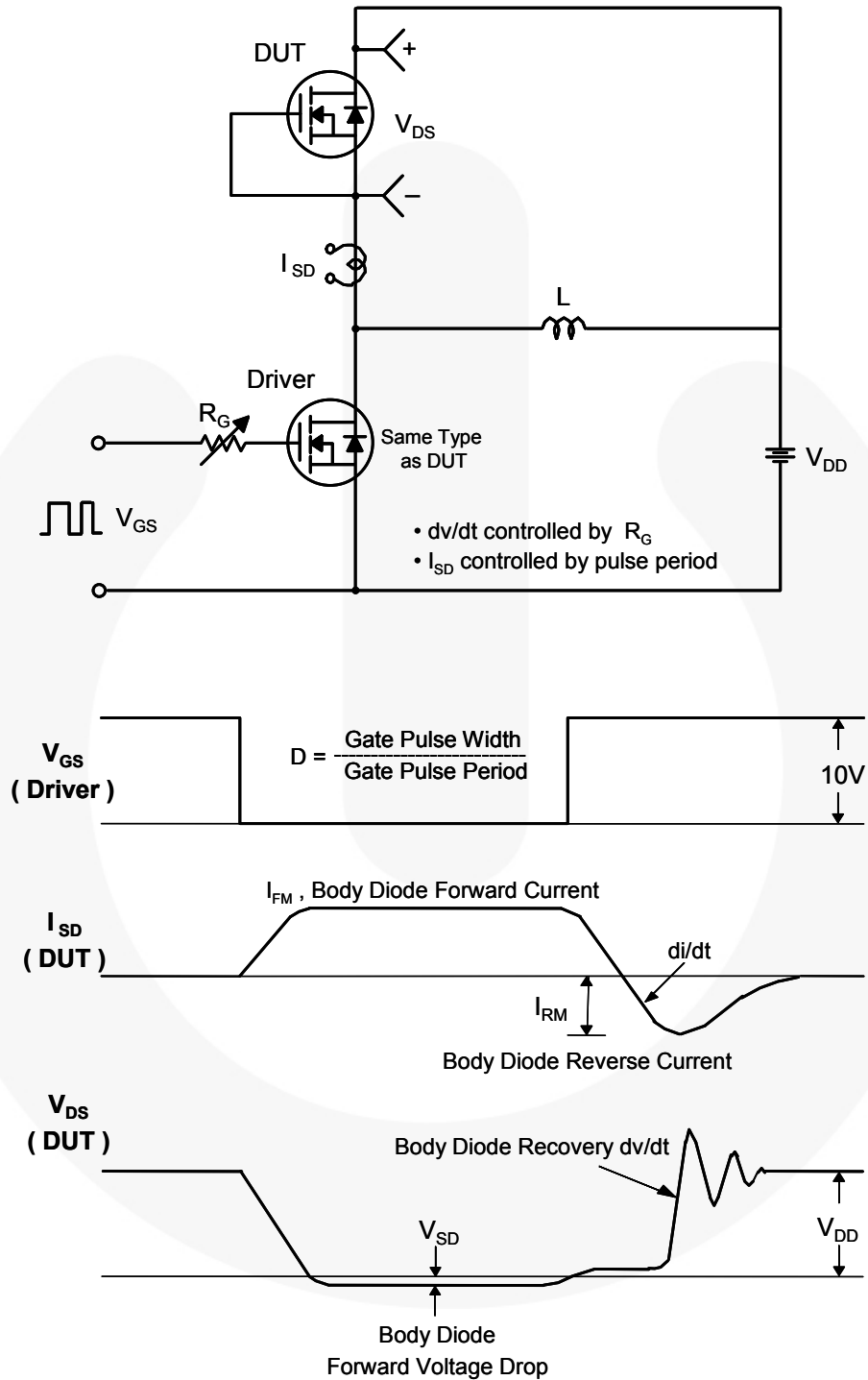
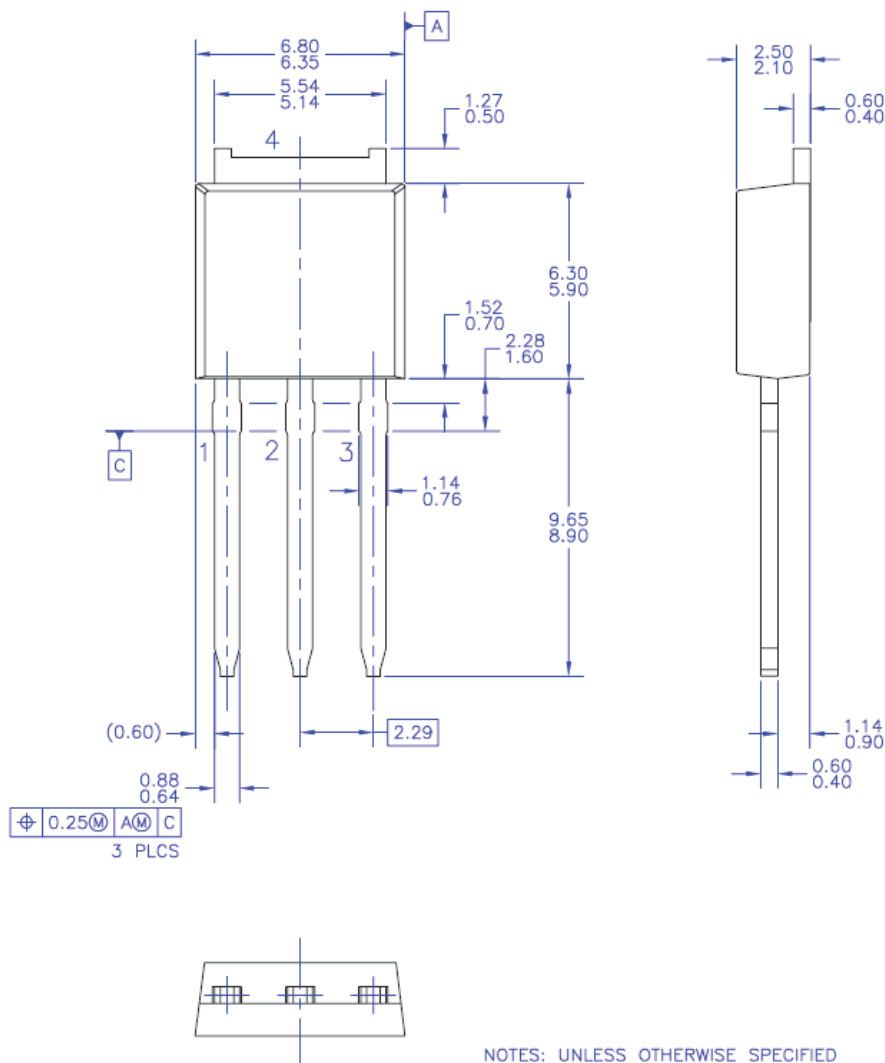


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions

## FQU13N06LTU



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) THIS PACKAGE CONFORMS TO JEDEC, TO-251, ISSUE C, VARIATION AA, DATED SEP 1988.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

Figure 16. TO251 (I-PAK), Molded, 3-Lead

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I66