LP3928 High Speed Bi-Directional Level Shifter and Ultra Low-Dropout CMOS Voltage Regulator

Check for Samples: LP3928

FEATURES

- **Ultra Small DSBGA Package**
- **Bi-directional Level-Shifter for Three Individual Signals: 1.8V to 2.85V and 2.85V to 1.8V Signal Level Translation**
- **Logic Controlled Enable Pins: 4 Different Operation Modes**
- **LDO Stable with Ceramic and High Quality Tantalum Capacitors**
- **Thermal Shutdown**

APPLICATIONS

- **Multi-Media Cards for Cellular Phones**
- **SD Cards for Cellular Handsets**
- **Logic Level Translation**
- **Portable Information Appliances**

KEY SPECIFICATIONS

- **Level Shifter:**
  - **4 ns Propagation Delay (typ.)**
  - **2 ns Rise and Fall Times (typ.)**
  - **20 ns Direction Switch Response Time**
  - **2 µA Input/Output Leakage Current**
- **Low-Dropout Regulator:**
  - **3.05V to 6.0V Input Range**
  - **150 mA Specified Output**
  - **Fast Turn-On Time: 200 µs (typ.)**
  - **100 mV Maximum Dropout with 150 mA Load**

DESCRIPTION

The LP3928 is designed for portable and wireless applications with demanding performance and space requirements.

The LP3928 provides level shifting and power conversion needed for applications interfacing differing voltage levels.

The part contains a bi-directional level shifter for three signals to translate the levels between 1.8V and 2.85V and an ultra low-dropout CMOS 2.85V voltage regulator.

The three level shifted signals are individually direction controlled. Signals going from 2.85V to 1.8V can also be latched using an external clock source. The latches are powered from internal 2.85V. There is also an option to by-pass the latches.

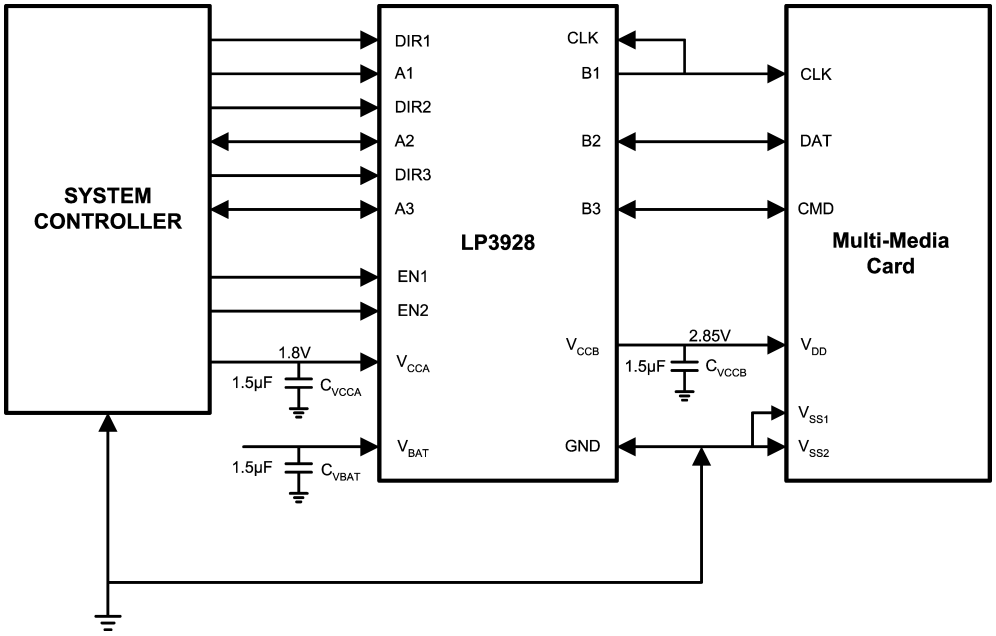
The built-in low-dropout voltage regulator is ideal for mobile phone and battery powered wireless applications. It provides up to 150 mA from a 3.05V to 6.0V input, and is characterized by extremely low dropout voltage, low quiescent current and low output noise voltage. It is stable with small 1.5 µF ±30% ceramic and high quality tantalum output capacitors, requiring smallest possible PC board area.

A shutdown mode is available for the level shifters and the regulator. High performance is achieved over various load conditions with very low rise and fall times.

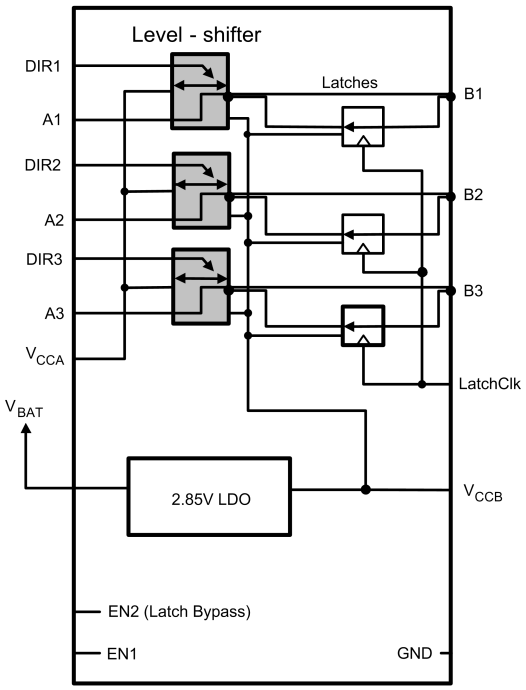
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TYPICAL APPLICATION CIRCUIT



BLOCK DIAGRAM



PACKAGE OUTLINE AND CONNECTION DIAGRAMS

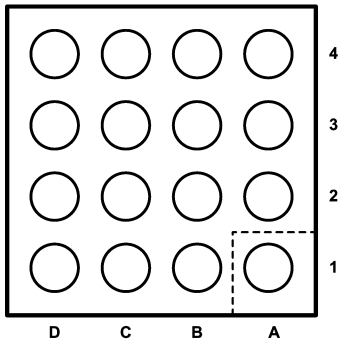


Figure 1. Bottom View
16 Bump DSBGA Package

PIN DESCRIPTIONS

Pin Name	DSBGA Bump Identifier	Logic Level	Function
A1	C4	1.8V	1.8V I/O Channel, (1)
A2	D4	1.8V	1.8V I/O Channel, (2)
A3	D3	1.8V	1.8V I/O Channel, (2)
B1	C1	2.85V	2.85V I/O Channel, (2)
B2	D1	2.85V	2.85V I/O Channel, (2)
B3	D2	2.85V	2.85V I/O Channel, (2)
DIR1	B3	1.8V	Direction control input Channel 1: '1': A→B; 0; B→A
DIR2	B2	1.8V	Direction control input Channel 2: '1': A→B; 0; B→A
DIR3	C3	1.8V	Direction control input Channel 3: '1': A→B; 0; B→A
V_{CCA}	B4		IC supply to the 1.8V side
V_{CCB}	B1		IC supply, 2.85V output from LDO
V_{BAT}	A1		LDO supply, Battery voltage
GND	A3		Power ground connection
EN1	A4	1.8V	Mode pin 1, see Table 1 for modes and settings
EN2	A2	1.8V	Mode pin 2, see Table 1 for modes and settings
LatchClk	C2	2.85V	Clock input: rising edge latches B inputs (DIR=0, normal mode)

(1) Pin pairs A1–B1, A2–B2 and A3–B3 form 3 independent bi-directional level-shifting channels.
(2) Pin pairs A1–B1, A2–B2 and A3–B3 form 3 independent bi-directional level-shifting channels.

Table 1. Operation Modes

Inputs		State
EN1	EN2	
0	0	Level shifter off: High Z state on A_1–A_3, B_1–B_3, LDO off
0	1	Level shifter off: High Z state on A_1–A_3, B_1–B_3, LDO on
1	0	Latch bypassed in B to A direction, LDO=on (1)
1	1	ON, normal mode (latch active)

(1) LatchClk is not used here. It should not be left floating.

Table 2. Direction Control and LatchCLK (Normal Mode)

Inputs		Outputs and Direction
DIRx	LatchClk	
1	X	Ax to Bx
0	↓	No change (on Ax)
0	↑	Bx to Ax, see example

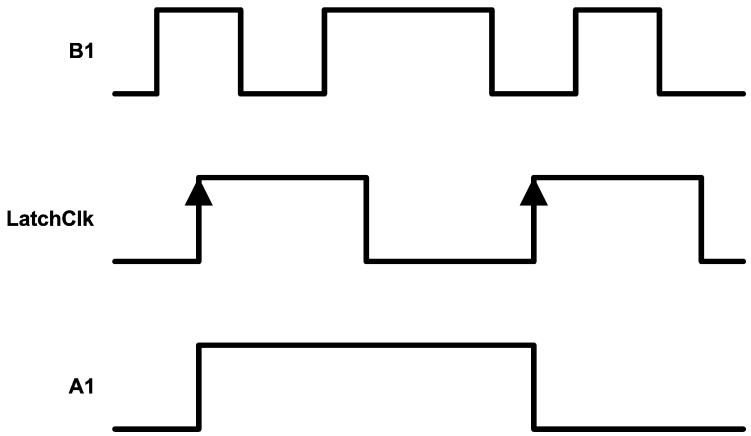


Figure 2. Example for Latch Mode, DIR1 = '0', EN1 = EN2 = '1' (delay not shown)

ABSOLUTE MAXIMUM RATINGS (1) (2)

V_{BAT}, V_{CCB}	−0.2V to +6.5V
V_{CCA}	−0.2V to +3.3V
A_1–A_3, EN, DIR	−0.2V to V_{CCA} + 0.2V
B_1–B_3, LatchClk	−0.2V to V_{CCB} + 0.2V
Junction Temperature	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (3)	235°C
Pad Temperature (3)	235°C
Power Dissipation (4) θ_{JA} (DSBGA), typical	180°C/W
Maximum Power Dissipation, DSBGA	360 mW
ESD Rating (5) Human Body Model	2 kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test condition, see Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) Additional information on lead temperature and pad temperature can be found in TI Application Note AN-1112(SNVS009).
(4) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula$P = (T_J - T_A)/\theta_{JA}$,Where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 360 mW rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150°C, for T_J, 85°C for T_A, and 180°C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 85°C. The thermal resistance can be better or worse than 180°C/W depending on board layout. Larger copper planes and thermal vias should be used to conduct heat away from the DSBGA solder bumps.
(5) The Human Body Model is 100 pF discharged through 1.5 kΩ resistor into each pin.

OPERATING CONDITIONS (1) (2)

V_{BAT}	3.05V to 6.0V
V_{CCA}	1.65V to 1.95V
V_{CCB}	(3)
Junction Temperature	−40°C to +125°C
Ambient Temperature	−40°C to +85°C
Maximum Power Dissipation (4)	220 mW

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test condition, see Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) V_{CCB} can be supplied from an external voltage source in the range of 1.65V to 3.6V, as long as both V_{BAT} and V_{CCB} are connected to the external source. Only the LDO quiescent current (see DC electrical specifications) will add to the level-shifter current consumption. This Operating Rating does not imply specified performance. For specified performance limits and associated test conditions, see Electrical Characteristics tables.
(4) Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 220 mW rating appearing under Operating Ratings results from substituting the maximum junction temperature for operation, 125°C, for T_J, 85°C for T_A, and 180°C/W for θ_{JA} into (1) above. More power can be dissipated at ambient temperatures below 85°C. The thermal resistance can be better or worse than 180°C/W depending on board layout. Larger copper planes and thermal vias should be used to conduct heat away from the DSBGA solder bumps.

ELECTRICAL CHARACTERISTICS: LEVEL SHIFTER DC VOLTAGE LEVELS

Unless otherwise specified: H = V_{IH} min, L = V_{IL} max, C_{VBAT} = 1 µF, I_{OUT} = 1 mA, C_{VCCB} = 1 µF, C_{VCCA} = 1 µF. Typical values and limits appearing in standard typeface apply for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (1)

Unless otherwise specified: EN1 = H, EN2 = X; 3.05V ≤ V_{BAT} ≤ 6V, 1.65V ≤ V_{CCA} ≤ 1.95V.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IHA}	High Level Input Voltage	For A Pins		**V_{CCA}*0.65**		**V_{CCA}+0.2**	V
V_{ILA}	Low Level Input Voltage			**0**		**V_{CCA}*0.35**	V
V_{OHA}	High Level Output Voltage	For A Pins	I_{OH}=4 mA	**V_{CCA}−0.45**	1.5	**V_{CCA}+0.2**	V
V_{OLA}	Low Level Output Voltage		I_{OL}=4 mA	**0**	0.1	**V_{CCA}*0.25**	V
V_{IHB}	High Level Input Voltage	For B Pins		**V_{CCB}*0.7**		**V_{CCB}+0.2**	V
V_{ILB}	Low Level Input Voltage			**0**		**V_{CCB}*0.3**	V
V_{OHB}	High Level Output Voltage	For B Pins	I_{OH}=4 mA	**V_{CCB}*0.7**	2.75	**V_{CCB}+0.2**	V
V_{OLB}	Low Level Output Voltage		I_{OL}=4 mA	**0**	0.1	**V_{CCB}*0.2**	V
$V_{IHEN-DIR}$	High Level Input Voltage	For EN and DIR Pins		**V_{CCA}*0.75**		**V_{CCA}+0.2**	V
$V_{ILEN-DIR}$	Low Level Input Voltage			**0**		**V_{CCA}*0.27**	V
$V_{IHLatClk}$	High Level Input Voltage	For LatchClk Pin		**V_{CCB}*0.7**		**V_{CCB}+0.2**	V
$V_{ILLatClk}$	Low Level Input Voltage			**0**		**V_{CCA}*0.3**	V

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

ELECTRICAL CHARACTERISTICS: LEVEL SHIFTER DC CURRENT LEVELS

Unless otherwise specified: EN1 = H, EN2 = X; V_{BAT} = 6V or V_{CCA} = 1.95V as applicable to B or A respectively.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IA}	Input Leakage Current Ai	Vi_A=0/1.9V, DIRi=H (V_{CCA} = 1.8V when Vi_A = 1.9V)		0.001	**±2**	µA
I_{IDIR_EN}	Input Leakage Current DIR/EN (1)	Vi=0/1.9V (V_{CCA} = 1.8V when Vi = 1.9V)		0.001	**±2**	µA
I_{IB}	Input Leakage Current Bi, LatchClk (2)	Vi_B=0/2.95V, DIRi=L		0.001	**±2**	µA
$I_{CHA\rightarrow B}$	Static I_{CCB} Current/Channel Static I_{CCB} Current Total (3) (4)	EN2=H, DIRi=H, Total Includes I_{BCOM}		550 2050	**875** **3330**	µA
$I_{CHB\rightarrow A}$	Static I_{CCB} Current/Channel Static I_{CCB} Current Total (5) (4)	EN2=L, DIRi=L Total Includes I_{BCOM}		2 406	**30** **840**	µA
I_{BCOM}	Common Static Level-Shifter I_{CCB} Current (6) (4)			400	**750**	µA
I_A	Static Level-Shifter I_{CCA} Current (7) (4)			90	**165**	µA
I_{CCBEXT}	Off State I_{CCB} Current with External V_{CCB} (8)	V_{BAT}=3.6V, EN1=L, EN2=L		15		µA
I_{OFFA}	Off State V_{CCA} Current	V_{CCA}=1.9V, EN1,2=0, Ai=0V, Bi=0V, DIRi=0V, LatchClk=0V		1.5	**5**	µA
I_{OFFBAT}	Off State V_{BAT} Current	EN1,2=L		0.005	**3**	µA
I_{OZA}	Output Leakage Current Ai	V_{CCA}=1.9V, Vi_A=0/1.9V, EN1=L		0.001	**±2**	µA
I_{OZB}	Output Leakage Current Bi	Vi_B=0V, V_{BAT}=3.35V, V_{CCB}=0, EN1=L		0.001	**±2**	µA
		Vi_B=2.95V, V_{BAT}=3.35V, V_{CCB}=2.95V, EN1=L		0.001	**±2**	µA
I_{SCA}	Short Circuit Current/ Channel Ai Output, V_{CCA}=1.9V, DIRi=L, EN2=L	Ai=0V, Bi=H	**−27**	−17		mA
		Ai=V_{CCA}, Bi=L		36	**56**	mA
I_{SCB}	Short Circuit Current/ Channel Bi Output, V_{BAT}=2.95V, DIRi=H	Bi=0V, Ai=H	**−90**	−58		mA
		Bi=2.95V, Ai=L		60	**90**	mA

(1) Input leakage current for pins DIRi, EN1, EN2.
(2) Input leakage current for pins Bi, LatchClk.
(3) This is the static current consumption from V_{CCB} for channel (i) when DIRi=H (A→B direction).
(4) Only $I_{CCBTOTAL}$ for DIR1=DIR2=DIR3=H and $I_{CCATOTAL}$ for DIR1=DIR2=DIR3=L will be tested in production.
Calculation example: assuming DIR1=H, DIR2=L, DIR3=L, then the typical I_{CCB} current will be:
$I_{CCBTOTAL} = I_{BCOM} + I_{CHA\rightarrow B} + 2 * I_{CHB\rightarrow A}$ = 450 µA + 530 µA + 2 * 2 µA = 984 µA
The typical I_{CCA} current is: $I_{CCATOTAL} = I_A$ = 90 µA.
(5) This is the static current consumption from V_{CCB} for channel (i) when DIRi=L (B→A direction).
(6) This is the static current consumption from V_{CCB} for the part common to the channels.
(7) This is the static current consumption from V_{CCA} for the part common to the channels.
(8) V_{CCB} can be supplied from an external voltage source in the range of 1.65V to 3.6V, as long as both V_{BAT} and V_{CCB} are connected to the external source. Only the LDO quiescent current (see DC electrical specifications) will add to the level-shifter current consumption. This Operating Rating does not imply specified performance. For specified performance limits and associated test conditions, see Electrical Characteristics tables.

ELECTRICAL CHARACTERISTICS: LEVEL SHIFTER AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified: EN1 = H, 3.05V ≤ V_{BAT} ≤ 6V, 1.65V ≤ V_{CCA} = 1.95V. ((1), (2))

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	C_{LB} = 35 pF, C_{LA} = 15 pF		4	**7**	ns
t_{PLH}		C_{LB} = 35 pF, C_{LA} = 15 pF		4	**7**	ns
t_R	Rise Time	C_{LB} = 35 pF, C_{LA} = 15 pF		2	**4**	ns
t_F	Fall Time	C_{LB} = 35 pF, C_{LA} = 15 pF		2	**4**	ns
t_{MATCH}	Delay Differences between Channel Outputs at Identical Input Signals				**1.5**	ns
t_{SL}	Latch Set Up Time			1	**2**	ns
t_{HL}	Latch Hold Time			1	**2**	ns
t_{LS}	Level-Shifter Mode Switch Response Time	(3)			**100**	ns
t_{DIR}	Level-Shifter Direction Switch Response Time	(4)			**20**	ns

(1) Unused inputs must be terminated.
(2) This electrical specification is ensured by design.
(3) This is the time it takes either to switch the level shifter on or off, or the time it takes to turn the latch by-pass on/off.
(4) This is the time it takes to switch the direction of the level shifter. After this time a signal can be applied on the new input. For the B→A direction, if EN2=1, the latch set-up time has to be considered separately.

ELECTRICAL CHARACTERISTICS: LDO ELECTRICAL CHARACTERISTICS

Unless otherwise specified: EN1 = L, EN2 = H; V_{OUTnom} = 2.85V, V_{BAT} = $V_{OUT(nom)}$ + 0.5V.

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1 mA		−2 **−3**	2 **3**	% of $V_{OUT(nom)}$
	Line Regulation Error (1)	V_{BAT} = ($V_{OUT(nom)}$ + 0.5V) to 6.0V, I_{OUT} = 1 mA		**−0.10**	**0.10**	%/V
	Load Regulation Error (2)	I_{OUT} = 1 mA to 150 mA			**0.005**	%/mA
	Output AC Line Regulation	V_{BAT} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 100 mA, C_{OUT} = 4.7 µF (Figure 3)	1.5			mV_{PP}
PSRR	Power Supply Rejection Ratio (3)	V_{BAT} = $V_{OUT(nom)}$ + 1V, f = 1 kHz, I_{OUT} = 50 mA, (Figure 4)	40			dB
		V_{BAT} = $V_{OUT(nom)}$ + 1V, f = 50 kHz, I_{OUT} = 50 mA, (Figure 4)	20			
I_Q	Quiescent Current	I_{OUT} = 1mA	85		**150**	µA
		I_{OUT} = 1 mA to 150 mA	130		**200**	
ΔV_{DO}	Dropout Voltage (4)	I_{OUT} = 1 mA	0.4		**2**	mV
		I_{OUT} = 50 mA	20		**35**	
		I_{OUT} = 100 mA	45		**70**	
		I_{OUT} = 150 mA	60		**100**	
I_{SC}	Short Circuit Current Limit	V_{BAT} = 6V, Output Grounded (Steady State)	500			mA
$I_{OUT(PK)}$	Peak Output Current	V_{OUT} ≥ $V_{OUT(nom)}$ − 5%, V_{BAT} = 6V	460	**200**		mA
T_{ON}	Turn-On Time (5) (3)		200	**130**	**430**	µs
ρn (1/f)	Output Noise Density	f = 1 kHz, C_{OUT} = 1 µF	0.6			µV/√Hz
e_n	Output Noise Voltage	BW = 10 Hz to 100 kHz, C_{OUT} = 1 µF	45			µVrms
Output Capacitor	Output Filter Capacitance(6)	V_{BAT} = 3.05V to 6V, I_{OUT} = 1mA to 150 mA		**1**	**22**	µF
	Output Filter Capacitance ESR (7)	V_{BAT} = 3.05V to 6V, I_{OUT} = 1mA to 150 mA		**5**	**500**	mΩ
Thermal Shutdown	Thermal Shutdown Temperature (8)		160			°C
	Thermal Shutdown Hysteresis		20			°C

(1) The output voltage changes slightly with line voltage. An increase in the line voltage results in a slight increase in the output voltage and vice versa.
(2) The output voltage changes slightly with load current. An increase in the load current results in a slight decrease in the output voltage and vice versa.
(3) This electrical specification is ensured by design.
(4) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its normal value. This specification does not apply for input voltages below 2.7V.
(5) Turn-on time is that between the enable input just exceeding V_{IH} and the output voltage just reaching 95% of its nominal value.
(6) Range of capacitor values for which the device will remain stable. This electrical specification is ensured by design.
(7) Range of capacitor ESR values for which the device will remain stable. This electrical specification is ensured by design.
(8) The built-in thermal shut-down of the LDO is also used to put all Ai and Bi outputs in tristate mode.

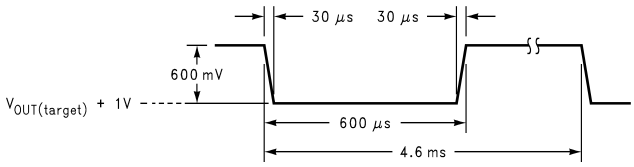


Figure 3. Output AC Line Regulation

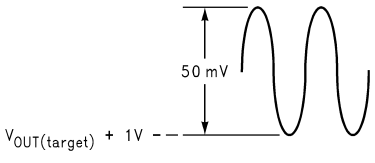


Figure 4. PSRR Input Perturbation

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: C_{VBAT} = 1 µF, C_{VCCA} = 1 µF, C_{VCCB} = 1 µF, V_{BAT} = 3.3V, V_{CCA} = 1.8V, T_A = 25°C.

Level Shifter Propagation Delay A→B

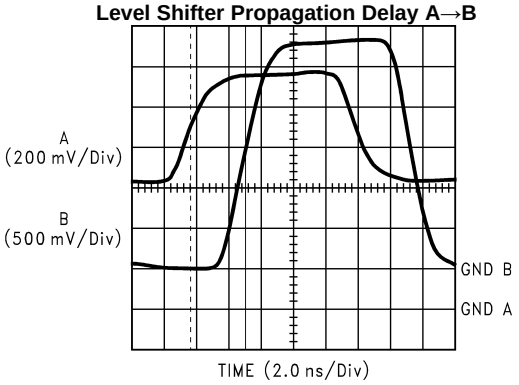


Figure 5.

Level Shifter Propagation Delay B→A

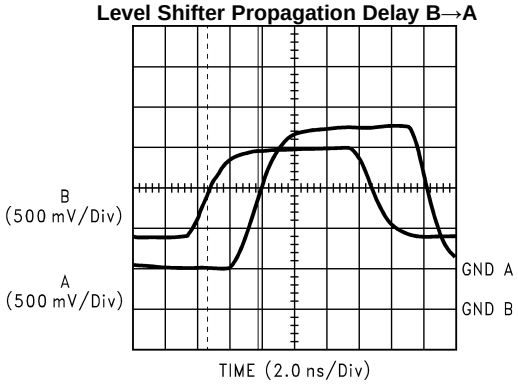


Figure 6.

Power Supply Rejection Ratio (V_{BAT}=3.46V)

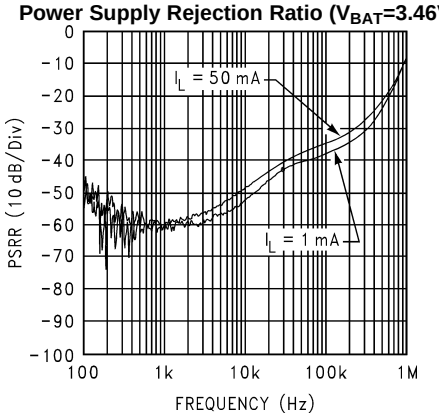


Figure 7.

APPLICATION HINTS

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3928 requires external capacitors for regulator stability. The LP3928 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitance of ≅ 1 µF is required between the LP3928 V_{BAT} pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the V_{BAT} pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be specified by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≅ 1 µF over the entire operating temperature range.

FAST ON-TIME

The LP3928 utilizes a speed up circuitry to ramp up the internal V_{REF} voltage to its final value to achieve a fast output turn on time.

CAPACITOR CHARACTERISTICS

The LP3928 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1 µF to 4.7 µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3928.

The ceramic capacitor's capacitance can vary with temperature.

Most large value ceramic capacitors (≅ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in ceramic capacitor is X7R, which holds the capacitance within ±15%.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 4.7 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

OUTPUT CAPACITOR

The LP3928 is designed specifically to work with very small ceramic output capacitors, any ceramic capacitor (dielectric types Z5U, Y5V or X7R) in 1.5 µF to 22 µF range with 5 mΩ to 500 mΩ ESR range is suitable in the LP3928 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see section Capacitor Characteristics).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range.

The output capacitor should be placed as near to the V_{CCB} pin as possible.

NO-LOAD STABILITY

The LDO of the LP3928 will remain stable and in regulation with no external load connected to the LDO output V_{CCB}. This is especially important in CMOS RAM keep-alive applications.

LEVEL SHIFTER DIRECTION CONTROL AND LATCH CLOCK

The direction of the level shifter is set to Ax→Bx by pulling the DIRx pin to high. The direction of each of the three channels can be set individually. In this mode a change at the LatchClk pin has no effect.

A low at the DIRx pin sets the direction to Bx→Ax. If EN2 is set to high (enabling latch mode), a rising edge of LatchClk will update Ax depending on the level at Bx. A falling edge of LatchClk will not change Ax.

DSBGA ASSEMBLY

For assembly recommendations of DSBGA package please refer to TI Application Note AN-1112(SNVS009).

DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct sunlight will cause misoperation of the device. Light sources such as Halogen lamps can effect electrical performance if brought near to the device.

The wavelengths which have most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance.

A DSBGA test board was brought to within 1 cm of a fluorescent desk lamp and the effect on the regulated output voltage was negligible, showing a deviation of less than TBD from nominal.

OPERATION MODES, EN1 AND EN2

The output of the LDO (V_{CCB}) is turned off and the level shifter channels are set to a high Z state by pulling the enable input pins EN1 and EN2 low.

EN1=0 and EN2=1 turns the LDO on and the level shifter off.

EN1=1 and EN2=0 turns the LDO on and the latch of the level shifter is bypassed in B to A direction. The Latch Clock is not used in this mode. The LatchClk pin should not be left floating but actively terminated.

EN1=1 and EN2=1 turns the LDO on and activates the latch in B to A direction.

To assure proper operation, the signal source used to drive the EN input pins must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under Level Shifter DC Voltage Levels.

Both pins, EN1 and EN2 must be actively terminated.

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3928TLX-1828/NOPB	ACTIVE	DSBGA	YZR	16		TBD	Call TI	Call TI		L8B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

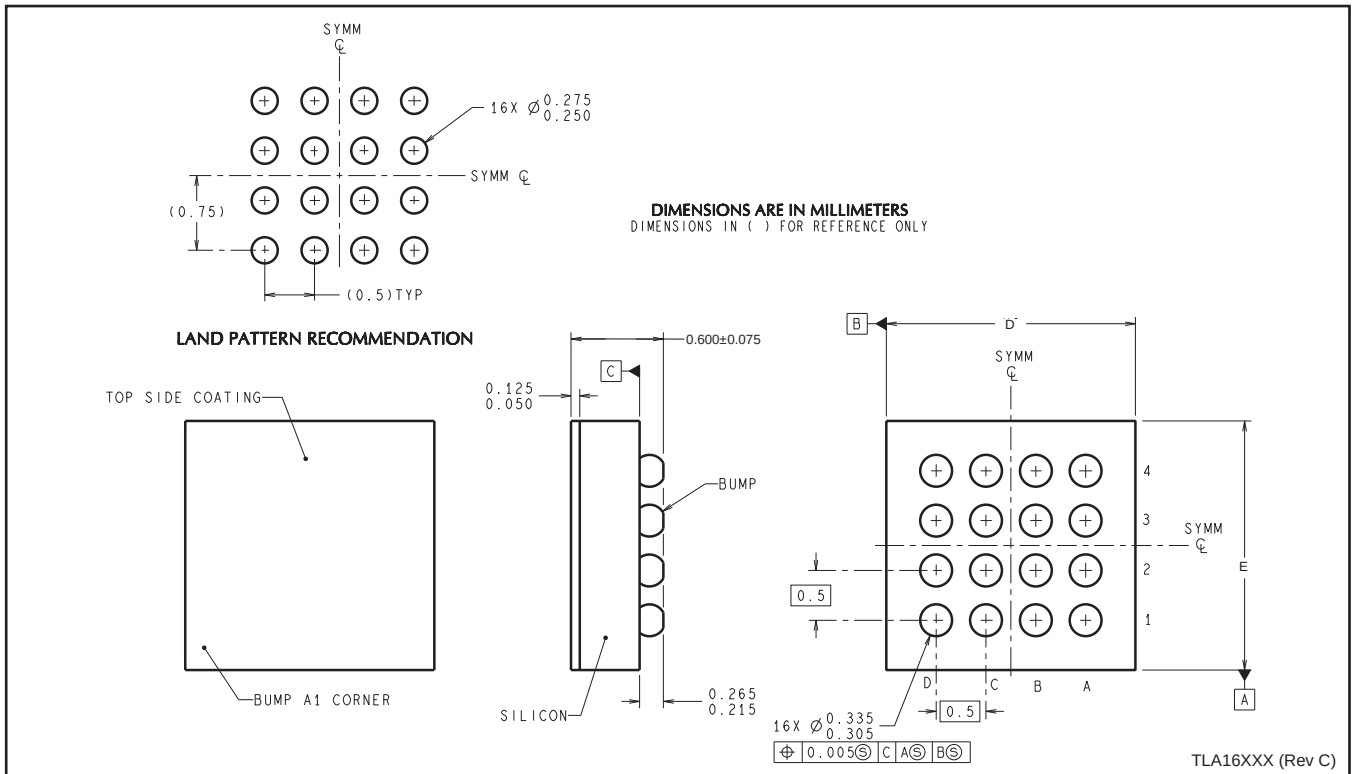
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

YZR0016



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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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