

TMXF28155 Supermapper™ 155/51 Mb/s SONET/SDH xDS3/DS2/DS1/E1/DS0

1 Introduction

The last issue of this data sheet was October 13, 2003. A change history can be found in [Section 9, Change History, on page 63](#). Red change bars have been installed on all text, figures, and tables that were added or changed. All changes to the text are highlighted in red. Changes within figures, and the figure title itself, are highlighted in red, if feasible. Formatting or grammatical changes have not been highlighted. Deleted sections, paragraphs, figures, or tables will be specifically mentioned.

This document is based on the June 2002 *Supermapper* data sheet with some clarifications. The documentation package for the TMXF28155 *Supermapper* 155/51 Mb/s SONET/SDH xDS3/DS2/DS1/E1/DS0 system chip consists of the following documents:

- The *Supermapper Family Register Description* and the *Supermapper Family System Design Guide*. These two documents are available on a password-protected website.
- The *Supermapper Product Description*, and the *Supermapper Hardware Design Guide* (this document). These two documents are available on the public website shown below.

To access related documents, including the documents mentioned above, please go to the following public website, or contact your Agere representative (see the last page of this document).

http://www.agere.com/enterprise_metro_access/mappers_muxes.html

This document describes the hardware interfaces to the Agere Systems Inc. TMXF28155 *Supermapper* device. Information relevant to the use of the device in a board design is covered. Pin descriptions, dc electrical characteristics, timing diagrams, ac timing parameters, packaging, and operating conditions are included.

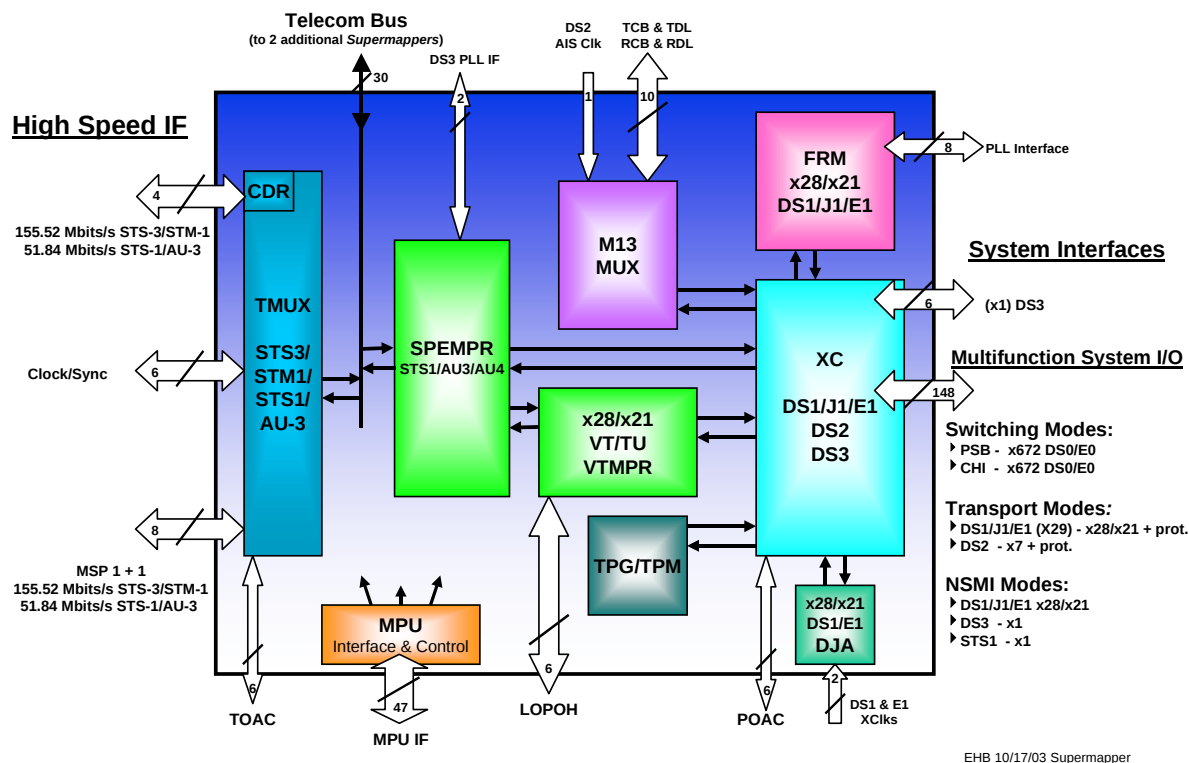


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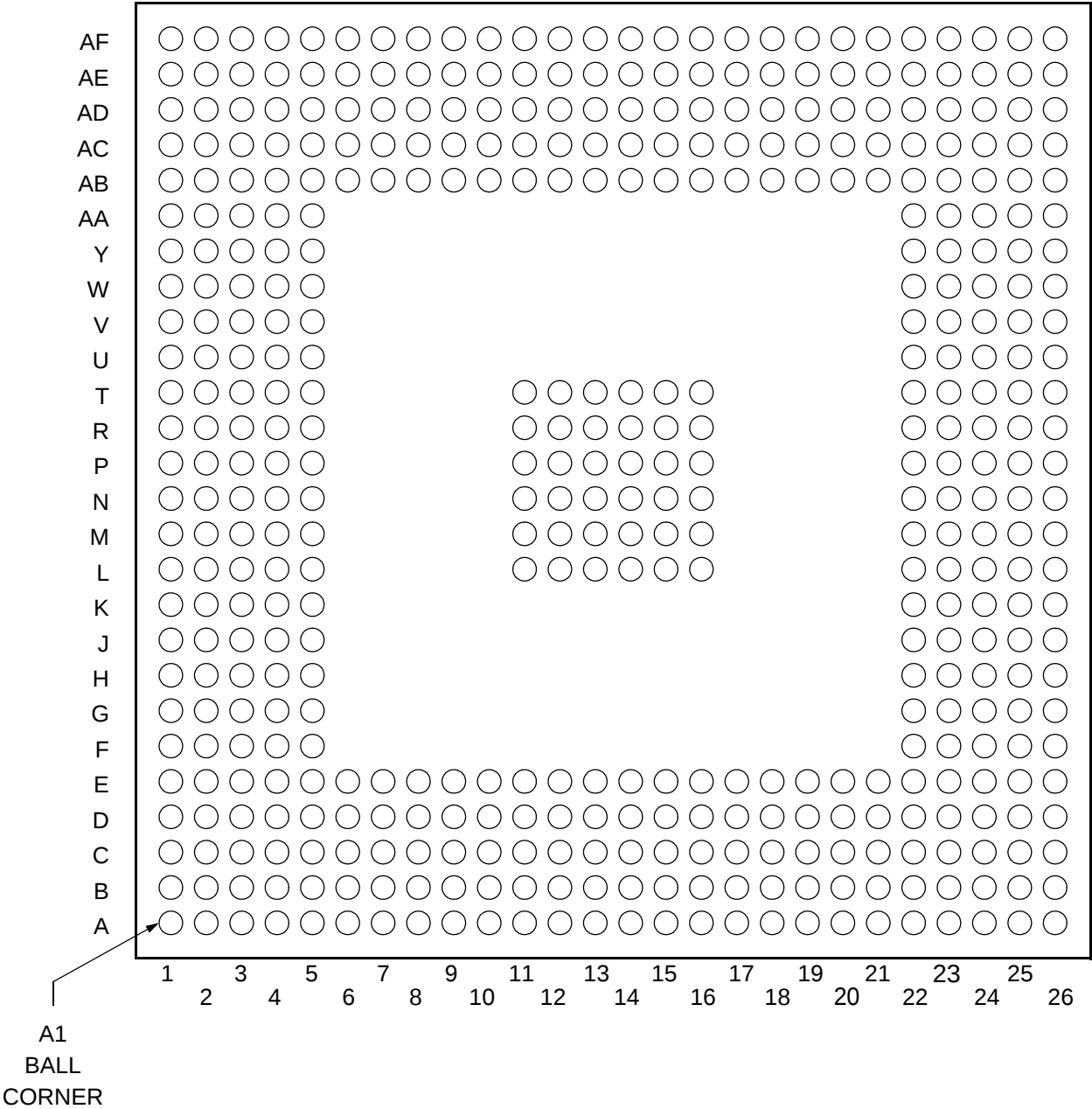
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2 Pin Information

2.1 456-Pin PBGA Pin Diagram

The TMXF28155 *Supermapper* is housed in a 456-pin plastic ball grid array. Figure 2-1 shows the ball assignment viewed from the top of the package. The pins are spaced on a 1.0 mm pitch.



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Figure 2-1. Pin Diagram of 456-Pin PBGA (Bottom View)

2.2 Pin Assignments for 456-Pin PBGA by Pin Number Order

Table 2-1. Pin/Name

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	VDD	B22	LINETXDATA10	D17	LINETXDATA4	G2	LINERXDATA10
A2	VSS	B23	LINETXDATA11	D18	LINETXDATA5	G3	LINERXCLK11
A3	LINERXDATA17	B24	LINETXDATA12	D19	LINETXSYNC7	G4	LINERXCLK10
A4	LINERXDATA18	B25	LINETXCLK13	D20	LINETXCLK8	G5	VSS
A5	VDD	B26	VSS	D21	LINETXDATA9	G22	VSS
A6	VSS	C1	LINERXSYNC15	D22	LINETXSYNC11	G23	LINETXCLK19
A7	LINERXDATA21	C2	LINERXDATA14	D23	VSS	G24	LINETXCLK18
A8	LINERXSYNC23	C3	LINERXCLK17	D24	LINETXCLK15	G25	LINETXSYNC19
A9	LINERXCLK24	C4	LINERXCLK18	D25	LINETXSYNC16	G26	LINETXDATA18
A10	VDD	C5	LINERXCLK19	D26	LINETXDATA15	H1	LINERXDATA9
A11	VSS	C6	LINERXCLK20	E1	VDD	H2	LINERXCLK9
A12	LINERXDATA27	C7	LINERXCLK21	E2	LINERXDATA12	H3	LINERXSYNC10
A13	LINERXSYNC29	C8	LINERXDATA22	E3	LINERXCLK13	H4	LINERXSYNC9
A14	LINETXDATA1	C9	LINERXSYNC24	E4	LINERXSYNC13	H5	LINERXDATA16
A15	LINETXSYNC3	C10	LINERXCLK25	E5	VDD	H22	RDLDATA
A16	VSS	C11	LINERXCLK26	E6	LINERXSYNC17	H23	LINETXDATA20
A17	VDD	C12	LINERXCLK27	E7	VSS	H24	LINETXDATA19
A18	LINETXCLK6	C13	LINERXDATA28	E8	TDLCLK	H25	LINETXCLK20
A19	LINETXDATA7	C14	LINETXSYNC2	E9	TDLCLK	H26	LINETXSYNC20
A20	LINETXSYNC9	C15	LINETXCLK3	E10	DS2AISCLK	J1	LINERXCLK8
A21	VSS	C16	LINETXCLK4	E11	VDD	J2	LINERXSYNC8
A22	VDD	C17	LINETXCLK5	E12	TCBCLK	J3	LINERXDATA8
A23	LINETXSYNC12	C18	LINETXDATA6	E13	TCBCLK	J4	LINERXDATA7
A24	LINETXSYNC13	C19	LINETXSYNC8	E14	TCBSYNC	J5	LINERXCLK16
A25	VSS	C20	LINETXCLK9	E15	RCBCLK	J22	DS3DATAINCLK
A26	VDD	C21	LINETXCLK10	E16	VDD	J23	LINETXSYNC22
B1	VSS	C22	LINETXCLK11	E17	RCBCLK	J24	LINETXSYNC21
B2	LINERXCLK15	C23	LINETXCLK12	E18	RCBSYNC	J25	LINETXDATA21
B3	LINERXSYNC18	C24	LINETXCLK14	E19	RDLCLK	J26	LINETXCLK21
B4	LINERXSYNC19	C25	LINETXSYNC15	E20	VSS	K1	VDD
B5	LINERXSYNC20	C26	LINETXDATA14	E21	LINETXDATA13	K2	LINERXSYNC7
B6	LINERXDATA20	D1	LINERXSYNC14	E22	VDD	K3	LINERXCLK7
B7	LINERXSYNC22	D2	LINERXDATA13	E23	LINETXDATA16	K4	LINERXDATA6
B8	LINERXCLK23	D3	LINERXCLK14	E24	LINETXCLK16	K5	LINERXSYNC16
B9	LINERXDATA24	D4	VSS	E25	LINETXSYNC17	K22	DS3NEGDATAIN
B10	LINERXDATA25	D5	LINERXDATA19	E26	VDD	K23	LINETXSYNC23
B11	LINERXDATA26	D6	LINERXSYNC21	F1	VSS	K24	LINETXCLK22
B12	LINERXSYNC28	D7	LINERXCLK22	F2	LINERXSYNC12	K25	LINETXDATA22
B13	LINERXCLK29	D8	LINERXDATA23	F3	LINERXCLK12	K26	VDD
B14	LINETXCLK1	D9	LINERXSYNC25	F4	LINERXDATA11	L1	VSS
B15	LINETXDATA2	D10	LINERXSYNC26	F5	LINERXDATA15	L2	LINERXSYNC6
B16	LINETXSYNC4	D11	LINERXSYNC27	F22	LINETXSYNC14	L3	LINERXCLK6
B17	LINETXSYNC5	D12	LINERXCLK28	F23	LINETXSYNC18	L4	LINERXDATA5
B18	LINETXSYNC6	D13	LINERXDATA29	F24	LINETXCLK17	L5	VDD
B19	LINETXCLK7	D14	LINETXSYNC1	F25	LINETXDATA17	L11	VSS
B20	LINETXDATA8	D15	LINETXCLK2	F26	VSS	L12	VSS
B21	LINETXSYNC10	D16	LINETXDATA3	G1	LINERXSYNC11	L13	VSS

Table 2-1. Pin/Name

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
L14	VSS	P15	VSS	V1	RLSSPE	AB10	CTAPRH
L15	VSS	P16	VSS	V2	RLSPAR	AB11	VDD
L16	VSS	P22	DS3NEGDATAOUT	V3	RLSJ0J1V1	AB12	VSSA_CDR
L22	VDD	P23	LINETXSYNC27	V4	RLSCLK	AB13	CTAPRP
L23	LINETXSYNC24	P24	LINETXSYNC28	V5	TDO	AB14	LOPOHVALIDIN
L24	LINETXCLK23	P25	LINETXCLK27	V22	PHASEDETUP	AB15	LOPOHCLKOUT
L25	LINETXDATA23	P26	LINETXDATA27	V23	DATA0	AB16	VDD
L26	VSS	R1	RLSDATA7	V24	DATA3	AB17	LOPOHDATAOUT
M1	LINERXSYNC5	R2	LINERXSYNC1	V25	DATA1	AB18	LOPOHVALIDOUT
M2	LINERXDATA4	R3	RLSDATA6	V26	DATA2	AB19	RXDATAEN
M3	LINERXCLK5	R4	LINERXCLK1	W1	TLSDATA6	AB20	VSS
M4	LINERXCLK4	R5	TCK	W2	TLSDATA7	AB21	MODE2_PLL
M5	SCAN_MODE	R11	VSS	W3	TLSDATA5	AB22	VDD
M11	VSS	R12	VSS	W4	RLSV1	AB23	ADDR19
M12	VSS	R13	VSS	W5	TMSN	AB24	INTN
M13	VSS	R14	VSS	W22	TXDATAEN	AB25	DATA15
M14	VSS	R15	VSS	W23	DATA4	AB26	VDD
M15	VSS	R16	VSS	W24	DATA7	AC1	RLSSYNC52
M16	VSS	R22	DS3POSDATAOUT	W25	DATA5	AC2	RLSC52
M22	DS3POSDATAIN	R23	LINETXCLK28	W26	DATA6	AC3	TLSC52
M23	LINETXCLK25	R24	LINETXCLK29	Y1	TLSDATA2	AC4	VSS
M24	LINETXCLK24	R25	LINETXDATA28	Y2	TLSDATA3	AC5	TPOACSYNC
M25	LINETXSYNC25	R26	LINETXSYNC29	Y3	TLSDATA1	AC6	AUTO_AIS1
M26	LINETXDATA24	T1	VSS	Y4	TLSDATA4	AC7	RHSCP
N1	LINERXDATA3	T2	RLSDATA4	Y5	VSS	AC8	THSSYNCP
N2	LINERXCLK3	T3	RLSDATA3	Y22	VSS	AC9	VDDA_CDR
N3	LINERXSYNC4	T4	RLSDATA5	Y23	DATA8	AC10	RPSC155P
N4	LINERXSYNC3	T5	VDD	Y24	DATA11	AC11	REF10
N5	SCAN_EN	T11	VSS	Y25	DATA9	AC12	TPSC155P
N11	VSS	T12	VSS	Y26	DATA10	AC13	LOPOHCLKIN
N12	VSS	T13	VSS	AA1	VSS	AC14	LOPOHDATAIN
N13	VSS	T14	VSS	AA2	TLSCLK	AC15	ETOGGLE
N14	VSS	T15	VSS	AA3	TLSPAR	AC16	TSTMUX0
N15	VSS	T16	VSS	AA4	TLSDATA0	AC17	E1XCLK
N16	VSS	T22	VDD	AA5	RTOACSYNC	AC18	CSN
N22	DS3DATAOUTCLK	T23	LINETXDATA29	AA22	ADDR13	AC19	ADDR0
N23	LINETXDATA26	T24	RSTN	AA23	DATA12	AC20	ADDR4
N24	LINETXDATA25	T25	PMRST	AA24	DATA14	AC21	ADDR8
N25	LINETXCLK26	T26	VSS	AA25	DATA13	AC22	ADDR12
N26	LINETXSYNC26	U1	VDD	AA26	VSS	AC23	VSS
P1	LINERXSYNC2	U2	RLSDATA1	AB1	VDD	AC24	ADDR17
P2	LINERXCLK2	U3	RLSDATA0	AB2	TLSSPE	AC25	APS_INTN
P3	LINERXDATA1	U4	RLSDATA2	AB3	TLSV1	AC26	ADDR18
P4	LINERXDATA2	U5	TDI	AB4	TLSJ0J1V1	AD1	RTOACCLK
P5	IDDQ	U22	PHASEDETDOWN	AB5	VDD	AD2	TLSSYNC52
P11	VSS	U23	DTN	AB6	TTOACCLK	AD3	RTOACDATA
P12	VSS	U24	PAR1	AB7	VSS	AD4	RPOACDATA
P13	VSS	U25	PAR0	AB8	TRSTN	AD5	TPOACDATA
P14	VSS	U26	VDD	AB9	IC3STATEN	AD6	AUTO_AIS3

Table 2-1. Pin/Name

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
AD7	RHSFSYNCN	AD25	ADDR16	AE17	MPCLK	AF9	THSDP
AD8	RHSCN	AD26	ADDR15	AE18	ADSN	AF10	VDD
AD9	THSSYNCN	AE1	VSS	AE19	ADDR1	AF11	VSS
AD10	RPSD155P	AE2	TTOACDATA	AE20	ADDR5	AF12	RESHI
AD11	RPSC155N	AE3	RPOACCLK	AE21	ADDR9	AF13	TPSD155P
AD12	REF14	AE4	TPOACCLK	AE22	ADDR11	AF14	TSTPHASE
AD13	TPSC155N	AE5	LOSEXT	AE23	VDDS_PLL	AF15	TSTMODE
AD14	ECSEL	AE6	AUTO_AIS2	AE24	MODE1_PLL	AF16	VSS
AD15	TSTSFTLD	AE7	RHSDN	AE25	ADDR14	AF17	VDD
AD16	DS1XCLK	AE8	THSCN	AE26	VSS	AF18	RWN
AD17	MPMODE	AE9	THSDN	AF1	VDD	AF19	ADDR2
AD18	DSN	AE10	RPSD155N	AF2	VSS	AF20	ADDR6
AD19	ADDR3	AE11	CTAPTH	AF3	TTOACSYNC	AF21	VSS
AD20	ADDR7	AE12	RESLO	AF4	RPOACSYNC	AF22	VDD
AD21	ADDR10	AE13	TPSD155N	AF5	VDD	AF23	VSSA_PLL
AD22	VDDD_PLL	AE14	BYPASS	AF6	VSS	AF24	MODE0_PLL
AD23	VSSS_PLL	AE15	EXDNUF	AF7	RHSDP	AF25	VSS
AD24	CLKIN_PLL	AE16	TSTMUX1	AF8	THSCP	AF26	VDD

2.3 Pin Assignments for 456-Pin PBGA by Signal Name

Table 2-2. Pin Assignments for 456-Pin PBGA by Signal Name

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
ADDR0	AC19	CTAPRP	AB13	ECSEL	AD14	LINERXCLK24	A9
ADDR1	AE19	CTAPTH	AE11	ETOGGLE	AC15	LINERXCLK25	C10
ADDR2	AF19	DATA0	V23	EXDNUP	AE15	LINERXCLK26	C11
ADDR3	AD19	DATA1	V25	IC3STATEN	AB9	LINERXCLK27	C12
ADDR4	AC20	DATA2	V26	IDDQ	P5	LINERXCLK28	D12
ADDR5	AE20	DATA3	V24	INTN	AB24	LINERXCLK29	B13
ADDR6	AF20	DATA4	W23	LINERXCLK1	R4	LINERXDATA1	P3
ADDR7	AD20	DATA5	W25	LINERXCLK2	P2	LINERXDATA2	P4
ADDR8	AC21	DATA6	W26	LINERXCLK3	N2	LINERXDATA3	N1
ADDR9	AE21	DATA7	W24	LINERXCLK4	M4	LINERXDATA4	M2
ADDR10	AD21	DATA8	Y23	LINERXCLK5	M3	LINERXDATA5	L4
ADDR11	AE22	DATA9	Y25	LINERXCLK6	L3	LINERXDATA6	K4
ADDR12	AC22	DATA10	Y26	LINERXCLK7	K3	LINERXDATA7	J4
ADDR13	AA22	DATA11	Y24	LINERXCLK8	J1	LINERXDATA8	J3
ADDR14	AE25	DATA12	AA23	LINERXCLK9	H2	LINERXDATA9	H1
ADDR15	AD26	DATA13	AA25	LINERXCLK10	G4	LINERXDATA10	G2
ADDR16	AD25	DATA14	AA24	LINERXCLK11	G3	LINERXDATA11	F4
ADDR17	AC24	DATA15	AB25	LINERXCLK12	F3	LINERXDATA12	E2
ADDR18	AC26	DS1XCLK	AD16	LINERXCLK13	E3	LINERXDATA13	D2
ADDR19	AB23	DS2AISCLK	E10	LINERXCLK14	D3	LINERXDATA14	C2
ADSN	AE18	DS3DATAINCLK	J22	LINERXCLK15	B2	LINERXDATA15	F5
APS_INTN	AC25	DS3DATAOUTCLK	N22	LINERXCLK16	J5	LINERXDATA16	H5
AUTO_AIS1	AC6	DS3NEGDATAIN	K22	LINERXCLK17	C3	LINERXDATA17	A3
AUTO_AIS2	AE6	DS3NEGDATAOUT	P22	LINERXCLK18	C4	LINERXDATA18	A4
AUTO_AIS3	AD6	DS3POSDATAIN	M22	LINERXCLK19	C5	LINERXDATA19	D5
BYPASS	AE14	DS3POSDATAOUT	R22	LINERXCLK20	C6	LINERXDATA20	B6
CLKIN_PLL	AD24	DSN	AD18	LINERXCLK21	C7	LINERXDATA21	A7
CSN	AC18	DTN	U23	LINERXCLK22	D7	LINERXDATA22	C8
CTAPRH	AB10	E1XCLK	AC17	LINERXCLK23	B8	LINERXDATA23	D8

Table 2-2. Pin Assignments for 456-Pin PBGA by Signal Name (continued)

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
LINERXDATA24	B9	LINETXCLK7	B19	LINETXDATA19	H24	LOPOHCLKOUT	AB15
LINERXDATA25	B10	LINETXCLK8	D20	LINETXDATA20	H23	LOPOHDATAIN	AC14
LINERXDATA26	B11	LINETXCLK9	C20	LINETXDATA21	J25	LOPOHDATAOUT	AB17
LINERXDATA27	A12	LINETXCLK10	C21	LINETXDATA22	K25	LOPOHVALIDIN	AB14
LINERXDATA28	C13	LINETXCLK11	C22	LINETXDATA23	L25	LOPOHVALIDOUT	AB18
LINERXDATA29	D13	LINETXCLK12	C23	LINETXDATA24	M26	LOSEXT	AE5
LINERXSYNC1	R2	LINETXCLK13	B25	LINETXDATA25	N24	MODE0_PLL	AF24
LINERXSYNC2	P1	LINETXCLK14	C24	LINETXDATA26	N23	MODE1_PLL	AE24
LINERXSYNC3	N4	LINETXCLK15	D24	LINETXDATA27	P26	MODE2_PLL	AB21
LINERXSYNC4	N3	LINETXCLK16	E24	LINETXDATA28	R25	MPCLK	AE17
LINERXSYNC5	M1	LINETXCLK17	F24	LINETXDATA29	T23	MPMODE	AD17
LINERXSYNC6	L2	LINETXCLK18	G24	LINETXSYNC1	D14	PAR0	U25
LINERXSYNC7	K2	LINETXCLK19	G23	LINETXSYNC2	C14	PAR1	U24
LINERXSYNC8	J2	LINETXCLK20	H25	LINETXSYNC3	A15	PHASEDETDOWN	U22
LINERXSYNC9	H4	LINETXCLK21	J26	LINETXSYNC4	B16	PHASEDETUP	V22
LINERXSYNC10	H3	LINETXCLK22	K24	LINETXSYNC5	B17	PMRST	T25
LINERXSYNC11	G1	LINETXCLK23	L24	LINETXSYNC6	B18	RCBCLK	E17
LINERXSYNC12	F2	LINETXCLK24	M24	LINETXSYNC7	D19	RCBDATA	E15
LINERXSYNC13	E4	LINETXCLK25	M23	LINETXSYNC8	C19	RCBSYNC	E18
LINERXSYNC14	D1	LINETXCLK26	N25	LINETXSYNC9	A20	RDLCLK	E19
LINERXSYNC15	C1	LINETXCLK27	P25	LINETXSYNC10	B21	RDLDATA	H22
LINERXSYNC16	K5	LINETXCLK28	R23	LINETXSYNC11	D22	REF10	AC11
LINERXSYNC17	E6	LINETXCLK29	R24	LINETXSYNC12	A23	REF14	AD12
LINERXSYNC18	B3	LINETXDATA1	A14	LINETXSYNC13	A24	RESHI	AF12
LINERXSYNC19	B4	LINETXDATA2	B15	LINETXSYNC14	F22	RESLO	AE12
LINERXSYNC20	B5	LINETXDATA3	D16	LINETXSYNC15	C25	RHSCN	AD8
LINERXSYNC21	D6	LINETXDATA4	D17	LINETXSYNC16	D25	RHSCP	AC7
LINERXSYNC22	B7	LINETXDATA5	D18	LINETXSYNC17	E25	RHSDN	AE7
LINERXSYNC23	A8	LINETXDATA6	C18	LINETXSYNC18	F23	RHSDP	AF7
LINERXSYNC24	C9	LINETXDATA7	A19	LINETXSYNC19	G25	RHSFSYN CN	AD7
LINERXSYNC25	D9	LINETXDATA8	B20	LINETXSYNC20	H26	RLSC52	AC2
LINERXSYNC26	D10	LINETXDATA9	D21	LINETXSYNC21	J24	RLSCLK	V4
LINERXSYNC27	D11	LINETXDATA10	B22	LINETXSYNC22	J23	RLSDATA0	U3
LINERXSYNC28	B12	LINETXDATA11	B23	LINETXSYNC23	K23	RLSDATA1	U2
LINERXSYNC29	A13	LINETXDATA12	B24	LINETXSYNC24	L23	RLSDATA2	U4
LINETXCLK1	B14	LINETXDATA13	E21	LINETXSYNC25	M25	RLSDATA3	T3
LINETXCLK2	D15	LINETXDATA14	C26	LINETXSYNC26	N26	RLSDATA4	T2
LINETXCLK3	C15	LINETXDATA15	D26	LINETXSYNC27	P23	RLSDATA5	T4
LINETXCLK4	C16	LINETXDATA16	E23	LINETXSYNC28	P24	RLSDATA6	R3
LINETXCLK5	C17	LINETXDATA17	F25	LINETXSYNC29	R26	RLSDATA7	R1
LINETXCLK6	A18	LINETXDATA18	G26	LOPOHCLKIN	AC13	RLSJ0J1V1	V3

Table 2-2. Pin Assignments for 456-Pin PBGA by Signal Name (continued)

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
RLSPAR	V2	TLSPAR	AA3	VDD	AB11	VSS	N12
RLSSPE	V1	TLSSPE	AB2	VDD	AB16	VSS	N13
RLSSYNC52	AC1	TLSSYNC52	AD2	VDD	AB22	VSS	N14
RLSV1	W4	TLSV1	AB3	VDD	AB26	VSS	N15
RPOACCLK	AE3	TMSN	W5	VDD	AF1	VSS	N16
RPOACDATA	AD4	TPOACCLK	AE4	VDD	AF5	VSS	P11
RPOACSYNC	AF4	TPOACDATA	AD5	VDD	AF10	VSS	P12
RPSC155N	AD11	TPOACSYNC	AC5	VDD	AF17	VSS	P13
RPSC155P	AC10	TPSC155N	AD13	VDD	AF22	VSS	P14
RPSD155N	AE10	TPSC155P	AC12	VDD	AF26	VSS	P15
RPSD155P	AD10	TPSD155N	AE13	VDDA_CDR	AC9	VSS	P16
RSTN	T24	TPSD155P	AF13	VDDD_PLL	AD22	VSS	R11
RTOACCLK	AD1	TRSTN	AB8	VDDS_PLL	AE23	VSS	R12
RTOACDATA	AD3	TSTMODE	AF15	VSS	A2	VSS	R13
RTOACSYNC	AA5	TSTMUX0	AC16	VSS	A6	VSS	R14
RWN	AF18	TSTMUX1	AE16	VSS	A11	VSS	R15
RXDATAEN	AB19	TSTPHASE	AF14	VSS	A16	VSS	R16
SCAN_EN	N5	TSTSFTLD	AD15	VSS	A21	VSS	T1
SCAN_MODE	M5	TTOACCLK	AB6	VSS	A25	VSS	T11
TCBCLK	E13	TTOACDATA	AE2	VSS	B1	VSS	T12
TCBDATA	E12	TTOACSYNC	AF3	VSS	B26	VSS	T13
TCBSYNC	E14	TXDATAEN	W22	VSS	D4	VSS	T14
TCK	R5	VDD	A1	VSS	D23	VSS	T15
TDI	U5	VDD	A5	VSS	E7	VSS	T16
TDLCLK	E9	VDD	A10	VSS	E20	VSS	T26
TDLDATA	E8	VDD	A17	VSS	F1	VSS	Y5
TDO	V5	VDD	A22	VSS	F26	VSS	Y22
THSCN	AE8	VDD	A26	VSS	G5	VSS	AA1
THSCP	AF8	VDD	E1	VSS	G22	VSS	AA26
THSDN	AE9	VDD	E5	VSS	L1	VSS	AB7
THSDP	AF9	VDD	E11	VSS	L11	VSS	AB20
THSSYNCN	AD9	VDD	E16	VSS	L12	VSS	AC4
THSSYNCP	AC8	VDD	E22	VSS	L13	VSS	AC23
TLSC52	AC3	VDD	E26	VSS	L14	VSS	AE1
TLSCLK	AA2	VDD	K1	VSS	L15	VSS	AE26
TLSDATA0	AA4	VDD	K26	VSS	L16	VSS	AF2
TLSDATA1	Y3	VDD	L5	VSS	L26	VSS	AF6
TLSDATA2	Y1	VDD	L22	VSS	M11	VSS	AF11
TLSDATA3	Y2	VDD	T5	VSS	M12	VSS	AF16
TLSDATA4	Y4	VDD	T22	VSS	M13	VSS	AF21
TLSDATA5	W3	VDD	U1	VSS	M14	VSS	AF25
TLSDATA6	W1	VDD	U26	VSS	M15	VSSA_CDR	AB12
TLSDATA7	W2	VDD	AB1	VSS	M16	VSSA_PLL	AF23
TLSJ0J1V1	AB4	VDD	AB5	VSS	N11	VSSS_PLL	AD23

2.4 Pin Descriptions

2.4.1 High-Speed I/O Pin Descriptions

The high-speed I/O consists of five LVDS signals (10 pins) that connect the *Supermapper* to an external OC-3 optoelectronic device. It exchanges an STS-3 or STM-1 signal between the TMUX and an OC-3 transceiver. The *Supermapper* is capable of recovering a clock from the receive data, or it can accept a clock recovered externally by the optoelectronic device. If internal clock recovery is used, the *Supermapper* uses THSCP/N as a reference.

The high-speed I/O may also run at 51.84 Mb/s in applications that terminate an STS-1 or EC-1 signal. In this case, the (electrical) line signals are typically terminated by a line interface unit (LIU) chip. The operating speed of the high-speed I/O is determined by bit TMUX_STS1MODE in register TMUX_RCV_TX_MODE.

Table 2-3. High-Speed I/O Pin Descriptions

Pin	Symbol	Type	I/O	Description
AF7, AE7	RHSDP RHSDN	LVDS	I	Receive High-Speed Data. 155.52 Mb/s serial data input in STS-3 or STM-1 format, or 51.84 Mb/s data in STS-1 format. If RHSD is not used (in a slave <i>Supermapper</i> , for example), the P input should be pulled high through a 1 k Ω resistor and the N input pulled low through a 1 k Ω resistor. RHSD is typically provided by an OC-3 transceiver, an STS-1 line interface unit, or a higher-order (e.g., STS-12) demultiplexing chip.
AC7, AD8	RHSCP RHSCN	LVDS	I	Receive High-Speed Clock. 155.52 MHz or 51.84 MHz clock for STS-3 or STS-1 input data. Typically supplied by an external OC-3 optoelectronic device, or an STS-1/EC-1 line interface unit, synchronous with RHSD. If the internal clock recovery (CDR) feature is enabled, RHSC is not required and should be connected to a 1 k Ω resistor to VDD (RHSCP input) and VSS (RHSCN input).
AF8, AE8	THSCP THSCN	LVDS	I	Transmit High-Speed Clock. Transmit 155.52 MHz or 51.84 MHz clock. Master clock for the transmit sections of the TMUX, telecom bus, SPE, and VT mappers. THSC is also used as a reference clock for the receive CDR, if it is being used. Note: A 155 MHz THSC is required when using the CDR in 51 Mb/s mode.
AC8, AD9	THSSYNCP THSSYNCN	LVDS	I	Transmit High-Speed Frame Synchronization. An optional input that may be used to specify the position of the transmit STS-3, STM-1, or STS-1 frame. THSSYNC marks the position of bit 1 of the A1 byte, i.e., the first bit of the overhead in the THSD output. If THSSYNC is not used, the P input should be pulled high through a 1 k Ω resistor, and the N input pulled low through a 1 k Ω resistor. A typical application for this pin may be to synchronize a group of <i>Supermappers</i> so that their STS-3 outputs may be multiplexed into an STS-12 signal.
AF9, AE9	THSDP THSDN	LVDS	O	Transmit High-Speed Data. Transmit output for STS-3, STM-1, or STS-1 serial data. Typically connected to an OC-3 transceiver or an LIU, if operating in STS-1 mode. May also be connected to a higher-order multiplexing device, for example, STS-12.

2.4.2 Protection Switch I/O Pin Description

The protection switch I/O provides additional copies of the high-speed interface signals so that various protection schemes may be implemented. The protection interface may be used when the high-speed interface is operating in both STS-3 and STS-1 modes. If the protection port is not used, the input clock and data may be left unconnected, or tied to power (P inputs) or ground (N inputs) through 1 k Ω resistors. Unused protection outputs should be left unconnected.

Table 2-4. Protection Switch I/O Pin Description

Pin	Symbol	Type	I/O	Description
AD10, AE10	RPSD155P RPSD155N	LVDS	I	Receive Protection Data. Receive side high-speed serial data input from protection board.
AC10, AD11	RPSC155P RPSC155N	LVDS	I	Receive Protection Clock. Receive side high-speed clock input from protection board.
AF13, AE13	TPSD155P TPSD155N	LVDS	O	Transmit Protection Data. Transmit side high-speed serial data output to protection board.
AC12, AD13	TPSC155P TPSC155N	LVDS	O	Transmit Protection Clock. Transmit side high-speed clock output to protection board.

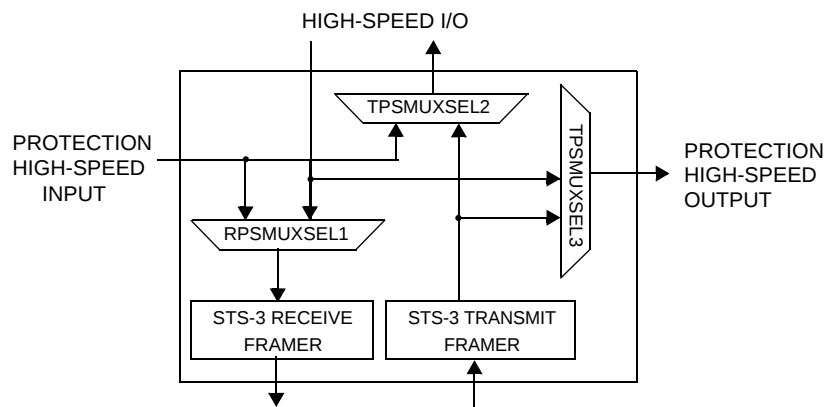


Figure 2-2. Protection Switch

2.4.3 Telecom Bus (Low-Speed I/O) Pin Description

The telecom bus on the *Supermapper* is used for interconnecting STS-1 signals. It has two 8-bit data buses, one for upstream data and one for downstream data, plus clock and frame indication signals for each bus. The telecom bus can operate at 19.44 MHz (space for three STS-1 signals) or 6.48 MHz (space for 1 STS-1 signal).

Supermappers in OC-3 applications are typically connected using the telecom bus, and the bus is configured to operate at 19.44 MHz.

Table 2-5. Telecom Bus (Low-Speed I/O) Pin Description

Pin	Symbol	Type	I/O	Description
R1, R3, T4, T2, T3, U4, U2, U3	RLSDATA[7:0]	LVC MOS	I/O	Receive Low-Speed Data [7:0], Parallel Data Bus. Used to connect the downstream STS-1 signals from the master to the slave devices. In master mode, RLSDATA is an output bus, 8 bits wide. It contains all the received data for distribution to the two slave devices. Connect to RLSDATA[7:0] on the slave devices. In slave mode, these pins are inputs and should be connected to the RLSDATA[7:0] outputs on the master. RLSDATA contains three byte-interleaved STS-1 time slots. The slot used by each SPE mapper in the slaves and the master device is determined by programming the SPE_RSTS3TMSLOT register bits.
V4	RLSCLK	LVC MOS	I/O	Receive Low-Speed Clock. This is a 19.44 MHz or 6.48 MHz clock for the receive low-speed data bits. In master mode, this is a 19.44 MHz output clock for distribution to the two slave devices. Connect to RLSCLK on the slaves, RLSCLK is an input signal on slave devices. RLSC52, RLSSYNC52, and RLSCLK must come from the same clocking source. Note: As outputs, these pins have 6 mA drive capability.
V2	RLSPAR	LVC MOS	I/O	Receive Low-Speed Parity. Receive data parity bit, may be configured for odd or even parity generated on RLSDATA[7:0]. The default is odd parity; it may be set to even by setting bit 2 of the register 0x4001B. An output in master mode and an input in slave mode. Connect the RLSPAR (output) on the master to the RLSPAR (input) pins on the slaves.
V1	RLSSPE	LVC MOS	I/O	Receive Low-Speed SPE Marker. Receive synchronous payload envelope timing indicator. It is high while there is SPE data on the RLSDATA[7:0] output bus (master mode). Connect to RLSSPE on the slaves. RLSSPE is an input on slave devices.
V3	RLSJ0J1V1	LVC MOS	I/O	Receive Low-Speed J0/J1/V1 Marker. On the master device, this is an output that is high while J0-1, J1 (1, 2, and 3), and V1 (1, 2, and 3) bytes are present on the RLSDATA bus. Connect to RLSJ0J1V1 on the slaves, which is an input.
W4	RLSV1	LVC MOS	I/O	Receive Low-Speed V1 Marker. Receive V1 timing indicator. On the master, this is an output that is high while the V1 bytes (1, 2, and 3) are present on RLSDATA[7:0] output bus. Connect to RLSV1 on the slaves. It is high every VT multiframe (superframe). Connect to RLSV1 (input) on the slaves.
W2, W1, W3, Y4, Y2, Y1, Y3, AA4	TLSDATA[7:0]	LVC MOS	I/O	Transmit Low-Speed Data [7:0]. This parallel data bus is used to connect the upstream STS-1 signals from the slave devices to the master device. In master mode, TLSDATA is an 8 bit wide input bus and contains all the transmit STS-1 data from the slave devices. In slave mode, these pins are outputs and should be connected to the TLSDATA[7:0] inputs on the master. TLSDATA contains three byte-interleaved STS-1 time slots. The slot used by each SPE mapper in the slaves and the master device is determined by programming the SPE_TSTS3TMSLOT register bits.
AA2	TLSCLK	LVC MOS	I/O	Transmit Low-Speed Clock. This is a 19.44 MHz or 6.48 MHz clock for the TLSDATA[7:0] bits. TLSCLK is an output on a master <i>Super-mapper</i> and an input on a slave. TLSC52, TLSSYNC52, and TLSCLK must come from the same clocking source, (should be connected together between master and slave devices). Note: As outputs, these pins have 6 mA drive capability.

Table 2-5. Telecom Bus (Low-Speed I/O) Pin Description (continued)

Pin	Symbol	Type	I/O	Description
AA3	TLSPAR	LVC MOS	I/O	Transmit Low-Speed Parity. This parity bit is generated on the TLSDATA[7:0] . This is an output from the slave device and input to the master device. May be configured for odd or even parity generation and checking.
AB2	TLSSPE	LVC MOS	I/O	Transmit Low-Speed SPE Marker. . High while the STS-1 payloads are present on the TLSDATA[7:0] bus. Low while the STS-1 overhead is present on the TLSDATA[7:0] bus. An output from the master and input on the slaves. (Should be connected between master and slave devices)
AB4	TLSJ0J1V1	LVC MOS	I/O	Transmit Low-Speed J0/J1/V1 Marker. Transmit J0, J1, or V1 timing indicator. High while the J0, J1, or V1 bits are present on the TLSDATA[7:0] bus. An output on the master and input on slaves.
AB3	TL SV1	LVC MOS	I/O	Transmit Low-Speed V1 Marker. Transmit V1 timing indicator. High while the V1 bits are present on the TLSDATA[7:0] bus. An output on the master and input on slaves. The V1 position is fixed from the maser device. It is high every VT multiframe (superframe). (Should be connected between master and slave devices).
AC2	RLSC52	LVC MOS	I/O	Receive Low-Speed Clock. This is an output on the master and an input on the slave. This is synchronous to the 51.84 MHz clock. This clock is used by SPEMPR and VTMPR internally. (Should be connected between master and slave devices). Note: As outputs, these pins have 6 mA drive capability.
AC1	RLSSYNC52	LVC MOS	I/O	Receive Low-Speed Sync. This is an output on the master and an input on the slave. This is synchronous to the 51.84 MHz clock. This clock is used by SPEMPR and VTMPR internally. (Should be connected between master and slave devices).
AC3	TLSC52	LVC MOS	I/O	Transmit Low-Speed Clock. This is an output on the master and an input on the slave. This is synchronous to the 51.84 MHz clock. (Should be connected between master and slave devices). Note: TLSC52 can be used as the master clock for the DS1/E1 framer, see register 0x00012. In this case, this clock should be provided even if the TMUX, SPE and/or VT mappers are not used.
AD2	TLSSYNC52	LVC MOS	I/O	Transmit Low-Speed Sync. This is an output on the master and an input on the slave. This is synchronous to the 51.84 MHz clock. Should be connected between master and slave devices).

2.4.4 TOAC and POAC

The transport and path overhead access channels (TOAC and POAC) allow parts of the SONET/SDH overhead to be examined externally (receive direction) or overwritten (transmit direction) through serial data ports. Each port has clock and data lines and a synchronization signal that marks the last bit of the frame so that the rest of the overhead bytes can be identified.

The receive TOAC and POAC channels contain all of the respective overheads bytes. The transmit channels contain space for all the overhead bytes, but whether they are actually transmitted depends on how the device is programmed. Some overhead bytes cannot be modified; some may be modified only through the CPU port; some may be modified only through the overhead access channels; and some may be modified either through the CPU port, or through the overhead access channels.

Table 2-6. TOAC and POAC

Pin	Symbol	Type	I/O	Description
Transmit Overhead Access Channel (TOAC)				
AD1	RTOACCLK	LVC MOS	O	Receive TOAC Clock. Receive side serial access channel clock output for the transport overhead bytes.
AD3	RTOACDATA	LVC MOS	O	Receive TOAC Data. Receive side serial access channel data output for the transport overhead bytes.
AA5	RTOACSYNC	LVC MOS	O	Receive TOAC Synchronization. Receive side sync output for TOAC channel. Active-high during the LSB of the last byte.
AB6	TTOACCLK	LVC MOS	O	Transmit TOAC Clock. Transmit side serial access channel clock output for the transport overhead bytes.
AE2	TTOACDATA	LVC MOS	I Pull-down	Transmit TOAC Data. Transmit side serial access channel data input for the transport overhead bytes.
AF3	TTOACSYNC	LVC MOS	O	Transmit TOAC Synchronization. Transmit side sync output for TOAC channel. Active-high during the LSB of the last byte.
Path Overhead Access Channel (POAC)				
AE3	RPOACCLK	LVC MOS	O	Receive POAC Clock. Receive side serial access channel clock output for the path overhead bytes.
AD4	RPOACDATA	LVC MOS	O	Receive POAC Data. Receive side serial access channel data output for the path overhead bytes.
AF4	RPOACSYNC	LVC MOS	O	Receive POAC Synchronization. Receive side sync output for POAC channel. Active-high during the last bit of the last byte of the POAC frame.
AE4	TPOACCLK	LVC MOS	O	Transmit POAC Clock. Transmit side serial access channel clock output for the path overhead bytes.
AD5	TPOACDATA	LVC MOS	I Pull-down	Transmit POAC Data. Transmit side serial access channel data input for the path overhead bytes.
AC5	TPOACSYNC	LVC MOS	O	Transmit POAC Synchronization. Transmit side sync output for POAC channel. Active-high during the last bit of the last byte.

2.4.5 Miscellaneous Signals

Table 2-7. Miscellaneous Signals

Pin	Symbol	Type	I/O	Description
AE5	LOSEXT	LVC MOS	I Pull-up	Loss of Signal External. External loss of signal input. If external clock and data recovery is used on the high-speed I/O port, it may be connected to this input, which can be configured to assert the LOS register bit normally associated with the internal LOS detection in the internal CDR block. The polarity of LOS may be programmed active-high or low; see register TMUX_RHS_CTL, bit TMUX_LOSEXT_LEVEL.
AD6, AE6, AC6	AUTO_AIS	LVC MOS	I/O	AIS Enable [3:1]. Control signal for automatic AIS insertion on each STS1. The STS-1 AIS is applied downstream on the telecom bus, i.e., it is an output from masters and an input to slaves. If the <i>Supermapper</i> is configured as a master, then there is no need to do anything as the AUTO_AIS is an output. If the <i>Supermapper</i> is configured as a slave (i.e., if the TMUX is not used), then those slave devices should have their AUTO_AIS pulled down to ground. For STS-3 applications where there are three <i>Supermappers</i> , the AUTO_AIS should be connected appropriately between master and slave devices. For STS-1 applications where there is one <i>Supermapper</i> in master mode, the AUTO_AIS should be unconnected. For STS-1 applications where one <i>Supermapper</i> is in slave mode, the AUTO_AIS should be pulled low.
AD7	RHSFSYNCN	LVC MOS	O	Receive High-Speed Frame Synchronization. Receive side frame sync output indicating the frame location of the high-speed data input. May be used as an 8 kHz timing reference for network synchronization to the receive high-speed data input (STS-3 or STS-1).

2.4.6 DS3 Port

If a DS3 output is required in a *Supermapper* application and the DS3 signal has been recovered (demapped) from an STS-1, then it is necessary to smooth the DS3 recovered clock. The DS3 clock extracted from the STS-1 clock will have considerable jitter introduced when the SONET overhead is removed and pointer adjustments are made. A phase-locked loop is recommended for this purpose. The *Supermapper* contains a phase comparator that can be used in conjunction with an external low-pass filter and voltage-controlled crystal oscillator to implement the PLL.

Table 2-8. DS3 Port

Pin	Symbol	Type	I/O	Description
V22	PHASEDETUP	LVC MOS	O	Phase Detector Up. Phase error signal out to external filter and VCXO. This output will generate an error signal when the VCXO output is slower than the reference signal.
U22	PHASEDETDOWN	LVC MOS	O	Phase Detector Down. Phase error signal out to external filter and VCXO. This output will generate an error signal when the VCXO output is faster than the reference signal.
R22	DS3POSDATAOUT	LVC MOS	O	Positive Data Output. Serial DS3 positive data out to LIU when the DS3 output port is operating in dual-rail mode. Nonreturn-to-zero DS3 data output when the DS3 output is operating in single-ended mode.
P22	DS3NEGDATAOUT	LVC MOS	O	Negative Data Output. Serial DS3 negative data output to LIU when the DS3 port is operating in dual-rail mode. In single-rail mode, this output is not used and may be left unconnected.
N22	DS3DATAOUTCLK	LVC MOS	I Pull-down	DS3 Data Out Clock. 44.736 MHz DS3 clock input. If the <i>Supermapper</i> is being used to map DS3 data to and from STS-1, then this clock should be supplied by the external VCXO that is associated with the DS3 clock recovery PLL. In other DS3 modes (e.g., M13), this input will be supplied by an external crystal oscillator.
M22	DS3POSDATAIN	LVC MOS	I Pull-down	Positive Data Input. If the DS3 port is configured in dual-rail mode, then this input is serial positive data from an external DS3 LIU. If the DS3 port is configured in single-rail mode, then this input is serial nonreturn-to-zero data from the external LIU.
K22	DS3NEGDATAIN	LVC MOS	I Pull-down	Negative Data In. In dual-rail mode, this is negative data from an external DS3 LIU. In single-rail mode, it may be connected to the bipolar violation output of the external DS3 LIU, left unconnected, or tied to ground.
J22	DS3DATAINCLK	LVC MOS	I Pull-down	DS3 Data In Clock. This is a 44.736 MHz clock input from the clock recovery in the external DS3 LIU.

Table 2-9. DS3 Port C-Bit and Datalink Access

Pin	Symbol	Type	I/O	Description
E14	TCBSYNC	LVC MOS	O	Transmit C-Bit Sync. In the C-bit parity mode, 10 C-bits may optionally be input for multiplexing into the transmit DS3 frame through the TCBDATA input. The TCBSYNC output is low, except during the rising edge of TCBCLK that is used to input C2.
E13	TCBCLK	LVC MOS	O	Transmit C-Bit Clock. A gapped clock (nominally 93.983 kHz) for accepting selected C-bits on input M13_CBDATA.
E12	TCBDATA	LVC MOS	I Pull-down	Transmit C-Bit Data. In the C-bit parity mode, the network requirements bit (C2) and the unused C-bits (C4, C5, C6, C16, C17, C18, C19, C20, and C21) may optionally be input for multiplexing into the transmit DS3 frame through this input.
E9	TDLCLK	LVC MOS	O	Transmit Data Link Clock. A gapped clock (nominally 28.195 kHz) for accepting path maintenance data link C-bits on input TDLDATA.
E8	TDLDATA	LVC MOS	I Pull-down	Transmit Data Link Data. The path maintenance data link C-bits (C13, C14, and C15) may optionally be input for multiplexing into the transmit DS3 frame through this input.

Table 2-10. M13 Multiplexer/Demultiplexer Receive Section

Pin	Symbol	Type	I/O	Description
E18	RCBSYNC	LVC MOS	O	Receive C-Bit Sync. Ten C-bits are output on RCBDATA after they are demultiplexed from the received DS3 signal. The RCBSYNC output is low, except during the rising edge of RCBDATA that is used to output C2.
E17	RCBCLK	LVC MOS	O	Receive C-Bit Clock. A gapped clock (nominally 93.983 kHz) for outputting selected C-bits on RCBDATA.
E15	RCBDATA	LVC MOS	O	Receive C-Bit Data. The received network requirements bit (C2) and the received unused C-bits (C4, C5, C6, C16, C17, C18, C19, C20, and C21) are output after they are demultiplexed from the received DS3 signal.
E19	RDLCLK	LVC MOS	O	Receive Data Link Clock. A gapped clock (nominally 28.195 kHz) for outputting path maintenance data link C-bits on RDLDATA.
H22	RDLDATA	LVC MOS	O	Receive Data Link Data. The received path maintenance data link C-bits (C13, C14, and C15) that are demultiplexed from the received DS3 signal.

Reference clocks, used internally in the jitter attenuation and AIS generation processes are defined. Note that these are typically supplied by free-running crystal oscillators.

Table 2-11. Reference Clocks

Pin	Symbol	Type	I/O	Description
AC17	E1XCLK	LVC MOS	I Pull-down	E1 X Clock. This clock signal is used by the E1 test pattern generator (i.e., to generate E1 AIS (all 1s), as a reference to the E1 DJA, and as a clock source for the E1 test pattern generator and test pattern monitor. This input may be provided by a 2.048 MHz, a 32.768 MHz, or a 65.536 MHz $\pm$ 50 ppm free-running crystal oscillator, or clocking chip. For the E1 DJA, an input of 32.768 MHz or 65.536 MHz must be used.
AD16	DS1XCLK	LVC MOS	I Pull-down	DS1 X Clock. This clock signal is used for three purposes: to generate DS1 AIS (all 1s), as a reference to the DS1 DJA, and as a clock source for the DS1 test pattern generator and test pattern monitor. This input may be provided by a 1.544 MHz, a 24.704 MHz, or a 49.408 MHz $\pm$ 32 ppm free-running crystal oscillator, or clocking chip. For the DS1 DJA, an input of 24.704 MHz or 49.408 MHz must be used.
E10	DS2AISCLK	LVC MOS	I Pull-down	DS2 AIS Clock. See separate DS2/E2 application note for use in DS2 mode. VC11 AIS Clock. A 1.664 MHz clock input. In the VT mapper mode, this clock is used to generate VC11 AIS. The clock is used when VC11 is sent from the LINETXDATA[30:1] outputs. The 1.664 MHz clock is for a VC11 payload. There are 27 bytes per VT1.5 in each STS-1 frame, excluding the VT overhead (1 byte), 26 bytes/125 μ s = 1.664 Mbits/s. (VC11 rate is 1.728 Mbits/s.) If used, this input can be provided by a free-running crystal oscillator, or a clocking chip.

2.4.7 Low-Order Path Overhead Access Channel

Each VT has a low-order path overhead, and this interface allows access to all LOPOH bits for all VTs. Note that the purpose of doing this is slightly different from the transport and path overhead access. These are used to cross couple the bits between links in a protection scheme, rather than provide access for examination or modification of the overhead, although that is possible too.

Table 2-12. Low-Order Path Overhead Access Channel

Pin	Symbol	Type	I/O	Description
Transmit Direction				
AC13	LOPOHCLKIN	LVC MOS	I Pull-down	Low-Order Path Overhead Clock. 6.48 MHz clock supplied from external circuits that provide the low-order path overhead data.
AC14	LOPOHDATAIN	LVC MOS	I Pull-down	Low-Order Path Overhead Data. The following parts of the low-order (VT) overhead are presented at this pin: communication channel bits (O bits), V5, J2, Z6/N2, Z7, and K4 byte.
AB14	LOPOHVALIDIN	LVC MOS	I Pull-down	Low-Order Path Overhead Data Input Valid. This signal is a mask that indicates the location of the overhead bytes in LOPOHDATAIN.
Receive Direction				
AB15	LOPOHCLKOUT	LVC MOS	O	Low-Order Path Overhead Clock. 6.48 MHz clock supplied to external circuits that receive the low-order path overhead data.
AB17	LOPOHDATAOUT	LVC MOS	O	Low-Order Path Overhead Data. Line and path REI, RDI, O bits, V5, J2, Z6/N2, and Z7/K4 byte.
AB18	LOPOHVALIDOUT	LVC MOS	O	Low-Order Path Overhead Data Output Valid. This signal is a mask that indicates the location of the overhead bytes in LOPOHDATAOUT.

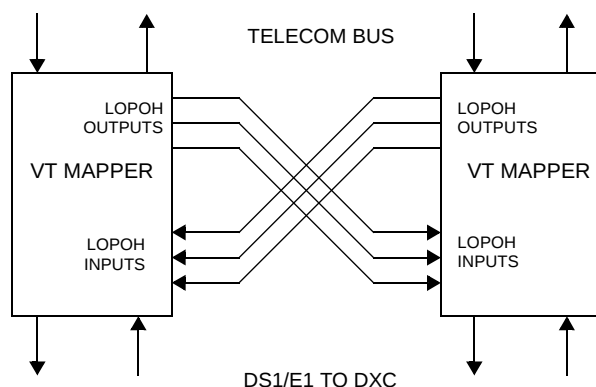


Figure 2-3. DS1/E1 to DXC Block Diagram

Table 2-13. Multifunction System Interface

Pin	Symbol	Type	I/O	Description
C13, A12, B11, B10, B9, D8, C8, A7, B6, D5, A4, A3, H5, F5, C2, D2, E2, F4, G2, H1, J3, J4, K4, L4, M2, N1, P4, P3	LINERXDATA[28:1]	LVC MOS	I Pull-down	Line Receive Data [28:1]. Configurable inputs to the internal cross connect. The use depends on the application. Generally, these inputs are used for the received positive-rail or single-rail DS1/E1 line data input. If operating in dual-rail mode, the negative rail will be expected on LINERXSYNC[28:1]. Using dual-rail mode implies that the internal B8ZS or HDB3 decoders are enabled, and line code violations can be detected and counted inside the <i>Supermapper</i>. These data inputs may be assigned, using the cross connect block, to the DS1 or E1 inputs on the VT mapper, M13 or DS1/E1 framers. It is also possible to use the inputs for DS2 data, in which case they may be assigned to the M23 multiplexer inputs.
D13	LINERXDATA29	LVC MOS	I Pull-down	Receive Data 29. Configurable input to the internal cross connect. May be used as an additional line receive data input, for a protection channel. Other possible uses are as follows: Global transmit line clock input. Externally supplied 1.544 MHz or 2.048 MHz low jitter clock phase-locked to the TDM system clock. Used for transmit line clock on the DS1/E1 framer. This is not normally used because the DS1/E1 framer has a PLL that can generate a 1.544 MHz/2.048 MHz clock from the TDM system clock (CHI clock). This applies in PSB and CHI modes. Receive data input. If NSMI mode is used, this will be a 51.84 Mbits/s serial data input.
D12, C12, C11, C10, A9, B8, D7, C7, C6, C5, C4, C3, J5, B2, D3, E3, F3, G3, G4, H2, J1, K3, L3, M3, M4, N2, P2, R4	LINERXCLK[28:1]	LVC MOS	I/O Pull-down	Receive Clock [28:1]. Configurable inputs/outputs to the internal cross connect. Typically a line clock associated with the corresponding LINERXDATA input. It can therefore be running at DS1, E1, or DS2 rate. The cross connect is used to assign these inputs to the VT mapper, M13, or DS1/E1 framer.
B13	LINERXCLK29	LVC MOS	I/O Pull-down	Receive Clock 29. May be used as additional receive clock input for a DS1/E1 protection channel. Also has special use as a master clock. In CHI mode, it is the receive clock input (2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz). In PSB mode, it is the receive clock input (19.44 MHz). In NSMI mode, it is the receive clock input (51.84 MHz).

Table 2-13. Multifunction System Interface (continued)

Pin	Symbol	Type	I/O	Description
B12, D11, D10, D9, C9, A8, B7, D6, B5, B4, B3, E6, K5, C1, D1, E4, F2, G1, H3, H4, J2, K2, L2, M1, N3, N4, P1, R2	LINERXSYNC[28:1]	LVC MOS	I	Line Receive Synchronous[28:1]. Multifunction input. Channel assignment may be configured through the internal cross connect. Can be used as the negative rail of a DS1/E1 signal in conjunction with LINERXDATA[28:1], when operating in dual-rail mode. In CHI mode, these inputs are used for receive TDM highways that may run at 2.048, 4.096, or 8.192 Mbits/s. In parallel system bus mode, the receive system data bus inputs are assigned to LINERXSYNC 16:1. The PSB is a 16-bit wide bus that operates at 19.44 MHz.
A13	LINERXSYNC29	LVC MOS	I/O	Line Receive Synchronous 29. Multifunction input. Channel assignment may be configured through the internal cross connect. Can be used as the negative rail of a DS1/E1 signal in conjunction with LINERXDATA 29, when operating in dual-rail mode. In CHI and PSB modes, this input is used as the receive system frame synchronization input. In NSMI mode, it is the receive control input .
R25, P26, N23, N24, M26, L25, K25, J25, H23, H24, G26, F25, E23, D26, C26, E21, B24, B23, B22, D21, B20, A19, C18, D18, D17, D16, B15, A14	LINETXDATA[28:1]	LVC MOS	I/O	Line Transmit Data [28:1] Configurable outputs from the internal cross connect. Used for transmit positive-rail or single-rail DS1/E1 line data outputs. May be connected to the DS1/E1 outputs from the VT mapper, M13 MUX, or DS1/E1 framer line outputs. May also be used as DS2 outputs.
T23	LINETXDATA29	LVC MOS	O	Line Transmit Data 29. Configurable output from the internal cross connect. An extra DS1 or E1 transmit port that may be used for protection or as a timing reference output. In NSMI mode, it will be a serial data output (51.84 Mbits/s).
R23, P25, N25, M23, M24, L24, K24, J26, H25, G23, G24, F24, E24, D24, C24, B25, C23, C22, C21, C20, D20, B19, A18, C17, C16, C15, D15, B14	LINETXCLK[28:1]	LVC MOS	I/O	Line Transmit Clock [28:1]. Configurable outputs from the internal cross connect. Can be used as the clock signals for LINETXDATA[28:1] in DS1, E1, and DS2 modes.
R24	LINETXCLK29	LVC MOS	I/O	Line Transmit Clock 29. Configurable output to the internal cross connect for the protection or timing reference channel. Also used as the transmit global system clock input for CHI (2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz), PSB (19.44 MHz). In NSMI mode, it will be an output (51.84 MHz).

Table 2-13. Multifunction System Interface (continued)

Pin	Symbol	Type	I/O	Description
P24, P23, N26, M25, L23, K23, J23, J24, H26, G25, F23, E25, D25, C25, F22, A24, A23, D22, B21, A20, C19, D19, B18, B17, B16, A15, C14, D14	LINETXSYNC[28:1]	LVC MOS	I/O	Line Transmit Synchronous [28:1]. Configurable inputs/outputs to the internal cross connect. An output when used as the negative rail of a DS1 or E1 output port operating in dual-rail mode. In CHI mode, these pins may be used as output TDM highways. In PSB mode, bits 16:1 are used for the transmit data bus, and bits 28:17 are not used. These pins may also be used as DS2 I/O to/from the M12 block as follows: 7:1—Tx data out. 14:8—Tx clock in. 21:16—Rx data in. 28:22—Rx clock in.
R26	LINETXSYNC29	LVC MOS	I/O	Line Transmit Synchronous 29. Configurable input/output to the internal cross connect. An output when used as the negative rail of a DS1 or E1 output port operating in dual-rail mode. In CHI and PSB modes, it is used as the transmit system frame synchronization input. In NSMI mode, it is the transmit control output.
AB19	RXDATAEN	LVC MOS	O	NSMI Receive Enable. Receive data enable for NSMI mode. FRM NSMI is not used. M13 NSMI indicates location of OH insertion for DS3 frames
W22	TXDATAEN	LVC MOS	O	NSMI Transmit Enable. Transmit data enable for NSMI mode. FRM NSMI transmit control frame sync. It is used to indicate framer requests for bytes for a particular link. M13 NSMI indicates location of DS3 OH bytes.

2.4.8 Framer PLL

The DS1/E1 framer has a phase-locked loop that may be used to generate a transmit line clock at 1.544 MHz or 2.048 MHz. The reference signal for this PLL may be chosen from a number of possible sources, all typically synchronized to the system clock (CHI transmit/receive clock, for example). In order to ensure reliable performance, this PLL has its own isolated power pins. The PLL also has a number of test control pins that are used for factory testing only.

The PLL is active when framer bit FRM_PLL_BYPAS = 0. When FRM_PLL_BYPAS = 1, the PLL is bypassed and an external clock at the system interface is used as the line clock. An example would be when the framers are programmed for a CHI interface at 2.048 MHz and the frames are programmed for E1, the PLL may be bypassed and the CHI system clock may be used as the line clock.

Table 2-14. Framer PLL

Pin	Symbol	Type	I/O	Description					
AD24	CLKIN_PLL	LVC MOS	I Pull-down	Clock In PLL. Phase locked-loop reference clock input. Frequency should be consistent with the MODE_PLL pins in the PLL Mode1 table below. A 1.544 MHz/2.048 MHz clock for DS1/E1 transmit outputs is generated synchronous to this clock.					
AB21, AE24, AF24	MODE[2:0]_PLL	LVC MOS	I Pull-down	PLL Mode 1. PLL control input 1. The PLL mode inputs should be hardwired to the logic levels shown in the table below, depending on the frequency of the reference supplied to CLKIN_PLL.					
				Mode[2:0]		CLKIN_PLL	Mode[2:0]		CLKIN_PLL
				000		Reserved	100		16.384 MHz
				001		51.84 MHz	101		8.192 MHz
				010		26.62 MHz	110		4.096 MHz
				011		19.44 MHz	111		2.048 MHz

Table 2-15. Microprocessor Interfaces

Pin	Symbol	Type	I/O	Description
AE17	MPCLK	LVC MOS	I	Processor Clock. This is the synchronous microprocessor clock (when MPMODE = 1). The maximum clock frequency is 60 MHz. This clock is required to properly sample address, data, and control signals from the microprocessor in both asynchronous and synchronous modes of operation. This clock must be within the range of 16 MHz—60 MHz.
AD17	MPMODE	LVC MOS	I	Control Port Mode. If the microprocessor interface is synchronous, MPMODE should be high. If the microprocessor interface is asynchronous, MPMODE should be set to 0.
AC18	CSN	LVC MOS	I Pull-up	Chip Select. Active-low chip select. For synchronous mode, it should be stable beyond a certain setup time before the rising clock edge when ADSN is active. For asynchronous mode, it should be stable before DSN is asserted.
AE18	ADSN	LVC MOS	I	Address Strobe. Active-low address strobe that is a 1 MPCLK cycle wide pulse for synchronous mode and active for the entire read/write cycle for asynchronous mode. Address bus signals, ADDR[19:0], are transparently latched into <i>Supermapper</i> when ADSN is low. The address bus should remain valid for the duration of ADSN.
AF18	RWN	LVC MOS	I	Read/Write Cycle Selection. RWN is set high for a read operation, or set low for write operation.
AD18	DSN	LVC MOS	I	Data Strobe. DSN is not used for synchronous mode. For asynchronous mode, write operation, DSN becomes active after data is stable. For read operation, it is similar to ADSN.
AB23, AC26, AC24, AD25, AD26, AE25, AA22, AC22, AE22, AD21, AE21, AC21, AD20, AF20, AE20, AC20, AD19, AF19, AE19, AC19	ADDR[19:0]	LVC MOS	I	Address [19:0]. ADDR19 is the most significant and ADDR0 the least significant bit for addressing all the internal <i>Supermapper</i> registers during CPU access cycles. Note: The <i>Supermapper</i> is little-endian; the least significant byte is stored in the lowest address and the most significant byte is stored in the highest address. Care must be exercised in connection to microprocessors that use big-endian byte ordering.
AB25, AA24, AA25, AA23, Y24, Y26, Y25, Y23, W24, W26, W25, W23, V24, V26, V25, V23	DATA[15:0]	LVC MOS	I/O	Data [15:0]. Data bus for all transfers between the CPU and the internal <i>Supermapper</i> registers. The pins are inputs during write cycles and outputs during read cycles. DATA15 is the MSB, and DATA0 is the LSB.
U24, U25	PAR[1:0]	LVC MOS	I/O	CPU Port Parity [1:0]. Byte-wide parity bits for data. PAR[1] is the parity for DATA[15:8], and PAR[0] is the parity for DATA[7:0].

Table 2-15. Microprocessor Interfaces (continued)

Pin	Symbol	Type	I/O	Description
U23	DTN	LVC MOS	O Open Drain	Data Transfer Acknowledge. In synchronous CPU mode, DTN goes low at the fourth cycle for write or the fifth cycle for read, resulting in a fixed two wait-states for writes and three wait-states for reads. In asynchronous CPU mode, after qualification of ADSN and DSN by the MPCLK clock, DTN goes low for two MPCLK clock cycles for writes and three MPCLK clock cycles for reads. DTN goes high with the rising edge of ASDN.
AB24	INTN	LVC MOS	O Open Drain	Interrupt. <i>Supermapper</i> interrupt request, active-low. This is an open-drain output and should be connected to an external pull-up resistor.
AC25	APS_INTN	LVC MOS	O Open Drain	APS Interrupt. Automatic protection switch interrupt request, active-low. This is an open-drain output and should be connected to an external pull-up resistor.

Table 2-16. General-Purpose Interface

Pin	Symbol	Type	I/O	Description
T24	RSTN	LVC MOS	I Pull-up	Reset. Global reset, active-low. Initializes all internal registers to their default state.
T25	PMRST	LVC MOS	I/O Pull-down	Performance Monitor Reset. May be configured as an input and then used to directly reset all the counters associated with DS1/E1 performance monitoring. If an internal PM reset is used, PMRST is configured as an output that indicates when a PM reset occurred.
R5	TCK	LVC MOS	I	Test Clock. This signal provides timing for the boundary scan and TAP controller. This signal should be static, except during boundary-scan testing.
P5	IDDQ	LVC MOS	I Pull-up	Do not connect.
U5	TDI	LVC MOS	I Pull-up	Test Data In. Data input for the boundary scan; sampled on the rising edge of TCK.
W5	TMSN	LVC MOS	I Pull-up	Test Mode Select (Active-Low). Controls boundary-scan test operations. TMSN is sampled on the rising edge of TCK.
AB8	TRSTN	LVC MOS	I Pull-down	Test Reset (Active-Low). This signal is an asynchronous reset for the TAP controller.
V5	TDO	LVC MOS	O	Test Data Out. Updated on the falling edge of TCK. The TDO output is high impedance, except when scanning out test data.
AB9	IC3STATEN	LVC MOS	I Pull-up	Global Output Enable. All output and bidirectional buffers will be high impedance when this input is low. Normally pulled high internally.

2.4.9 Test Pins

These pins are for factory test purposes only and must be connected properly. They are used to establish special configurations for testing, inserting test data, etc. For normal operation, they should be left unconnected; each is equipped with a pull-up or pull-down to the inactive (normal operation) state.

Table 2-17. Test Pins

Pin	Symbol	Type	I/O	Description
N5	SCAN_EN	LVC MOS	I Pull-down	Test Only. Scan enable (active-high).
M5	SCAN_MODE	LVC MOS	I Pull-down	Test Only. Serial scan input for testing (active-high).
AE14	BYPASS	LVC MOS	I Pull-down	Test Only. Enables functional bypassing of the clock synthesis with a test clock (active-high).
AF14	TSTPHASE	LVC MOS	I Pull-down	Test Only. Controls bypass of 32 PLL-generated phases with 32 low-speed phases, generated by test logic (active-high).
AD14	ECSEL	LVC MOS	I Pull-down	Test Only. Enables external test control of 155 MHz clock phase selection through ETOGGLE and EXDNUP inputs (active-high).
AC15	ETOGGLE	LVC MOS	I Pull-down	Test Only. Moves 155 MHz clock selection one phase per positive pulse > 20 ns. Active + pulse.
AE15	EXDNUP	LVC MOS	I Pull-down	Test Only. Direction of phase changes. 0 = down. 1 = up.
AF15	TSTMODE	LVC MOS	I Pull-down	Test Only. Enables CDR test mode.
AD15	TSTSFTLD	LVC MOS	I Pull-down	Test Only. Enables CDR test mode shift register.
AE16, AC16	TSTMUX[1:0]	LVC MOS	O	Test Only. CDR test mode output.

Table 2-18. LVDS Control Pins

Pin	Symbol	Type	I/O	Description
AF12 AE12	RESHI RESLO	LVC MOS	I	Resistor 1, 2. A 100 Ω 1% resistor should be connected between these two pins as a reference for the LVDS input buffer termination.
AC11	REF10	LVC MOS	I	Voltage Reference 1. 1.0 V reference voltage input.
AD12	REF14	LVC MOS	I	Voltage Reference 2. 1.4 V reference voltage input.
AB10	CTAPRH	LVC MOS	—	Center Tap 1. For RHSD P/N and RHSC P/N. An optional 0.1 μ F capacitor connected between CTAP pin and ground will improve the common-mode rejection of the LVDS input buffers.
AE11	CTAPTH	LVC MOS	—	Center Tap 2. For THSD P/N and THSC P/N. An optional 0.1 μ F capacitor connected between CTAP pin and ground will improve the common-mode rejection of the LVDS input buffers.
AB13	CTAPRP	LVC MOS	—	Center Tap 3. For RPSD155 P/N and RPSC155 P/N. An optional 0.1 μ F capacitor connected between CTAP pin and ground will improve the common-mode rejection of the LVDS input buffers.

Table 2-19. Analog Power and Ground Signals

Pin	Symbol	Type	Name/Description
AC9	VDDA_CDR	—	CDR Power. 3.3 V power supply for the internal CDR. Good engineering practice needs to be applied to minimize noise on this pin.
AB12	VSSA_CDR	—	CDR Ground. Isolated ground for the internal CDR.
AE23	VDDS_PLL	—	Analog VDD for PLL. 3.3 V power supply for the framer's PLL. Good engineering practice needs to be applied.
AF23	VSSA_PLL	—	Analog PLL Ground. Analog ground for PLL.
AD22	VDDD_PLL	—	Digital PLL Power. Digital 3.3 V for PLL. Good engineering practice needs to be applied to minimize noise on this pin.
AD23	VSSS_PLL	—	Digital Ground for PLL. Digital ground for PLL. Good engineering practice needs to be applied.

3 Pin Assignment Matrix

Table 3-1. Pin Matrix

	A	B	C	D	E	F	G	H	J
1	VDD	VSS	LINERXSYNC15	LINERXSYNC14	VDD	VSS	LINERXSYNC11	LINERXDATA9	LINERXCLK8
2	VSS	LINERXCLK15	LINERXDATA14	LINERXDATA13	LINERXDATA12	LINERXSYNC12	LINERXDATA10	LINERXCLK9	LINERXSYNC8
3	LINERXDATA17	LINERXSYNC18	LINERXCLK17	LINERXCLK14	LINERXCLK13	LINERXCLK12	LINERXCLK11	LINERXSYNC10	LINERXDATA8
4	LINERXDATA18	LINERXSYNC19	LINERXCLK18	VSS	LINERXSYNC13	LINERXDATA11	LINERXCLK10	LINERXSYNC9	LINERXDATA7
5	VDD	LINERXSYNC20	LINERXCLK19	LINERXDATA19	VDD	LINERXDATA15	VSS	LINERXDATA16	LINERXCLK16
6	VSS	LINERXDATA20	LINERXCLK20	LINERXSYNC21	LINERXSYNC17	—	—	—	—
7	LINERXDATA21	LINERXSYNC22	LINERXCLK21	LINERXCLK22	VSS	—	—	—	—
8	LINERXSYNC23	LINERXCLK23	LINERXDATA22	LINERXDATA23	TDLDATA	—	—	—	—
9	LINERXCLK24	LINERXDATA24	LINERXSYNC24	LINERXSYNC25	TDLCLK	—	—	—	—
10	VDD	LINERXDATA25	LINERXCLK25	LINERXSYNC26	DS2AISCLK	—	—	—	—
11	VSS	LINERXDATA26	LINERXCLK26	LINERXSYNC27	VDD	—	—	—	—
12	LINERXDATA27	LINERXSYNC28	LINERXCLK27	LINERXCLK28	TCBDATA	—	—	—	—
13	LINERXSYNC29	LINERXCLK29	LINERXDATA28	LINERXDATA29	TCBCLK	—	—	—	—
14	LINETXDATA1	LINETXCLK1	LINETXSYNC2	LINETXSYNC1	TCBSYNC	—	—	—	—
15	LINETXSYNC3	LINETXDATA2	LINETXCLK3	LINETXCLK2	RCBDATA	—	—	—	—
16	VSS	LINETXSYNC4	LINETXCLK4	LINETXDATA3	VDD	—	—	—	—
17	VDD	LINETXSYNC5	LINETXCLK5	LINETXDATA4	RCBCLK	—	—	—	—
18	LINETXCLK6	LINETXSYNC6	LINETXDATA6	LINETXDATA5	RCBSYNC	—	—	—	—
19	LINETXDATA7	LINETXCLK7	LINETXSYNC8	LINETXSYNC7	RDLCLK	—	—	—	—
20	LINETXSYNC9	LINETXDATA8	LINETXCLK9	LINETXCLK8	VSS	—	—	—	—
21	VSS	LINETXSYNC10	LINETXCLK10	LINETXDATA9	LINETXDATA13	—	—	—	—
22	VDD	LINETXDATA10	LINETXCLK11	LINETXSYNC11	VDD	LINETXSYNC14	VSS	RDLDATA	DS3DATAINCLK
23	LINETXSYNC12	LINETXDATA11	LINETXCLK12	VSS	LINETXDATA16	LINETXSYNC18	LINETXCLK19	LINETXDATA20	LINETXSYNC22
24	LINETXSYNC13	LINETXDATA12	LINETXCLK14	LINETXCLK15	LINETXCLK16	LINETXCLK17	LINETXCLK18	LINETXDATA19	LINETXSYNC21
25	VSS	LINETXCLK13	LINETXSYNC15	LINETXSYNC16	LINETXSYNC17	LINETXDATA17	LINETXSYNC19	LINETXCLK20	LINETXDATA21
26	VDD	VSS	LINETXDATA14	LINETXDATA15	VDD	VSS	LINETXDATA18	LINETXSYNC20	LINETXCLK21

Table 3-1. Pin Matrix (continued)

	K	L	M	N	P	R	T	U	V
1	VDD	VSS	LINERXSYNC5	LINERXDATA3	LINERXSYNC2	RLSDATA7	VSS	VDD	RLSSPE
2	LINERXSYNC7	LINERXSYNC6	LINERXDATA4	LINERXCLK3	LINERXCLK2	LINERXSYNC1	RLSDATA4	RLSDATA1	RLSPAR
3	LINERXCLK7	LINERXCLK6	LINERXCLK5	LINERXSYNC4	LINERXDATA1	RLSDATA6	RLSDATA3	RLSDATA0	RLSJ0J1V1
4	LINERXDATA6	LINERXDATA5	LINERXCLK4	LINERXSYNC3	LINERXDATA2	LINERXCLK1	RLSDATA5	RLSDATA2	RLSCLK
5	LINERXSYNC16	VDD	SCAN_MODE	SCAN_EN	IDDQ	TCK	VDD	TDI	TDO
6	—	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—	—
11	—	VSS	VSS	VSS	VSS	VSS	VSS	—	—
12	—	VSS	VSS	VSS	VSS	VSS	VSS	—	—
13	—	VSS	VSS	VSS	VSS	VSS	VSS	—	—
14	—	VSS	VSS	VSS	VSS	VSS	VSS	—	—
15	—	VSS	VSS	VSS	VSS	VSS	VSS	—	—
16	—	VSS	VSS	VSS	VSS	VSS	VSS	—	—
17	—	—	—	—	—	—	—	—	—
18	—	—	—	—	—	—	—	—	—
19	—	—	—	—	—	—	—	—	—
20	—	—	—	—	—	—	—	—	—
21	—	—	—	—	—	—	—	—	—
22	DS3NEGDATAIN	VDD	DS3POSDATAIN	DS3DATAOUTCLK	DS3NEGDATAOUT	DS3POSDATAOUT	VDD	PHASEDETDOWN	PHASEDETUP
23	LINETXSYNC23	LINETXSYNC24	LINETXCLK25	LINETXDATA26	LINETXSYNC27	LINETXCLK28	LINETXDATA29	DTN	DATA0
24	LINETXCLK22	LINETXCLK23	LINETXCLK24	LINETXDATA25	LINETXSYNC28	LINETXCLK29	RSTN	PAR1	DATA3
25	LINETXDATA22	LINETXDATA23	LINETXSYNC25	LINETXCLK26	LINETXCLK27	LINETXDATA28	PMRST	PAR0	DATA1
26	VDD	VSS	LINETXDATA24	LINETXSYNC26	LINETXDATA27	LINETXSYNC29	VSS	VDD	DATA2

Table 3-1. Pin Matrix (continued)

	W	Y	AA	AB	AC	AD	AE	AF
1	TLSDATA6	TLSDATA2	VSS	VDD	RLSSYNC52	RTOACCLK	VSS	VDD
2	TLSDATA7	TLSDATA3	TLSCCLK	TLSSPE	RLSC52	TLSSYNC52	TTOACDATA	VSS
3	TLSDATA5	TLSDATA1	TLSPAR	TLSV1	TLSC52	RTOACDATA	RPOACCLK	TTOACSYNC
4	RLSV1	TLSDATA4	TLSDATA0	TLSJ0J1V1	VSS	RPOACDATA	TPOACCLK	RPOACSYNC
5	TMSN	VSS	RTOACSYNC	VDD	TPOACSYNC	TPOACDATA	LOSEXT	VDD
6	—	—	—	TTOACCLK	AUTO_AIS1	AUTO_AIS3	AUTO_AIS2	VSS
7	—	—	—	VSS	RHSCP	RHSFSYNCH	RHSDN	RHSDP
8	—	—	—	TRSTN	THSSYNCP	RHSCN	THSCN	THSCP
9	—	—	—	IC3STATEN	VDDA_CDR	THSSYNCH	THSDN	THSDP
10	—	—	—	CTAPRH	RPSC155P	RPSD155P	RPSD155N	VDD
11	—	—	—	VDD	REF10	RPSC155N	CTAPTH	VSS
12	—	—	—	VSSA_CDR	TPSC155P	REF14	RESLO	RESHI
13	—	—	—	CTAPRP	LOPOHCLKIN	TPSC155N	TPSD155N	TPSD155P
14	—	—	—	LOPOHVALIDIN	LOPOHDATAIN	ECSEL	BYPASS	TSTPHASE
15	—	—	—	LOPOHCLKOUT	ETOGGLE	TSTSFTLD	EXDNUP	TSTMODE
16	—	—	—	VDD	TSTMUX0	DS1XCLK	TSTMUX1	VSS
17	—	—	—	LOPOHDATAOUT	E1XCLK	MPMODE	MPCLK	VDD
18	—	—	—	LOPOHVALIDOUT	CSN	DSN	ADSN	RWN
19	—	—	—	RXDATAEN	ADDR0	ADDR3	ADDR1	ADDR2
20	—	—	—	VSS	ADDR4	ADDR7	ADDR5	ADDR6
21	—	—	—	MODE2_PLL	ADDR8	ADDR10	ADDR9	VSS
22	TXDATAEN	VSS	ADDR13	VDD	ADDR12	VDDD_PLL	ADDR11	VDD
23	DATA4	DATA8	DATA12	ADDR19	VSS	VSSS_PLL	VDDS_PLL	VSSA_PLL
24	DATA7	DATA11	DATA14	INTN	ADDR17	CLKIN_PLL	MODE1_PLL	MODE0_PLL
25	DATA5	DATA9	DATA13	DATA15	APS_INTN	ADDR16	ADDR14	VSS
26	DATA6	DATA10	VSS	VDD	ADDR18	ADDR15	VSS	VDD

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 4-1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
dc Supply Voltage Range	V _{DD}	−0.5	4.6	V
Storage Temperature Range	T _{stg}	−65	125	°C
Maximum Voltage (digital input pins)	—	—	5.25	V
Minimum Voltage (digital input pins)	—	−0.3	—	V

4.2 Thermal Parameters (Definitions and Values)

System and circuit board level performance depends not only on device electrical characteristics, but also on device thermal characteristics. The thermal characteristics frequently determine the limits of circuit board or system performance, and they can be a major cost adder or cost avoidance factor. When the die temperature is kept below 125 °C, temperature activated failure mechanisms are minimized. The thermal parameters that Agere provides for its packages help the chip and system designer choose the best package for their applications, including allowing the system designer to thermally design and integrate their systems.

It should be noted that all the parameters listed below are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

Θ_{JA}—Junction to Air Thermal Resistance

Θ_{JA} is a number used to express the thermal performance of a part under JEDEC standard natural convection conditions. Θ_{JA} is calculated using the following formula:

$$\Theta_{JA} = (T_J - T_{amb})/P; \text{ where } P = \text{power}$$

Θ_{JMA}—Junction to Moving Air Thermal Resistance

Θ_{JMA} is effectively identical to Θ_{JA} but represents performance of a part mounted on a JEDEC four layer board inside a wind tunnel with forced air convection. Θ_{JMA} is reported at airflows of 200 lft./min and 500 lft./min, which roughly correspond to 1 m/s and 2.5 m/s (respectively). Θ_{JMA} is calculated using the following formula:

$$\Theta_{JMA} = (T_J - T_{amb})/P$$

Θ_{JC}—Junction to Case Thermal Resistance

Θ_{JC} is the thermal resistance from junction to the top of the case. This number is determined by forcing nearly 100% of the heat generated in the die out the top of the package by lowering the top case temperature. This is done by placing the top of the package in contact with a copper slug kept at room temperature using a liquid refrigeration unit. Θ_{JC} is calculated using the following formula:

$$\Theta_{JC} = (T_J - T_C)/P$$

Θ_{JB}—Junction to Board Thermal Resistance

Θ_{JB} is the thermal resistance from junction to board. This number is determined by forcing the heat generated in the die out of the package through the leads or balls by lowering the board temperature and insulating the package top. This is done using a special fixture, which keeps the board in contact with a water chilled copper slug around the perimeter of the package while insulating the package top. Θ_{JB} is calculated using the following formula:

$$\Theta_{JB} = (T_J - T_B)/P$$

Ψ_{JT}

Ψ_{JT} correlates the junction temperature to the case temperature. It is generally used by the customer to infer the junction temperature while the part is operating in their system. It is not considered a true thermal resistance. Ψ_{JT} is calculated using the following formula:

$$\Psi_{JT} = (T_J - T_C)/P$$

Table 4-2. Thermal Parameter Values

Parameter	Temperature °C/Watt
Θ _{JA}	15.1
Θ _{JMA} (1 m/s)	11.8
Θ _{JMA} (2.5 m/s)	10.3
Θ _{JC}	4.2
Θ _{JB}	10.1
Ψ _{JT}	1.0

4.3 Reliability

Product reliability can be calculated as the probability that the product will perform under normal operating conditions for a set period of time. Factors influencing the reliability of a product cover a range of variables, including design and manufacturing. The failure rate of a product is given as the number of units failing per unit time. This failure rate is known as FIT, which is as follows:

1 FIT = 1 failure/1x10⁹ hours.

Another unit used for failure rate is known as MTBF, which is 1/FIT. Many assumptions are made when calculating the failure rate for a product, such as the average junction temperature and activation energy. The assumptions made for calculating FIT and MTBF are shown in Table 4-3:

Table 4-3. Reliability Data

Junction Temperature	FIT (Per 1x10 ⁹ Device Hours)	MTBF	Activation Energy
55 °C	34	2.9x10 ⁷ hours	0.7eV

4.4 Handling Precautions

Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. Agere employs both a human-body model (HBM) and a charged-device model (CDM) qualification requirement in order to determine ESD susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114 (HBM) and JESD22-C101 (CDM) standards.

Table 4-4. Handling Precaution

Device	Minimum HBM Threshold	Minimum CDM Threshold	
		Corner	Non-Corner
TMXF28155	2000 V	500 V	500 V

4.5 Operating Conditions

The following tables list the voltages required for proper operation of the TMXF28155 device, along with their tolerances.

Table 4-5. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power	VDD	3.14	3.3	3.47	V
Ground	VSS	—	0.0	—	V
1.0 V: LVDS Reference*	LVDS_REF10	—	1.0	—	V
1.4 V: LVDS Reference*	LVDS_REF14	—	1.4	—	V
Ambient Operating Temperature Range	TA	−40	—	85	°C

* Internal reference voltage is used if SMPR_LVDS_REF_SEL = 1, or else external voltage is used.

4.5.1 Power Consumption

Table 4-6. Power Consumption

Parameter	Typical Power*	Unit
VDD = 3.5 V, TA = 25 °C	3.185	W
VDD = 3.3 V, TA = 25 °C	2.772	W
VDD = 3.0 V, TA = 25 °C	2.190	W

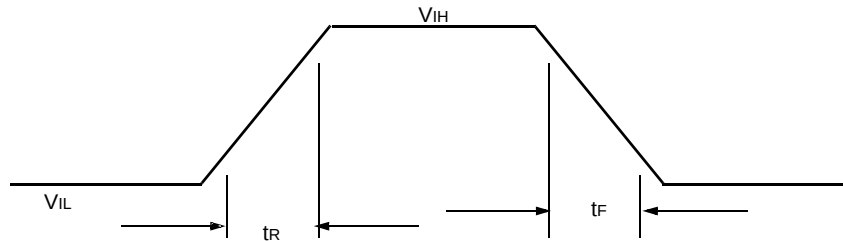
* When measuring power consumption of the *Supermapper*, the following blocks are powered on: TMUX, SPEMPR, VTMPR, DJA, FRAMER. MPCLK = 25 MHz.

4.6 Logic Interface Characteristics

Table 4-7. Logic Interface Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Current:					
Low	IOL	—	—	4.0	mA
High	IOH	—	—	4.0	mA
Output Voltage:					
Low	VOL	—	VSS	0.5	V
High	VOH	—	VDD – 0.5	3.465	V
Input Capacitance	CI	—	—	1.5	pF
Input Leakage	IL	—	—	1.0	μA
Input Voltage, High	VIH	—	VDD – 1.0	5.25	V
Input Voltage, Low	VIL	—	VSS	1.0	V

The input specification for the remaining (nonbalanced) inputs are specified in Figure 4-1.



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Figure 4-1. Single-Ended Input Specification

4.7 LVDS Interface Characteristics

Table 4-8. LVDS Interface Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Buffer Parameters						
Input Voltage Range, V_{IA} or V_{IB}	V_I	$V_{GPD} < 925 \text{ mV}$, dc—1 MHz	0.0	1.2	2.4	V
Input Differential Threshold	V_{IDTH}	$V_{GPD} < 925 \text{ mV}$, 311 MHz	−100	—	100	mV
Input Differential Hysteresis	V_{HYST}	$(+V_{IDTH}) - (-V_{IDTH})$	—	—	—*	mV
Receiver Differential Input Impedance	R_{IN}	With build-in termination, center-tapped	80	100	130	Ω
Output Buffer Parameters						
Output Voltage: Low (V_{OA} or V_{OB})	V_{OL}	$R_{LOAD} = 100 \Omega \pm 1\%$	—	—	1.475	V
High (V_{OA} or V_{OB})	V_{OH}	$R_{LOAD} = 100 \Omega \pm 1\%$	0.925	—	—	V
Output Differential Voltage	V_{OD}	$R_{LOAD} = 100 \Omega \pm 1\%$	0.25	—	0.40	V
Output Offset Voltage	V_{OS}	$R_{LOAD} = 100 \Omega \pm 1\%$	1.125	—	1.275	V
Output Impedance, Single Ended	R_O	$V_{CM} = 1.0 \text{ V}$ and 1.4 V	40	50	60	Ω
R_O Mismatch Between A and B	ΔR_O	$V_{CM} = 1.0 \text{ V}$ and 1.4 V	—	—	10	%
Change in Differential Voltage Between Complementary States	ΔV_{OD}	$R_{LOAD} = 100 \Omega \pm 1\%$	—	—	25	mV
Change in Output Offset Voltage Between Complementary States	ΔV_{OS}	$R_{LOAD} = 100 \Omega \pm 1\%$	—	—	25	mV
Output Current	I_{SA} , I_{SB}	Driver shorted to V_{SS}	6.8	—	24	mA
Output Current	I_{SAB}	Drivers shorted together	—	—	12	mA

* Buffer will not produce output transition when input is open-circuited.

5 Timing Characteristics

5.1 TMUX Block Timing

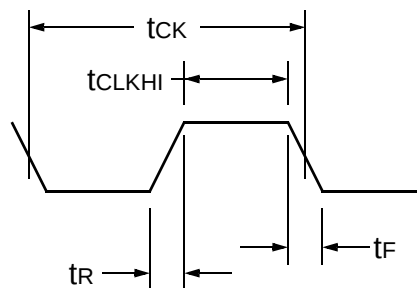
The TMUX (STS-N/STM-1) timing parameters can be grouped separately for clocks, inputs, and outputs. Table 5-1 shows the input clock specifications for this device. The rise and fall times refer to the transition times from 10% to 90% of full swing.

For definitions of the signal names, see [Section 2](#), Pin Information, on page 8.

Table 5-1. High-Speed Input Clock Specifications

Symbol	Parameter	Signal Name	155 Clock			51 Clock			Unit
			Min	Nominal	Max	Min	Nominal	Max	
FCK	Operating Frequency	THSCP/N	—	155.52 ± 30 ppm	—	—	51.84 ± 50 ppm	—	MHz
		RHSCP/N	—	155.52 ± 30 ppm	—	—	51.84 ± 50 ppm	—	MHz
		RPSC155P/N	—	155.52 ± 30 ppm	—	—			MHz
tCK	Clock Period	THSCP/N	—	6.43 ± 0.4%	—	—	19.29 ± 0.4%	—	ns
		RHSCP/N	—	6.43 ± 0.5%	—	—	19.29 ± 0.5%	—	ns
		RPSC155P/N	—	6.43 ± 0.5%	—	—			ns
tCLKHI	Clock Pulse High Time	THSCP/N	2.5	—	3.9	7.8	—	11.6	ns
		RHSCP/N	2.5	—	3.9	7.8	—	11.6	ns
		RPSC155P/N	2.5	—	3.9	—			ns
tR	Rise Time	THSCP/N	—	—	1.5	—	—	5.0	ns
		RHSCP/N	—	—	1.5	—	—	5.0	ns
		RPSC155P/N	—	—	1.5	—			ns
tF	Fall Time	THSCP/N	—	—	1.5	—	—	5.0	ns
		RHSCP/N	—	—	1.5	—	—	5.0	ns
		RPSC155P/N	—	—	1.5	—			ns

Note: When the true and complement inputs are floating, the input buffer will not oscillate.



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Figure 5-1. Generic Clock Timing

The output clock specifications are shown in Table 5-2.

Table 5-2. Output Clock Specifications

Signal Name	Reference CLK*	Frequency	Clock Pulse High Time (tCLKHI)	Test Condition	Max Rise Time (tR)	Max Fall Time (tF)	Unit
TLSCCLK	THSCP/N	19.44 MHz	24.43—27.00	CL = 50 pF	3.5	3.5	ns
TTOACCLK	THSCP/N	5.184 MHz	91.62—101.30	CL = 15 pF	3.5	3.5	ns
RLSCLK	RHSCP/N or Internal CDR Clock	19.44 MHz	24.43—27.00	CL = 50 pF	3.5	3.5	ns
RTOACCLK	RHSCP/N or Internal CDR Clock	5.184 MHz	91.62—101.30	CL = 15 pF	3.5	3.5	ns
TPSC155P/N	THSCP/N	155.5 MHz	3.119—3.311	CL = 15 pF	1.5	1.5	ns
TPOACCLK	THSCP/N	5.184 MHz	91.62—101.30	CL = 15 pF	3.5	3.5	ns
RPOACCLK	RHSCP/N	5.184 MHz	91.62—101.30	CL = 15 pF	3.5	3.5	ns
TLSC52	THSCP/N	51.84 MHz	9.162—10.130	CL = 30 pF	3.0	3.0	ns
RLSC52	RHSCP/N	51.84 MHz	9.162—10.130	CL = 30 pF	3.0	3.0	ns

* The specifications for the table are with all loopbacks disabled.

Note: Any of the telecom signals being used as inputs (slave *Supermapper*) need to meet these same output clock specifications.

Table 5-3. Input Timing Specifications

Input Name	Reference CLK	Min Setup Time (ts)	Min Hold Time (th)	Unit
Transmit Signals				
THSSYNCP/N	THSC ↑	3.5	0.0	ns
TLSDATA[7:0]	TLCLK ↑	5.0	0.0	ns
TLSPAR	TLCLK ↑	5.0	0.0	ns
TLSSPE	TLCLK ↓	5.0	0.0	ns
TLJ0J1V1	TLCLK ↓	5.0	0.0	ns
TLV1	TLCLK ↓	5.0	0.0	ns
TLSSYNC52	TLSC52 ↓	4.0	2.5	ns
TTOACDATA	TTOACCLK ↑	10.0	3.5	ns
TPOACDATA	TPOACCLK ↑	10.0	1.0	ns
Receive Signals				
RHSDP/N	RHSCP/N ↑↓*	2.0	0.0	ns
RPSD155P/N	RPSC155P/N ↑	2.0	0.0	ns
RLSDATA[7:0]	RLCLK ↓	4.0	0.0	ns
RLSPAR	RLCLK ↓	4.0	0.0	ns
RLSSPE	RLCLK ↓	4.0	0.0	ns
RLJ0J1V1	RLCLK ↓	4.0	0.0	ns
RLV1	RLCLK ↓	4.0	0.0	ns
RLSSYNC52	RLSC52 ↓	4.0	3.0	ns
Miscellaneous Signals				
LOSEXT	NA	ASYNC	ASYNC	—
AUTO_AIS[3:1]	NA	ASYNC	ASYNC	—

* Register 0x00010, bit 2, SMPR_RETIME_CKCLK_EDGE.

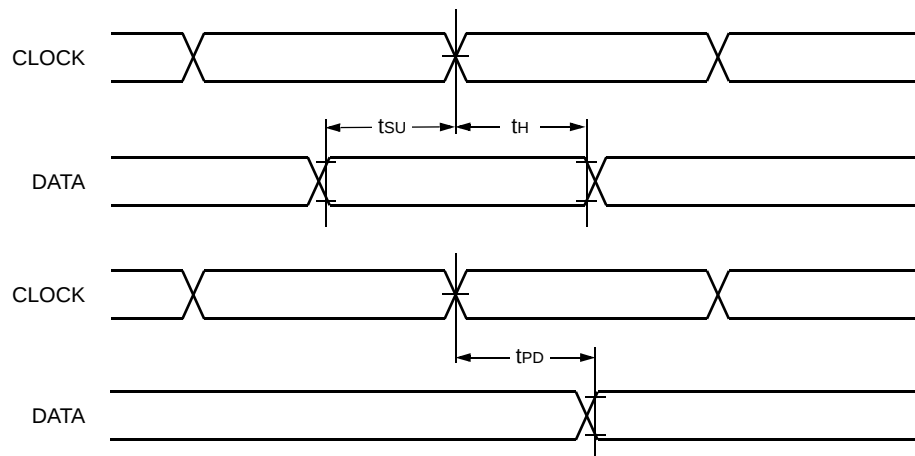


Figure 5-2. Generic Interface Data Timing

Table 5-4. Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay [†]		Unit
			tPD		
			Min	Max	
Transmit Signals					
THSDP/N	THSCP/N ↑	CL = 15 pF	2.6	8.0	ns
TPSD155P/N	TPSC155P/N↑	CL = 15 pF	0.6	2.9	ns
TLSDATA[7:0]	TLCLK ↑↓*	CL = 50 pF	4.0	12.0	ns
TLSPAR	TLCLK ↑↓*	CL = 50 pF	4.0	12.0	ns
TLSSPE	TLCLK ↑	CL = 50 pF	4.0	10.5	ns
TLSJ0J1V1	TLCLK ↑	CL = 50 pF	4.0	10.5	ns
TLSV1	TLCLK ↑	CL = 50 pF	4.0	10.5	ns
TLSSYNC52	TLSC52 ↑	CL = 30 pF	0.0	2.0	ns
TTOACSYNC	TTOACCLK ↑	CL = 15 pF	–2.0	30.0	ns
TPOACSYNC	TPOACCLK ↑	CL = 15 pF	–2.0	30.0	ns
Receive Signals					
RLSDATA[7:0]	RLCLK ↑	CL = 50 pF	5.5	12.0	ns
RLSPAR	RLCLK ↑	CL = 50 pF	5.5	12.0	ns
RLSSPE	RLCLK ↑	CL = 50 pF	5.5	12.0	ns
RLSJOJ1V1	RLCLK ↑	CL = 50 pF	5.5	12.0	ns
RLSVI	RLCLK ↑	CL = 50 pF	5.5	12.0	ns
RLSSYNC52	RLSC52 ↑	CL = 30 pF	0.5	3.0	ns
RTOACSYNC	RTOACCLK ↑	CL = 15 pF	–2.0	30.0	ns
RTOACDATA	RTOACCLK ↑	CL = 15 pF	–2.0	30.0	ns
RPOACSYNC	RPOACCLK ↑	CL = 15 pF	–2.0	30.0	ns
RPOACDATA	RPOACCLK ↑	CL = 15 pF	–2.0	30.0	ns
RHSFSYN CN	RLCLK ↑	CL = 30 pF	–1.0	8.0	ns
Miscellaneous Signals					
AUTO_AIS[3:1]	NA	—	ASYNC	ASYNC	—

* Register 0x00010, bit 1, SMPR_TELECOMBUS_EDGE.

† Propagation delay skew, t_{PLH} – t_{PHL}, is ± 200 ps. Negative propagation delay indicates that output comes out ahead of reference clock.

5.2 DS3 Timing

Table 5-5. DS3 Input Clock Specifications

Symbol	Parameter	Signal Name	Min	Max	Unit
F _{CK}	Clock Frequency	DS3DATAINCLK DS3DATAOUTCLK	—	44.736 ± 50 ppm	MHz
t _{CK}	Clock Period	DS3DATAINCLK DS3DATAOUTCLK	—	22.353	ns
t _{CLKHI}	Clock Pulse High Time	DS3DATAINCLK DS3DATAOUTCLK	6 6	16 12	ns ns
t _R	Rise Time	DS3DATAINCLK DS3DATAOUTCLK	0	2	ns
t _F	Fall Time	DS3DATAINCLK DS3DATAOUTCLK	0	2	ns

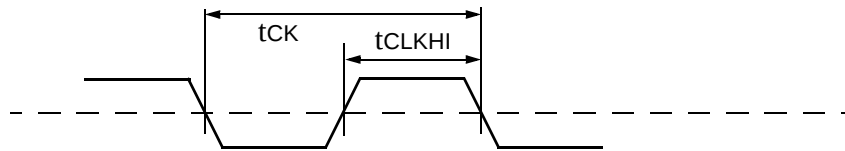


Figure 5-3. DS3DATAOUTCLK Timing

Table 5-6. Input Timing Specifications

Input Name	Reference CLK	Min Setup Time (t _s)	Min Hold Time (t _h)	Unit
DS3POSDATAIN	DS3DATAINCLK ↑↓*	4	0	ns
DS3NEGDATAIN	DS3DATAINCLK ↑↓*	4	0	ns

* Register 0x100A1, bit 0, M13_RDS3_EDGE. Register 0x30019, bit 5, SPE_TDS3CLK_EDGE.

Table 5-7. Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay t _{PD}		Unit
			Min	Max	
DS3POSDATAOUT	DS3DATAOUTCLK ↑↓	CL = 15 pF	2	6.5	ns
DS3NEGDATAOUT	DS3DATAOUTCLK ↑↓	CL = 15 pF	2	6.5	ns

Note: The up arrow applies to the SPE block, which means the DS3 output from SPE is clocked out on a fixed rising edge of DS3DATAOUTCLK. The down arrow applies to the M13 block, which means the DS3 output from M13 is clocked out on a fixed falling edge of DS3DATAOUTCLK.

5.3 M13 Timing

Table 5-8. M13 Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
FCK	Clock Frequency	TCBCLK	—	93.983 gapped	—	kHz
		TDLCLK	—	28.195 gapped	—	kHz
		E1XCLK	2.048	32.768	65.536	MHz
		DS1XCLK	1.544	24.704	49.408	MHz
		DS2AISCLK	—	6.312	—	MHz
		RCBCLK	—	93.983	—	kHz
		RDLCLK	—	28.195	—	kHz
tCLKHI	Clock Pulse High Time	TCBCLK	212.19	223.53	250.77	ns
		TDLCLK	212.19	223.53	250.77	ns
		RCBCLK	212.19	223.53	250.77	ns
		RDLCLK	212.19	223.53	250.77	ns
tR	Rise Time	TCBCLK	0	—	3	ns
		TDLCLK	0	—	3	ns
		E1XCLK	0	—	3	ns
		DS1XCLK	0	—	3	ns
		DS2AISCLK	0	—	3	ns
		RCBCLK	0	—	3	ns
		RDLCLK	0	—	3	ns
tF	Fall Time	TCBCLK	0	—	3	ns
		TDLCLK	0	—	3	ns
		E1XCLK	0	—	3	ns
		DS1XCLK	0	—	3	ns
		DS2AISCLK	0	—	3	ns
		RCBCLK	0	—	3	ns
		RDLCLK	0	—	3	ns

Table 5-9. Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (th)		Unit
		Min	Max	Min	Max	
TCBDATA	TCBCLK ↑	50	—	0	—	ns
TDLDATA	TDLCLK ↑	50	—	0	—	ns

Table 5-10. Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay tPD		Unit
			Min	Max	
TCBSYNC	TCBCLK ↑	CL = 15 pF	0.5	10	ns
RCBSYNC	RCBCLK ↑	CL = 15 pF	0.5	10	ns
RCBDATA	RCBCLK ↑	CL = 15 pF	0.5	10	ns
RDLDATA	RDLCLK ↑	CL = 15 pF	2	10	ns

5.4 VT Mapper Timing

5.4.1 VT Mapper Lower-Order Path Overhead Interface Timing

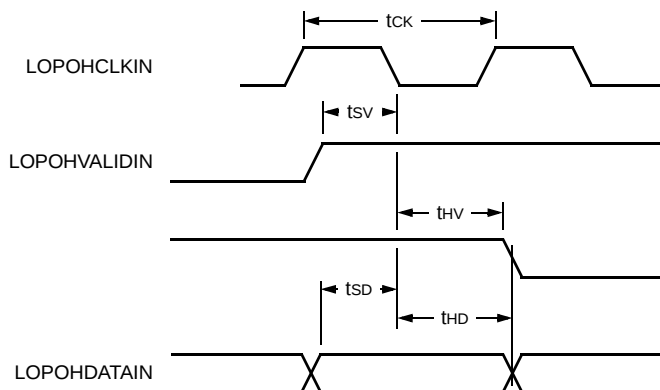
Table 5-11. VT Mapper Receive Path Overhead Detailed Timing

Symbol	Parameter	Min	Max	Unit
FCK	Clock Frequency	6.48	6.48	MHz
tCK	Clock Period	154	154	ns
tCLKHI	Clock Pulse High Time	50	75	ns
tR	Clock Rise Time	0	3	ns
tF	Clock Fall Time	0	3	ns
tSD *	LOPOH Data Setup Time	5	—	ns
tHD *	LOPOH Data Hold Time	2.0	—	ns
tSV †	LOPOH Valid Signal Setup Time	5	—	ns
tHV †	LOPOH Valid Signal Hold Time	3.7	—	ns
tPDV ‡	Clock to LOPOH Valid Signal Out	2.0	10.0	ns
tPDD ‡	Clock to LOPOH Data Out	2.0	10.0	ns

* tSD, tHD $\square \Rightarrow$ LOPOH_CLK $\downarrow$.

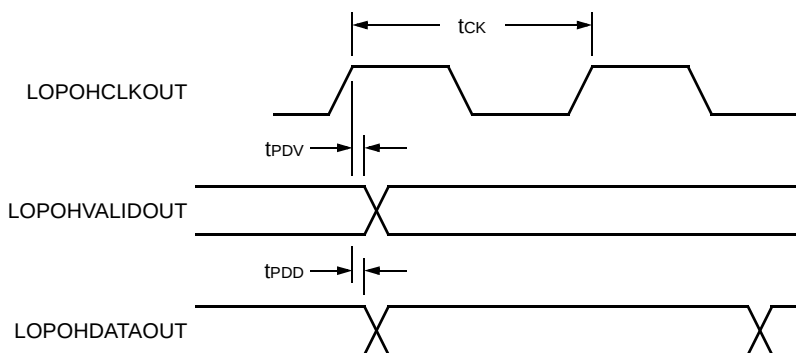
† tSV, tHV $\square \Rightarrow$ LOPOH_CLK $\downarrow$.

‡ tPDV, tPDD $\square \Rightarrow$ LOPOH_CLK $\uparrow$.



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Figure 5-4. VT Mapper Transmit Path Overhead Detailed Timing



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Figure 5-5. VT Mapper Receive Path Overhead Detailed Timing

5.5 Concentration Highway (CHI) Timing

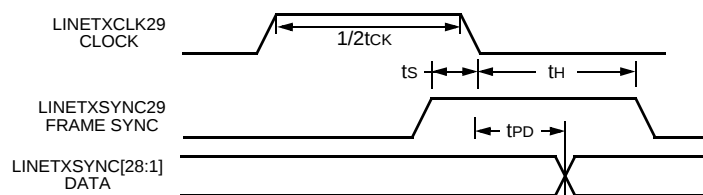
Table 5-12 and Table 5-13 with Figure 5-6 and Figure 5-7, respectively, illustrate the detailed CHI timing for clock, data, and frame synchronization.

Table 5-12. CHI Transmit Timing Characteristics

Symbol	Parameter	Min	Max	Unit
FCK	Clock Frequency*	2.048	16.384	MHz
tCK	Clock Period	488.2	61.04	ns
tR	Clock Rise Time	0	3	ns
tF	Clock Fall Time	0	3	ns
tS [†]	Frame Sync Setup Time	35	—	ns
tH [†]	Frame Sync Hold Time	0	—	ns
tPD [†]	Clock to CHI Data Delay	—	25	ns

* Fck can be either 2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz.

† tS, tH, and tPD, ⇒ LINETXCLK29 ↑↓ (Register 0x80050, bit 4, FRM_TFSCKE).



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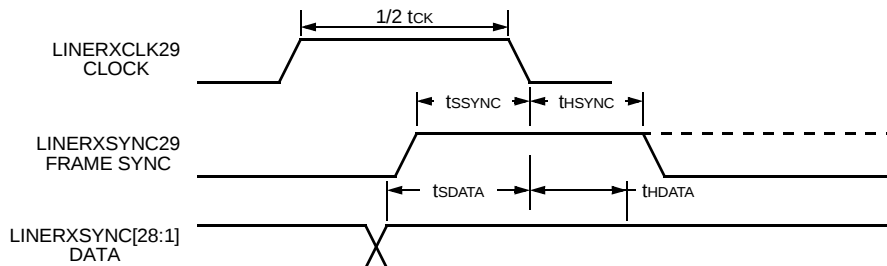
Figure 5-6. CHI Transmit I/O Timing

Table 5-13. CHI Receive Timing Characteristics

Symbol	Parameter	Min	Max	Unit
FCK	Clock Frequency*	2.048	16.384	MHz
tCK	Clock Period	488.2	61.04	ns
tR	Clock Rise Time	0	3	ns
tF	Clock Fall Time	0	3	ns
tSSYNC [†]	Frame Sync Setup Time	30	—	ns
tHSYNC [†]	Frame Sync Hold Time	3.4	—	ns
tSDATA [†]	CHI Data Setup Time	25	—	ns
tHDATA [†]	CHI Data Hold Time	0	—	ns

* FCK can be either 2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz.

† LINERXSYNC29 ↑↓ (Register 0x80150, bit 13, FRM_RFSCKE).



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Figure 5-7. CHI Receive I/O Timing

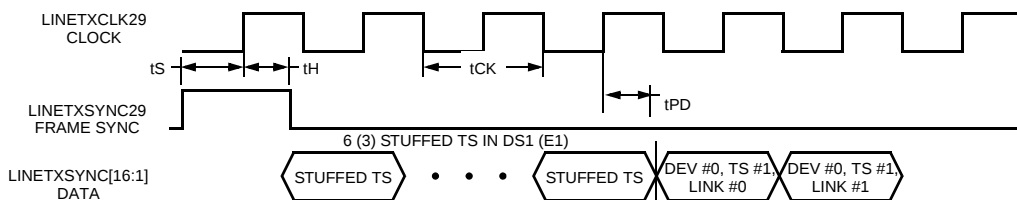
5.6 Parallel System Bus Timing

Table 5-14 and Table 5-15 with Figure 5-8 and Figure 5-9, respectively, show the transmit and receive timing. In the transmit direction (to the system interface), the frame sync is sampled and the data is clocked out on the rising edge of the clock. In the receive direction (from the switch), the data and frame sync are sampled on the rising edge of the clock.

Table 5-14. PSB Interface Transmit Timing Characteristics

Symbol	Parameter	Min	Max	Unit
FCK	Clock Frequency	19.44	19.44	MHz
tCK	Clock Period	51.44	51.44	ns
tR	Clock Rise Time	0	3	ns
tF	Clock Fall Time	0	3	ns
ts*	Frame Sync Setup Time	8	—	ns
th*	Frame Sync Hold Time	0	—	ns
tPD*	Clock to PSB Out Delay	3	10	ns

* LINEXCLK29 $\uparrow\downarrow$ (Register 0x80050, bit 4, FRM_TFSCKE).



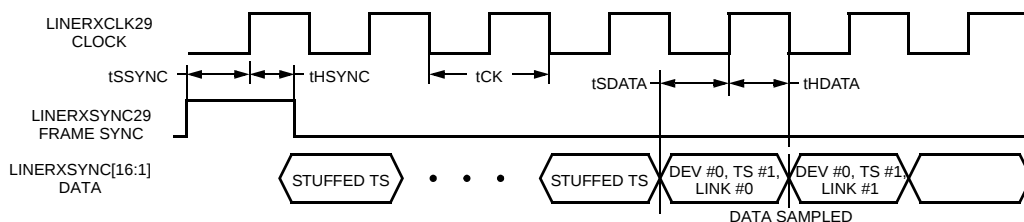
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Figure 5-8. Parallel System Bus Interface Transmit I/O Timing

Table 5-15. PSB Interface Receive Timing Characteristics

Symbol	Parameter	Min	Max	Unit
FCK	Clock Frequency	19.44	19.44	MHz
tCK	Clock Period	51.44	51.44	ns
tR	Clock Rise Time	0	3	ns
tF	Clock Fall Time	0	3	ns
tSSYNC*	Frame Sync Setup Time	8	—	ns
tHSYNC*	Frame Sync Hold Time	0	—	ns
tSDATA*	PSB to Clock Setup Time	8	—	ns
tHDATA*	PSB Hold Time from Clock	2.8	—	ns

* LINEXCLK29 $\uparrow\downarrow$ (Register 0x80150, bit 13, FRM_RFSCKE).



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Figure 5-9. Parallel System Bus Interface Receive I/O Timing

5.7 NSMI Timing (6-Pin) (to/from Framer)

Table 5-16. NSMI Input/Output Clock Specifications

Symbol	Parameter	Signal Name	I/O	Min	Nom	Max	Unit
FCK	Clock Frequency	LINETXCLK29 LINERXCLK29	Output Input	–50 ppm –50 ppm	51.84 51.84	50 ppm 50 ppm	MHz MHz
tCK = 1/FCK	Clock Period	LINETXCLK29 LINERXCLK29	Output Input	— —	19.29 19.29	— —	ns ns
tCKHI	Clock Pulse High Time	LINETXCLK29 LINERXCLK29	Output Input	6 6	— —	12 12	ns ns
tR	Rise Time	LINETXCLK29 LINERXCLK29	Output Input	— —	— —	3 3	ns ns
tF	Fall Time	LINETXCLK29 LINERXCLK29	Output Input	— —	— —	3 3	ns ns

Table 5-17. Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (th)		Unit
		Min	Max	Min	Max	
LINERXDATA29	LINERXCLK29 ↑	3	—	0	—	ns
LINERXSYNC29	LINERXCLK29 ↑	3	—	0.5	—	ns

Table 5-18. Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay tPD		Unit
			Min	Max	
LINETXDATA29	LINETXCLK29 ↑	CL = 15 pF	0.1	3.0	ns
LINETXSYNC29	LINETXCLK29 ↑	CL = 15 pF	0.1	5.0	ns

5.8 NSMI Timing (7-Pin) (to/from Framer)

Table 5-19. NSMI Output Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
FCK	Clock Frequency	LINETXCLK29 LINERXCLK29 RXDATAEN	–50 ppm –50 ppm –50 ppm	51.84/44.736 51.84/44.736 51.84/44.736	50 ppm 50 ppm 50 ppm	MHz MHz MHz
tCK = 1/FCK	Clock Period	LINETXCLK29 LINERXCLK29 RXDATAEN	— — —	19.29/22.35 19.29/22.35 19.29/22.35	— — —	ns ns ns
tCKHI	Clock Pulse High Time	LINETXCLK29 LINERXCLK29 RXDATAEN	6 6 —	1/2 tck 1/2 tck 1/2 tck	— — —	ns ns ns
tR	Rise Time	LINETXCLK29 LINERXCLK29 RXDATAEN	0 0 0	— — —	3 3 3	ns ns ns
tF	Fall Time	LINETXCLK29 LINERXCLK29 RXDATAEN	0 0 0	— — —	3 3 3	ns ns ns

Table 5-20. NSMI Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (th)		Unit
		Min	Max	Min	Max	
LINERXDATA29	LINERXCLK29 ↑	3.0	—	0	—	ns
LINERXSYNC29	LINERXCLK29 ↑	3.0	—	0.5	—	ns

Table 5-21. NSMI Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay tPD		Unit
			Min	Max	
LINETXDATA29	LINETXCLK29 ↑	CL = 15 pF	0.1	3.0	ns
LINETXSYNC29	LINETXCLK29 ↑	CL = 15 pF	0.1	5.0	ns
TXDATAEN	LINETXCLK29 ↑	CL = 15 pF	−0.6	0.2	ns

5.9 CHI Interface Timing

Table 5-22. CHI Interface Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
FCK	Clock Frequency	LINERXDATA29	−130 ppm	1.544 or 2.048	130 ppm	MHz
		LINERXCLK29	−50 ppm	2.048 or 4.096 or 8.192 or 16.384	50 ppm	MHz
		LINETXCLK29	−50 ppm	2.048 or 4.096 or 8.192 or 16.384	50 ppm	MHz
tCK = 1/FCK	Clock Period	LINERXDATA29 LINERXCLK29 LINETXCLK29	—	647.67 or 488.28 488.28, or 244.14 or 122.07, or 61.04 488.28, or 244.14 or 122.07, or 61.04	—	ns ns ns ns ns
tCKHI	Clock Pulse High Time	LINERXDATA29, LINERXCLK29 LINETXCLK29	—	1/2 tck	—	ns
tr	Rise Time	LINERXDATA29, LINERXCLK29 LINETXCLK29	0	—	3	ns
tf	Fall Time	LINERXDATA29, LINERXCLK29 LINETXCLK29	0	—	3	ns

Table 5-23. CHI Interface Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (th)		Unit
		Min	Max	Min	Max	
LINERXSYNC[28:1]	LINERXCLK[28:1] ↑↓	25	—	0	—	ns
LINERXSYNC29	LINERXCLK29 ↑↓	30	—	3.4	—	ns
LINETXSYNC29	LINETXCLK29 ↑↓	35	—	1.6	—	ns

Table 5-24. CHI Interface Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay tPD		Unit
			Min	Max	
LINETXSYNC[28:1]	LINETXCLK29 ↑↓	CL = 15 pF	—	25	ns

5.10 PSB Interface Timing

Table 5-25. PSB Interface Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
FCK	Clock Frequency	LINERXDATA29	–130 ppm	1.544	130 ppm	MHz
		LINERXCLK29	–50 ppm	or 2.048	50 ppm	MHz
		LINEXCLK29	–50 ppm	19.44	50 ppm	MHz
		LINEXCLK29	–50 ppm	19.44	50 ppm	MHz
tCK = 1/FCK	Clock Period	LINERXDATA29	—	647.67	—	ns
		LINERXCLK29	—	or 488.28	—	ns
		LINEXCLK29	—	51.44	—	ns
		LINEXCLK29	—	51.44	—	ns
tCKHI	Clock Pulse High Time	LINERXDATA29	—	1/2 tck	—	ns
		LINERXCLK29	—	1/2 tck	—	ns
		LINEXCLK29	—	1/2 tck	—	ns
		LINEXCLK29	—	1/2 tck	—	ns
tR	Rise Time	LINERXDATA29	0	—	3	ns
		LINERXCLK29	0	—	3	ns
		LINEXCLK29	0	—	3	ns
		LINEXCLK29	0	—	3	ns
tF	Fall Time	LINERXDATA29	0	—	3	ns
		LINERXCLK29	0	—	3	ns
		LINEXCLK29	0	—	3	ns
		LINEXCLK29	0	—	3	ns

Table 5-26. PSB Interface Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (th)		Unit
		Min	Max	Min	Max	
LINERXSYNC[16:1]	LINERXCLK29 ↑↓	8	—	2.8	—	ns
LINERXSYNC29	LINERXCLK29 ↑↓	8	—	0	—	ns
LINETXSYNC29	LINETXCLK29 ↑↓	8	—	0	—	ns

Table 5-27. PSB Interface Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay tPD		Unit
			Min	Max	
LINETXSYNC[16:1]	LINETXCLK29 ↑↓	CL = 15 pF	3	10	ns

5.11 Framer DS1/E1 Interface Timing

Table 5-28. Framer DS1/E1 Interface Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
Fck	Clock Frequency	TLSC52 LINERXCLK[29:1] LINETXCLK[29:1]	-50 ppm -130 ppm -50 ppm -130 ppm -50 ppm	51.84 1.544 or 2.048 1.544 or 2.048	50 ppm 130 ppm 50 ppm 130 ppm 50 ppm	MHz MHz MHz MHz MHz
tCK = 1/Fck	Clock Period	TLSC52 LINERXCLK[29:1] LINETXCLK[29:1]	—	19.29 647.67 or 488.28 647.67 or 488.28	—	ns ns ns ns ns
tCKHI	Clock Pulse High Time	TLSC52 LINERXCLK[29:1] LINETXCLK[29:1]	—	1/2 tck 1/2 tck 1/2 tck	—	ns ns ns
tR	Rise Time	TLSC52 LINERXCLK[29:1] LINETXCLK[29:1]	0 0 0	— — —	3 3 3	ns ns ns
tF	Fall Time	TLSC52 LINERXCLK[29:1] LINETXCLK[29:1]	0 0 0	— — —	3 3 3	ns ns ns

Table 5-29. Framer DS1/E1 Interface Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (th)		Unit
		Min	Max	Min	Max	
LINERXDATA[29:1]	LINERXCLK[29:1] ↑↓	12.0	—	9.0	—	ns
LINERXSYNC[29:1]	LINERXCLK[29:1] ↑↓	12.0	—	9.0	—	ns

Table 5-30. Framer DS1/E1 Interface Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay tPD		Unit
			Min	Max	
LINETXDATA[29:1]	LINETXCLK[29:1] ↑↓	CL = 15 pF	0.5	10	ns
LINETXSYNC[29:1]	LINETXCLK[29:1] ↑↓	CL = 15 pF	0.5	11	ns

5.12 DJA DS1/E1 Interface Timing

Table 5-31. DJA DS1/E1 Interface Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
Fck	Clock Frequency	LINERXCLK[29:1]	–130 ppm	1.544	130 ppm	MHz
			–50 ppm	or 2.048	50 ppm	MHz
		LINETXCLK[29:1]	–130 ppm	1.544	130 ppm	MHz
			–50 ppm	or 2.048	50 ppm	MHz
tCK = 1/Fck	Clock Period	LINERXCLK[29:1]	—	647.67	—	ns
				or 488.28		ns
		LINETXCLK[29:1]		647.67		ns
				or 488.28		ns
tCKHI	Clock Pulse High Time	LINERXCLK[29:1]	—	1/2 tck	—	ns
		LINETXCLK[29:1]		1/2 tck		ns
tR	Rise Time	LINERXCLK[29:1]	0	—	3	ns
		LINETXCLK[29:1]	0	—	3	ns
tF	Fall Time	LINERXCLK[29:1]	0	—	3	ns
		LINETXCLK[29:1]	0	—	3	ns

Table 5-32. DJA DS1/E1 Interface Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (th)		Unit
		Min	Max	Min	Max	
LINERXDATA[29:1]	LINERXCLK[29:1] ↑↓	NA	—	NA	—	ns

Table 5-33. DJA DS1/E1 Interface Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay tPD		Unit
			Min	Max	
LINETXDATA[29:1]	LINETXCLK[29:1] ↑↓	CL = 15 pF	–4.0	4.0	ns

5.13 M13 DS1/E1 Interface Timing

Table 5-34. M13 DS1/E1 Interface Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
Fck	Clock Frequency	LINERXCLK[29:1]	−130 ppm	1.544	130 ppm	MHz
			−50 ppm	or 2.048	50 ppm	MHz
		LINETXCLK[29:1]	−130 ppm	1.544	130 ppm	MHz
			−50 ppm	or 2.048	50 ppm	MHz
tck = 1/Fck	Clock Period	LINERXCLK[29:1]	—	647.67	—	ns
				or 488.28		ns
		LINETXCLK[29:1]		647.67		ns
				or 488.28		ns
tckHI	Clock Pulse High Time	LINERXCLK[29:1]	—	1/2 tck	—	ns
		LINETXCLK[29:1]		1/2 tck		ns
tr	Rise Time	LINERXCLK[29:1]	0	—	3	ns
		LINETXCLK[29:1]	0	—	3	ns
tF	Fall Time	LINERXCLK[29:1]	0	—	3	ns
		LINETXCLK[29:1]	0	—	3	ns

Table 5-35. M13 DS1/E1 Interface Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (th)		Unit
		Min	Max	Min	Max	
LINERXDATA[29:1]	LINERXCLK[29:1] ↑↓	12.0	—	8.0	—	ns

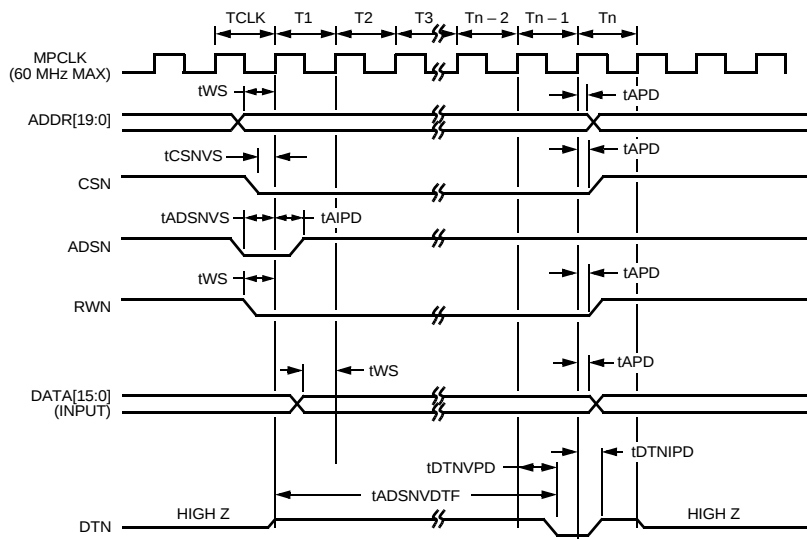
Table 5-36. M13 DS1/E1 Interface Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay tPD		Unit
			Min	Max	
LINETXDATA[29:1]	LINETXCLK[29:1] ↑↓	CL = 15 pF	−5.0	2.0	ns

5.14 Microprocessor Interface Timing

5.14.1 Synchronous Mode

The synchronous microprocessor interface mode is selected when MPMODE (pin AD17) = 1.



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Figure 5-10. Microprocessor Interface Synchronous Write Cycle (MPMODE (Pin AD17) = 1)

MPCLK 16 MHz minimum to 60* MHz maximum frequency.

ADDR [19:0] The address will be available throughout the entire cycle.

DATA[15:0] Data will be available during cycle T1.

RWN (Input) The read (H) write (L) signal is always high except during a write cycle.

CSN (Input) Chip select is an active-low signal.

DTN (Output) Data transfer acknowledge is active-low for one clock and then driven high before entering a high-impedance state. (This is done with an I/O pad using the input as feedback to qualify the 3-state term.) DTN will become 3-stated when CSN is high. Typically, DTN is active 4 or 5 MPCLK cycles after ADSN is low.

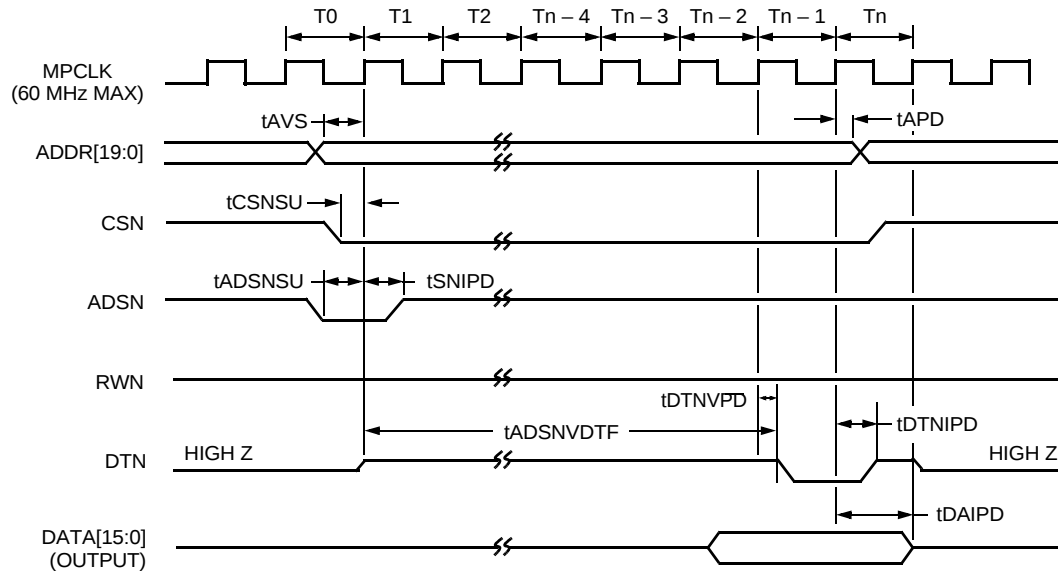
ADSN (Input) Address strobe is active-low. ADSN must be 1 MPCLK clock period wide.

* If DTN is used, then the maximum frequency for MPCLK is determined by the processor's setup specification for DTN. For example, a 9 ns setup time would limit MPCLK to 40 MHz for reliable DTN detection.

Table 5-37. Microprocessor Interface Synchronous Write Cycle Specifications

Symbol	Parameter	Setup (Min)	Hold (Min)	Delay (Max)	Unit
TCLK	MPCLK 16 MHz Min—60 MHz Max Frequency	—	—	—	ns
tWS	ADDR, RWN, DATA (write) Valid to MPCLK	3.5	0	—	ns
tAPD	MPCLK to ADDR, RWN, DATA, CSN (write) Invalid	—	5	—	ns
tCSNVS	CSN Valid to MPCLK	3.5	0	—	ns
tADSNVS	ADSN Valid to MPCLK	5.5	0	—	ns
tAIPD	MPCLK to ADSN Invalid	—	5	—	ns
tDTNVPD	MPCLK to DTN Valid	—	—	16	ns
tDTNIPD	MPCLK to DTN Invalid	—	—	16	ns
tADSNVDTF	ADSN Valid to DTN Fall	—	—	1000*	ns

* Certain registers in the VTMPR block have a very long acknowledge cycle (in the order of 32 MPCK). The reason is that those registers can also be accessed by the VTMPR lower order path overhead interface as part of SONET overhead termination functions. This interface runs at 6.48 MHz. Therefore, the user must insert long enough delay or use the DTN signal in MPU interface to read/write these registers correctly.



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Figure 5-11. Microprocessor Interface Synchronous Read Cycle (MPMODE (Pin AD17) = 1)

- MPCLK** 16 MHz minimum to 60* MHz maximum frequency.
- ADDR [19:0]** The address will be available throughout the entire cycle, and must be stable before ADSN turns high.
- DATA [15:0]** Read data is stable in $T_n - 1$.
- RWN (Input)** The read (H) write (L) signal is always high during the read cycle.
- CSN (Input)** Chip select is an active-low signal.
- DTN (Output)** Data transfer acknowledge on the host bus interface is initiated on T_6 . This signal is active for one clock and then driven high before entering a high-impedance state. (This is done with an I/O pad using the input as feedback to qualify the 3-state term.) Fall will become 3-stated when CS is high. Typically, DTN is active 4 or 5 MPCLK cycles after ADSN is low.
- ADSN (Input)** Address strobe is active-low. ADSN must be one MPCLK clock period wide.

* If DTN is used, then the maximum frequency for MPCLK is determined by the processor's setup specification for DTN. For example, a 9 ns setup time would limit MPCLK to 40 MHz for reliable DTN detection.

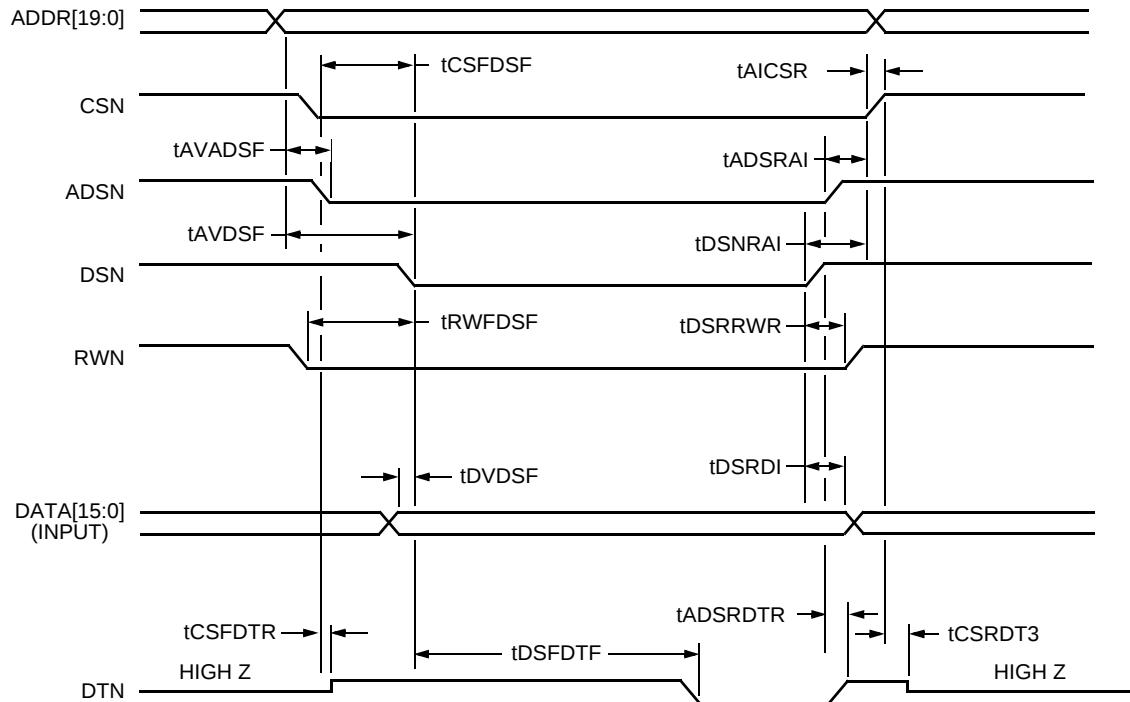
Table 5-38. Microprocessor Interface Synchronous Read Cycle Specifications

Symbol	Parameter	Setup (Min)	Hold (Min)	Delay (Min)	Delay (Max)	Unit
TCLK	MPCLK 16 MHz Min—60 MHz Max Frequency	—	—	—	—	ns
tAVS	ADDR Valid to MPCLK	3.5	0	—	—	ns
tAPD	MPCLK to ADDR Invalid	—	5	—	—	ns
tCSNSU	CSN Active to MPCLK	3.5	0	—	—	ns
tADSNSU	ADSN Valid to MPCLK	5.5	0	—	—	ns
tSNIPD	MPCLK to ADSN Inactive	—	5	—	—	ns
tDVPD	MPCLK to DTN Valid	—	—	4	16	ns
tDIPD	MPCLK to DTN Invalid	—	—	4	16	ns
tDAIPD	MPCLK to DATA 3-state	—	—	—	10	ns
tADSNDTF	ADSN Valid to DTN Fall	—	—	—	1000*	ns

* Certain registers in the VTMPR block have a very long acknowledge cycle (in the order of 32 MPCK). The reason is that those registers can also be accessed by the VTMPR lower order path overhead interface as part of SONET overhead termination functions. This interface runs at 6.48 MHz. Therefore, the user must insert long enough delay or use the DTN signal in MPU interface to read/write these registers correctly.

5.14.2 Asynchronous Mode

The asynchronous microprocessor interface mode is selected when MPMODE (pin AC18) = 0. Interface timing for the asynchronous mode write cycle is given in Figure 5-12 and in Table 5-39, and for the read cycle in Figure 5-13 and in Table 5-40.



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Figure 5-12. Microprocessor Interface Asynchronous Write Cycle Description (MPMODE (Pin AC18) = 0)

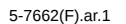
- ADDR [19:0]** Address is asynchronously passed from the host bus to the internal bus. The address will be available throughout the entire cycle.
- DATA [15:0]** Write data is asynchronously passed from the host bus to the internal bus. Data will be available throughout the entire cycle.
- RWN (Input)** The read (H) write (L) signal is always high except during a write cycle.
- CSN (Input)** Chip select is an active-low signal.
- DTN (Output)** Data transfer acknowledge (active-low). DTN is driven asynchronously based on the arrival of CSN. DTN is driven high until the internal transaction is done. DTN is driven high again when either ADSN or DSN is deasserted. DTN will become 3-stated when CSN is high.
- ADSN (Input)** Address strobe is active-low. ADSN must be a minimum of one MPCLK clock period wide.
- DSN (Input)** Data strobe is active-low.

Table 5-39. Microprocessor Interface Asynchronous Write Cycle Specifications

Symbol	Parameter	Typical Interval	Max Interval	Unit
tCSFDSF	CSN Fall to DSN Fall	0	—	ns
tAICSR	ADDR Invalid to CSN Rise	0	—	ns
tAVADSF	ADDR Valid to ADSN Fall	0	—	ns
tADSRAI	ADSN Rise to ADDR Invalid	0	—	ns
tAVDSF	ADDR Valid to DSN Fall	0	—	ns
tDSNRAI	DSN Rise to ADDR Invalid	0	—	ns
trWFDSF	RWN Fall to DSN Fall	0	—	ns
tDSRRWR	DSN Rise to RWN Rise	0	—	ns
tdVDSF	DATA Valid to DSN Fall	0	—	ns
tDSRDI	DSN Rise to DATA Invalid	0	—	ns
tCSFDTR	CSN Fall to DTN Rise	20	—	ns
tDSFDTF	DSN Fall to DTN Fall	120	1000*	ns
tADSRDTR	ADSN Rise to DTN Rise	20	—	ns
tCSRDT3	CSN Rise to DTN 3-state	10	—	ns

* Certain registers in the VTMPR block have a very long acknowledge cycle (in the order of 32 MPCK). The reason is that those registers can also be accessed by the VTMPR lower order path overhead interface as part of SONET overhead termination functions. This interface runs at 6.48 MHz. Therefore, the user must insert long enough delay or use the DTN signal in MPU interface to read/write these registers correctly.

Note: Specifications are valid for 50 MHz MPCLK with MPMODE = 0. Address strobe (ADSN) and chip select (CSN) may be connected and driven from the same source. In this configuration, the setup and hold times for ADSN must be satisfied.



ADDR [19:0] Address is asynchronously passed from the host bus to the internal bus. The address will be available throughout the entire cycle.

DATA [15:0] Read data on the internal bus is only valid for one clock cycle; therefore, a latch is necessary to meet the correct timing on the host bus.

RWN (Input) The read (H) write (L) signal is always high during a read cycle.

CSN (Input) Chip select is an active-low signal.

DTN (Output) Data transfer acknowledge (active-low). DTN is driven asynchronously based on the arrival of CSN, DSN, and ADSN. DTN is driven high while the internal bus transaction is in progress. There is no need to provide synchronization to outgoing signals in this mode. DTN is driven high and then placed in a high-impedance state when either ADSN or DSN is deasserted. DTN will become 3-stated when CSN is high.

ADSN (Input) Address strobe is active-low.

DSN (Input) Data strobe is active-low.

Table 5-40. Microprocessor Interface Asynchronous Read Cycle Specifications

Symbol	Parameter	Typical Interval	Max Interval	Unit
tCSFDSF	CSN Fall to DSN Fall	0 ¹	—	ns
tAICSR	ADDR Invalid to CSN Rise	0	—	ns
tAVADSF	ADDR Valid to ADSN Fall	0	60 ²	ns
tADSRAl	ADSN Rise to ADDR Invalid	0	—	ns
tAVDSF	ADDR Valid to DSN Fall	0	—	ns
tDSNRAl	DSN Rise to ADDR Invalid	0	—	ns
tCSFDTR	CSN Fall to DTN Rise	20	—	ns
tDSFDTF	DSN Fall to DTN Fall	100	1000 ^{3, 4, 7}	ns
tADSRDTR	ADSN Rise to DTN Rise	20 ⁵	—	ns
tCSRDT3	CSN Rise to DTN 3-state	10	—	ns
tDTVdV	DTN Valid to DATA Valid	0 ⁶	—	ns
tADSRD3	ADSN Rise to DATA 3-state	20	—	ns

1. DSN can be asserted up to 20 ns (1 clk at 50 MHz) previous to CSN.
2. ADDR can be asserted up to 60 ns (3 clk at 50 MHz) into cycle from ASDN.
3. DTN fall is variable depending on the block selected for access.
4. Leading edges of ADSN and DSN determine the Fall edge of DTN.
5. Rising edge of ADSN determines the rising edge of DTN.
6. Data toggle 20 ns (1 clk at 50 MHz) previous to CSN.
7. Certain registers in the VTMPR block have a very long acknowledge cycle (in the order of 32 MPCK). The reason is that those registers can also be accessed by the VTMPR lower order path overhead interface as part of SONET overhead termination functions. This interface runs at 6.48 MHz. Therefore, the user must insert long enough delay or use the DTN signal in MPU interface to read/write these registers correctly.

Note: Specifications are valid for 50 MHz MPCLK with MPMODE = 0. Address strobe (ADSN) and chip select (CSN) may be connected and driven from the same source. In this configuration, the setup and hold times for ADSN must be satisfied.

5.15 General-Purpose Interface Timing

Table 5-41. Input Timing Specifications

Input Name	Reference CLK	Min Setup Time (ts)	Min Hold Time (th)	Unit
JTAG Signals				
TDI	TCLK ↑	15.0	2.0	ns
TMSN	TCLK ↑	15.0	2.0	ns
TRSTN	NA	ASYNC	ASYNC	—
SCAN_EN	NA	ASYNC	ASYNC	—
SCAN_MODE	NA	ASYNC	ASYNC	—
Miscellaneous Signals				
RSTN	NA	ASYNC	ASYNC	—
PMRST	NA	ASYNC	ASYNC	—
IC3STATEN	NA	ASYNC	ASYNC	—
IDDQ	NA	ASYNC	ASYNC	—

Table 5-42. Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay* (tPD)		Unit
			Min	Max	
Transmit Signals					
TDO	TLCK ↓	CL = 25 pF	3.0	20.0	ns
Miscellaneous Signals					
PMRST	NA	—	ASYNC	ASYNC	—

* Propagation delay skew, tPLH – tPHL, is ±200 ps.

6 Telecom Bus Operation

6.1 Introduction

This section shows pin descriptions, timing requirements, and timing specifications of the telecom bus.

6.2 Telecom Bus Pin Descriptions

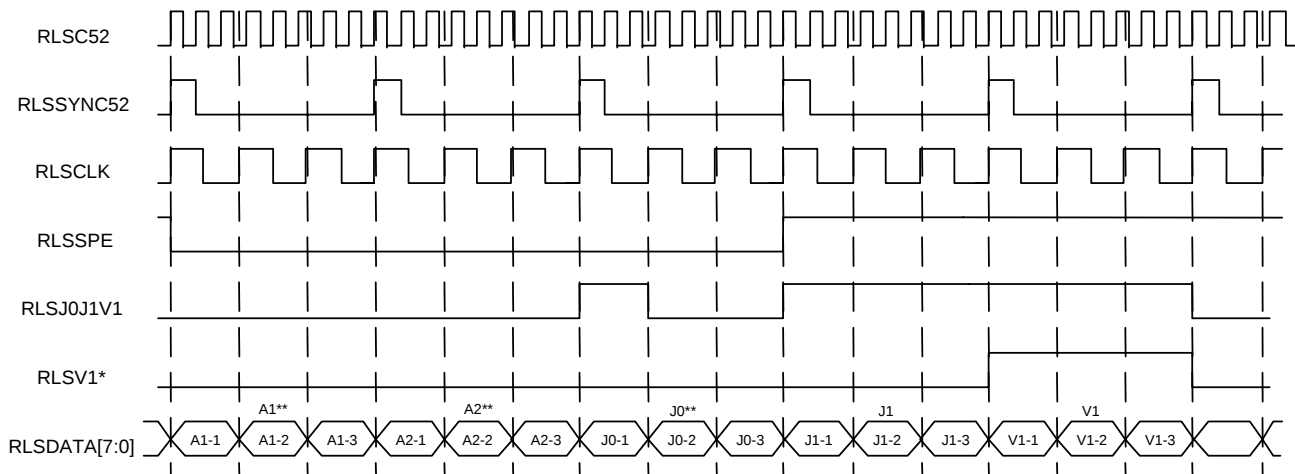
The following is a brief description of the telecom bus pins. The complete pin description can be found in [Table 2-5 on page 17](#).

Table 6-1. Telecom Bus Pins

Pin Name	Description
RLSC52	Receive Low-Speed Clock. An output on the master and input on the slave. This clock is used internally by the SPEMPR and the VTMPR.
RLSSYNC52	Receive Low-Speed Sync. This signal must be synchronous to the RLSC52. An output on the master and an input on the slave. This clock is also used internally by SPEMPR and VTMPR.
RLSCLK	Receive Low-Speed Clock. It is an output on the master and an input on the slave. RLSC52, RLSSYNC52, and RLSCLK must come from the same clocking source. Their timing alignment relationship is showed in Figure 6-1.
RLSSPE	Receive Low-Speed SPE Marker. High, while there are SPE data on the RLSDATA[7:0] output bus and low when there are overhead bytes on the output bus. It is an output on the master and input on the slave
RLSJ0J1V1	Receive Low-Speed J0/J1/V1 Marker. The V1 part of this signal is the same as the RLSV1 pin signal. It is an output on the master and input on the slave.
RLSV1	Receive Low-Speed V1 Marker. As noted in Figure 6-1, the V1 position depends on the H1 and the H2 pointer value. If the pointer value is 522, this signal is high after the three J1 bytes. RLSV1 is high every VT multiframe (superframe). It is an output on the master and an input on the slave.
RLSDATA[7:0]	Receive Low-Speed Data. It is an output data bus on the master and an input on the slave.
RLSPAR	Receive Low-Speed Parity. Bit 2 (register 0x4001B) sets this signal for odd or even parity generation. Bit 7 (register 0x3000B) sets this signal for odd or even parity check. This signal is recommended but not necessary on the telecom bus. It is an output on the master and an input on the slave.
TLSC52	Transmit Low-Speed Clock. An output on the master and an input on the slave. This clock is used by SPEMPR and VTMPR internally.
TLSSYNC52	Transmit Low-Speed Sync. An output on the master and an input on the slave. This clock is also used by SPEMPR and VTMPR internally. This is a 51.84 MHz clock.
TLSCLK	Transmit Low-Speed Clock. It is an output on the master and an input on the slave. The TLSC52, TLSSYNC52, and TLSCLK should come from the same clocking source. Their timing alignment relationship is shown in Figure 6-2.
TLSSPE	Transmit Low-Speed SPE Marker. When it is high, it indicates that the slave device should put the SPE data on the TLSDATA[7:0] output bus. It is an output on the master and input on slave
TLSJ0J1V1	Transmit Low-Speed J0/J1/V1 Marker. The V1 part of this signal is same as RLSV1 pin signal. It is an output on the master and input on slave.
TLSV1	Transmit Low-Speed V1 Marker. The V1 position is fixed as shown in Figure 6-2. It is high every VT multi-frame (superframe). An output on the master and input on slave.
TLSDATA[7:0]	Transmit Low-Speed Data. It is an input data bus on the master and output on the slave.
TLSPAR	Transmit Low-Speed Parity. Bit 9 of register 0x3001B sets this signal for odd or even parity generation. Bit 0 of register 0x40033 sets this signal for odd or even parity check. This signal is recommended but not necessary on the telecom bus. It is an input on the master and an output on the slave.

6.3 Telecom Bus Timing Diagrams

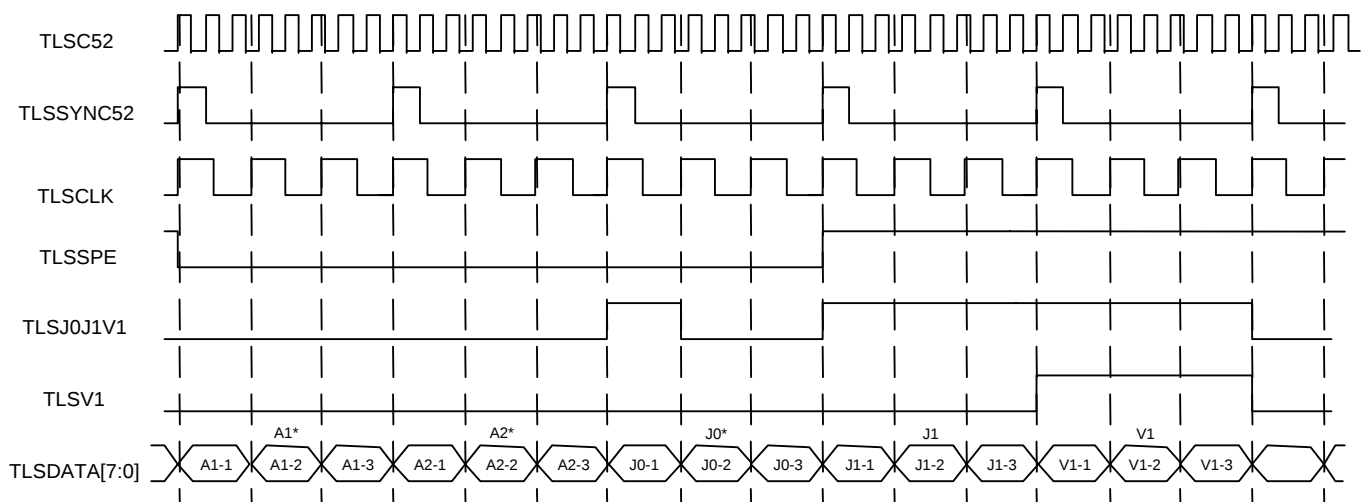
The following diagrams show the telecom bus timing in the receive and the transmit direction.



* The V1 position depends on the H1 and the H2 pointer value. In AU-4/TUG-3 mapping, there is one set of pointer values. In AU-3/TUG-2 mapping, there are three sets of pointer values. This diagram shows the V1 position when the pointer value(s) is (are) 522.

** A1, A2, and J0 bytes are not necessary to be valid bytes.

Figure 6-1. Receive Telecom Bus Timing Diagram for STS-3/STM-1 Signals



* A1, A2, and J0 bytes are not necessary to be valid bytes.

Figure 6-2. Transmit Telecom Bus Timing Diagram for STS-3/STM-1 Signals

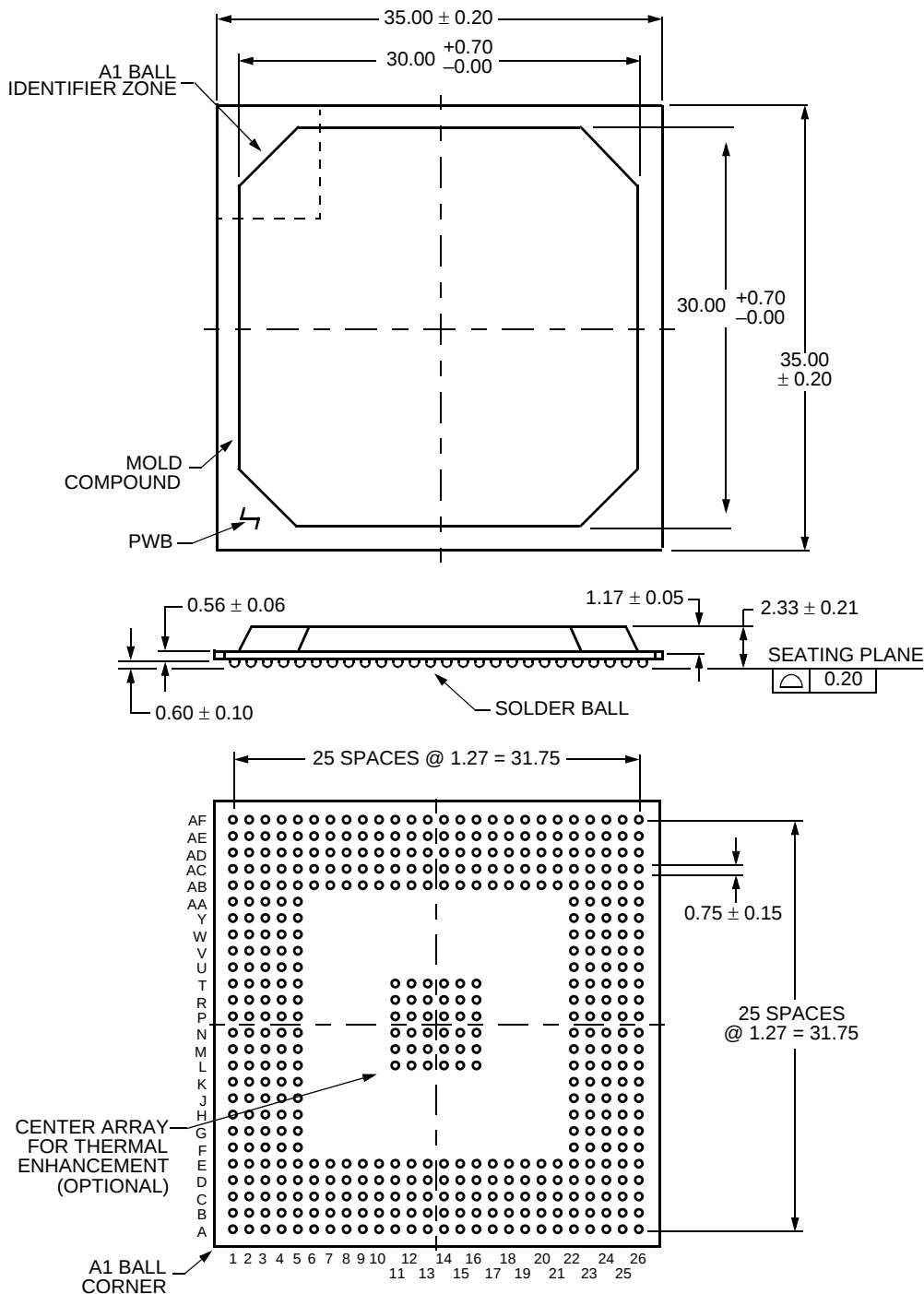
7 Ordering Information

Device	Device Code	Package	Temperature	Comcode
Supermapper V3.1	TMXF281553BAL-3C-DB	456-pin PBGA	−40 °C to +85 °C	700002098
Supermapper V3.2	TMXF281553BAL-C2-DB	456-pin PBGA	−40 °C to +85 °C	700067626

8 Outline Diagram

8.1 456-Pin PBGA

Dimensions are in millimeters.



5-6216(F)r.1

9 Change History

Changes that were made to this document are listed in Table 9-1.

Table 9-1. Document Changes

Change	Change	Change	Change	Change	Change	Change
page 21	page 22	page 23	page 24	page 34	page 42	page 61

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