DATA SHEET

TDF8771A
Triple 8-bit video Digital-to-Analog Converter (DAC)

Product specification

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Philips
Semiconductors

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Triple 8-bit video Digital-to-Analog Converter (DAC)

TDF8771A

FEATURES

- 8-bit resolution
- Sampling rate up to 35 MHz
- Internal reference voltage regulator
- No deglitching circuit required
- Large output voltage range
- 1 kΩ output load
- Power dissipation only 200 mW
- Single 5 V power supply
- 44-pin QFP package
- Operating ambient temperature from –40 to +85 °C.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

GENERAL DESCRIPTION

The TDF8771A is a triple 8-bit video Digital-to-Analog Converter (DAC). It converts the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz.

The DACs are based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.

The device is fabricated in a 5 V, CMOS process that ensures high functionality with low power dissipation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	R_L = 1 kΩ; note 1	10	30	45	mA
I_{DDD}	digital supply current	f_{clk} = 35 MHz	–	3	10	mA
T_{amb}	operating ambient temperature		–40	–	+85	°C
INL	integral non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.3	±1	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.15	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency		35	–	–	MHz
P_{tot}	total power dissipation	R_L = 1 kΩ; f_{clk} = 35 MHz; note 1	45	200	360	mW

Note

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDF8771AH	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

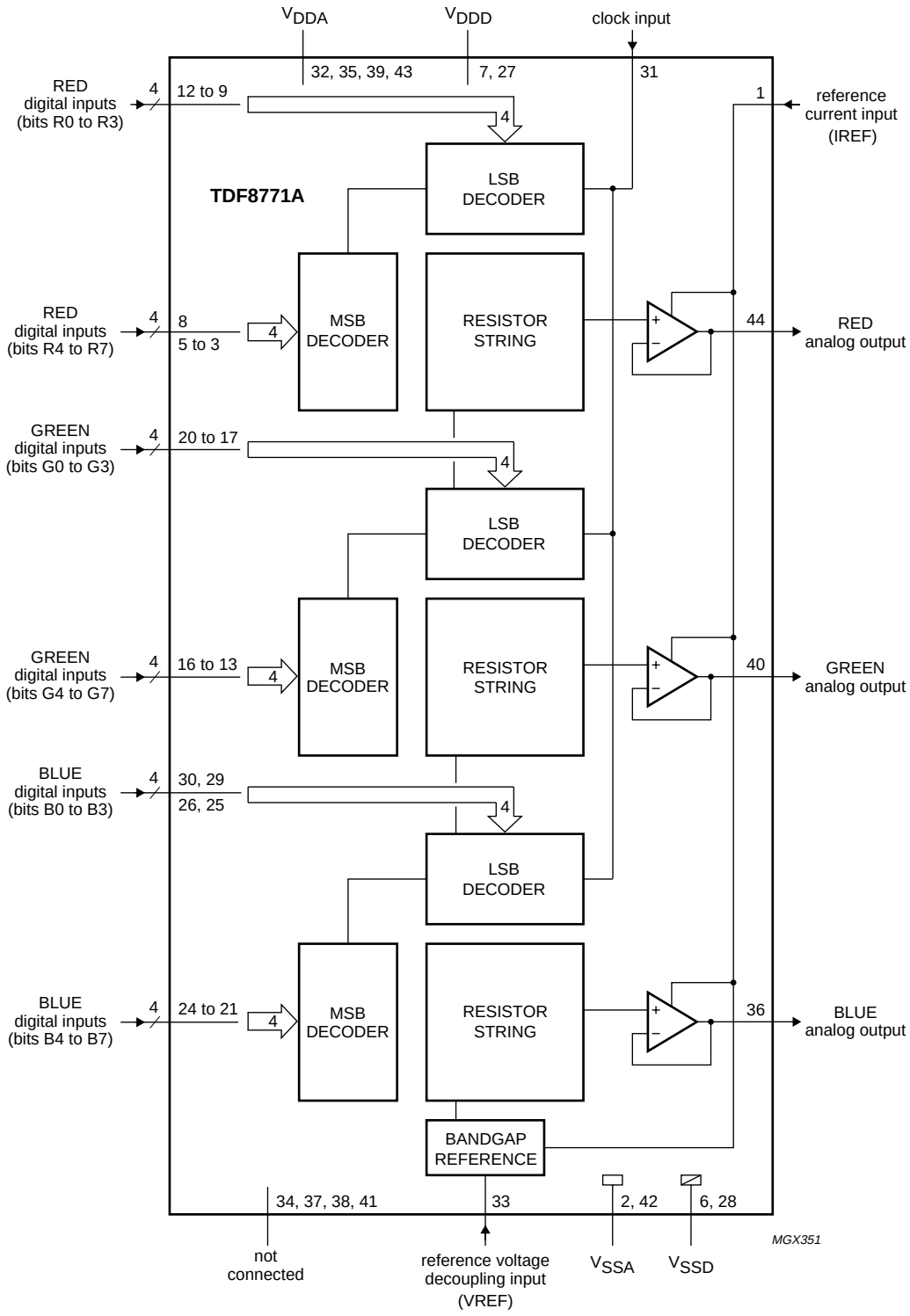


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IREF	1	reference current input for output buffers
V_{SSA1}	2	analog supply ground 1
R7	3	RED digital input data; bit 7 (MSB)
R6	4	RED digital input data; bit 6
R5	5	RED digital input data; bit 5
V_{SSD1}	6	digital supply ground 1
V_{DDD1}	7	digital supply voltage 1
R4	8	RED digital input data; bit 4
R3	9	RED digital input data; bit 3
R2	10	RED digital input data; bit 2
R1	11	RED digital input data; bit 1
R0	12	RED digital input data; bit 0 (LSB)
G7	13	GREEN digital input data; bit 7 (MSB)
G6	14	GREEN digital input data; bit 6
G5	15	GREEN digital input data; bit 5
G4	16	GREEN digital input data; bit 4
G3	17	GREEN digital input data; bit 3
G2	18	GREEN digital input data; bit 2
G1	19	GREEN digital input data; bit 1
G0	20	GREEN digital input data; bit 0 (LSB)
B7	21	BLUE digital input data; bit 7 (MSB)
B6	22	BLUE digital input data; bit 6
B5	23	BLUE digital input data; bit 5
B4	24	BLUE digital input data; bit 4
B3	25	BLUE digital input data; bit 3
B2	26	BLUE digital input data; bit 2
V_{DDD2}	27	digital supply voltage 2
V_{SSD2}	28	digital supply ground 2
B1	29	BLUE digital input data; bit 1
B0	30	BLUE digital input data; bit 0 (LSB)
CLK	31	clock input
V_{DDA1}	32	analog supply voltage 1
VREF	33	decoupling input for reference voltage
n.c.	34	not connected
V_{DDA2}	35	analog supply voltage 2
OUTB	36	BLUE analog output
n.c.	37	not connected
n.c.	38	not connected
V_{DDA3}	39	analog supply voltage 3
OUTG	40	GREEN analog output

SYMBOL	PIN	DESCRIPTION
n.c.	41	not connected
V_{SSA2}	42	analog supply ground 2
V_{DDA4}	43	analog supply voltage 4
OUTR	44	RED analog output

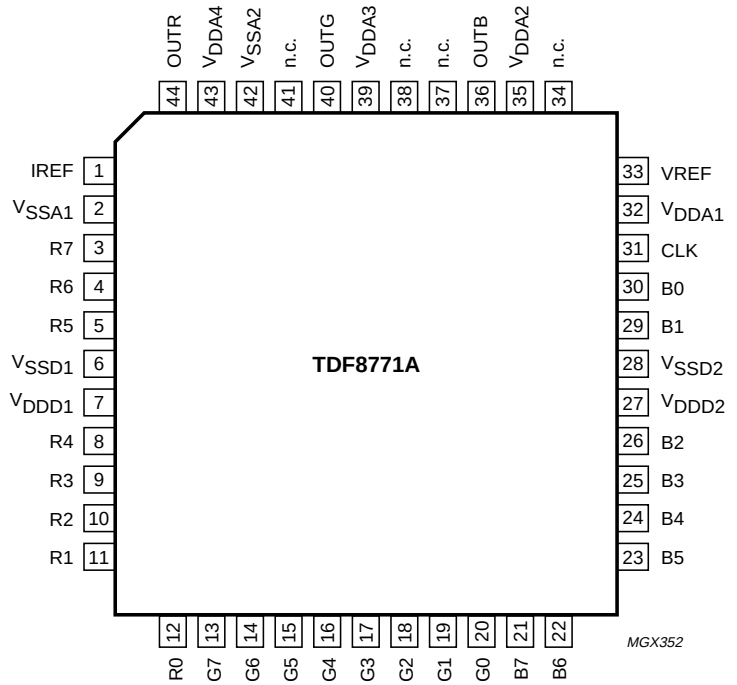


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	–0.5	+6.5	V
V_{DDD}	digital supply voltage	–0.5	+6.5	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}	–1.0	+1.0	V
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C
T_j	junction temperature	–	125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

V_{DDA} = V_{DDD} = 4.5 to 5.5 V; V_{SSA} and V_{SSD} shorted together; V_{DDA} − V_{DDD} = −0.5 to +0.5 V; T_{amb} = −40 to +85 °C; typical values measured at V_{DDA} = V_{DDD} = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	R_L = 1 kΩ; note 1	10	30	45	mA
I_{DDD}	digital supply current	f_{clk} = 35 MHz	–	3	10	mA
Inputs						
CLOCK INPUT (PIN 31)						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
R, G, B DIGITAL INPUTS (PINS 12 TO 8, 5 TO 3, 20 TO 13, 30, 29 AND 26 TO 21)						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
REFERENCE CURRENT INPUT FOR OUTPUT BUFFERS (PIN 1)						
I_I	input current		–	0.6	0.7	mA
Timing; see Fig.3						
$f_{clk(max)}$	maximum clock frequency		35	–	–	MHz
t_{CPH}	clock pulse width HIGH		9	–	–	ns
t_{CPL}	clock pulse width LOW		9	–	–	ns
t_r	clock rise time		–	–	6	ns
t_f	clock fall time		–	–	6	ns
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		4	–	–	ns
Voltage reference (pin 33, referenced to V_{SSA})						
V_{VREF}	reference voltage		1.180	1.238	1.305	V
Outputs						
OUTB, OUTG, OUTR ANALOG OUTPUTS (PINS 36, 40 AND 44, REFERENCED TO V_{SSA}) FOR 1 kΩ LOAD; see Table 1						
FSR	full-scale output voltage range		2.80	3.00	3.18	V
V_{os}	offset of analog voltage output		–	0.33	–	V
$V_{O(max)}$	maximum output voltage	data inputs = logic 1; note 2	2.95	3.30	3.52	V
$V_{O(min)}$	minimum output voltage	data inputs = logic 0; note 2	0.05	0.25	0.45	V
THD	total harmonic distortion	f_i = 4.43 MHz; f_{clk} = 35 MHz	–	−47	–	dB
Z_L	output load impedance		0.9	1.0	1.1	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transfer function (f_{clk} = 35 MHz)						
INL	integral non-linearity	ramp input	–	±0.3	±1	LSB
DNL	differential non-linearity	ramp input	–	±0.15	±0.5	LSB
α_{ct}	crosstalk DAC to DAC		–50	–	–	dB
M_{DAC}	DAC to DAC matching		–	1.0	2.8	%
Switching characteristics (for 1 kΩ output load); see Fig.4						
t_d	input to 50% output delay time	full-scale change	–	12	–	ns
t_{s1}	settling time	10% to 90% of full-scale change	–	15	–	ns
t_{s2}	settling time	to ±1 LSB	–	50	–	ns
Output transients (glitches)						
V_g	area for 1 LSB change		–	1	–	LSB·ns

Notes

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.
2. V_O is directly proportional to V_{VREF}.

Table 1 Input coding and DAC output voltages (typical values)

BINARY INPUT DATA (SYNC = BLANK = 0)	CODE	DAC OUTPUT VOLTAGES (V) OUTB, OUTR, OUTG R_L = 1 kΩ
0000 0000	0	0.262
0000 0001	1	0.273
to	to	to
1000 0000	128	1.731
to	to	to
1111 1110	254	3.188
1111 1111	255	3.200

TIMING

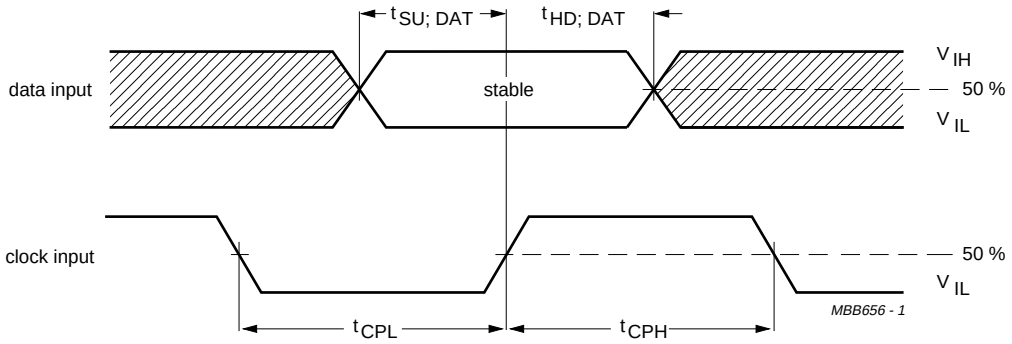


Fig.3 Input timing.

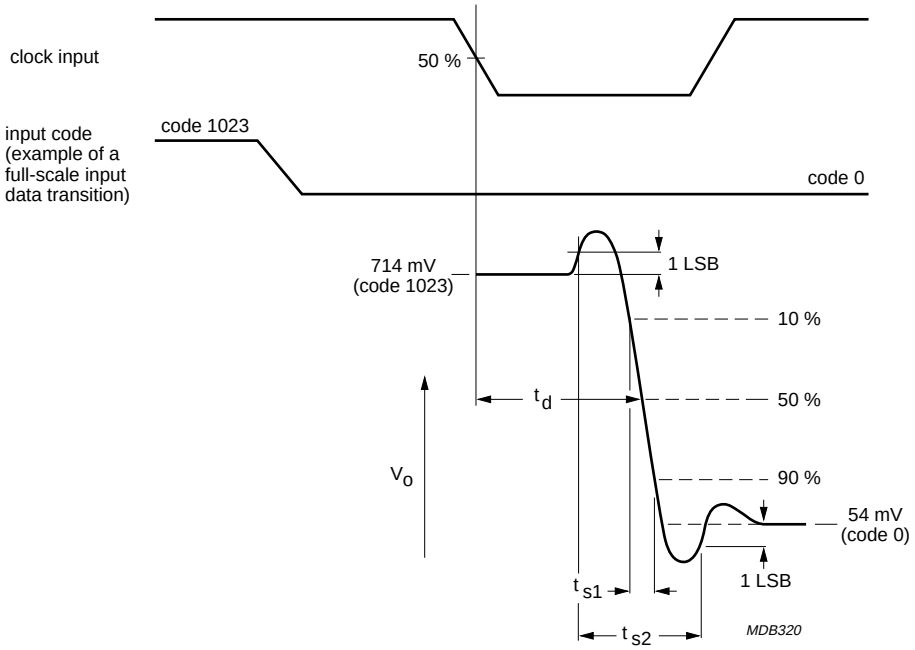
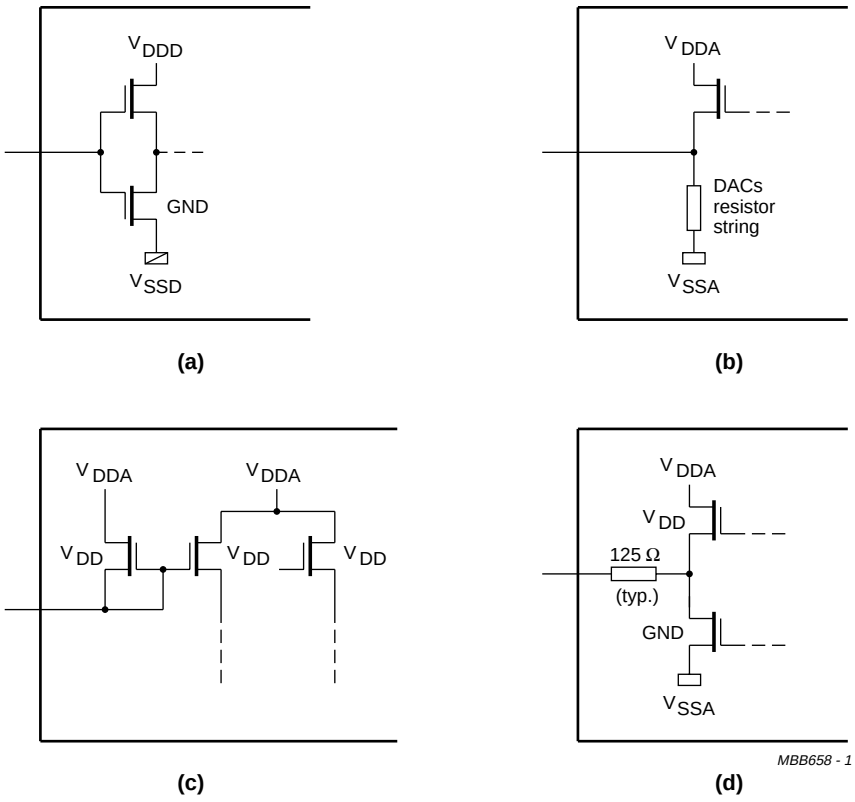


Fig.4 Switching timing.

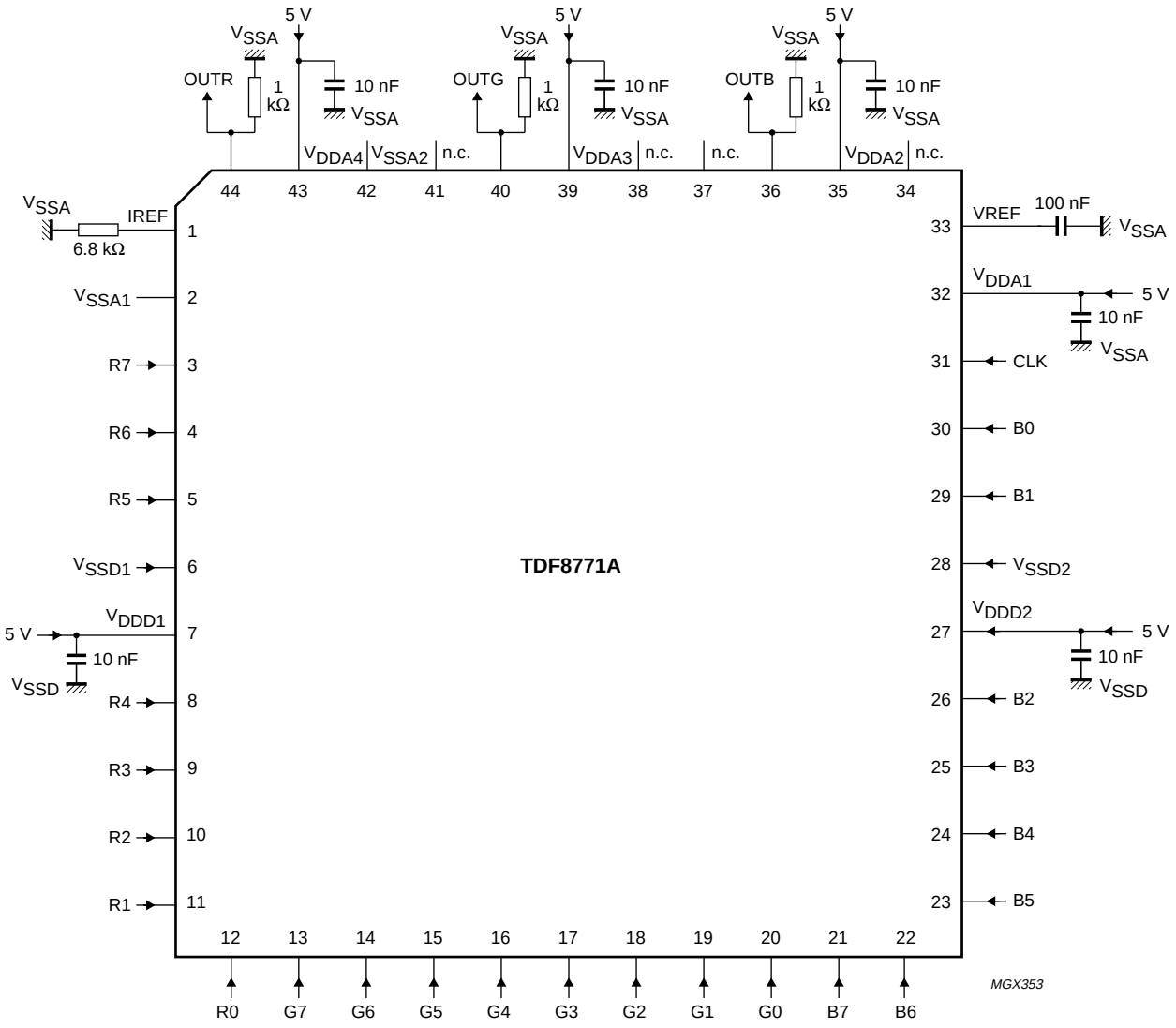
INTERNAL CIRCUITRY



(a) Digital inputs; pins 3 to 5, 8 to 26 and 29 to 31.
(b) Pin VREF (pin 33).
(c) Pin IREF (pin 1).
(d) Pins OUTB, OUTG and OUTR (pins 36, 40 and 44).

Fig.5 Internal circuitry.

APPLICATION INFORMATION



Analog and digital supplies should be separated and decoupled.
Supplies are not connected internally.
All ground pins must be connected. One ground plane is preferred although it depends on application.
See Figs 7 and 9 for example of anti-aliasing filter.

Fig.6 Application diagram.

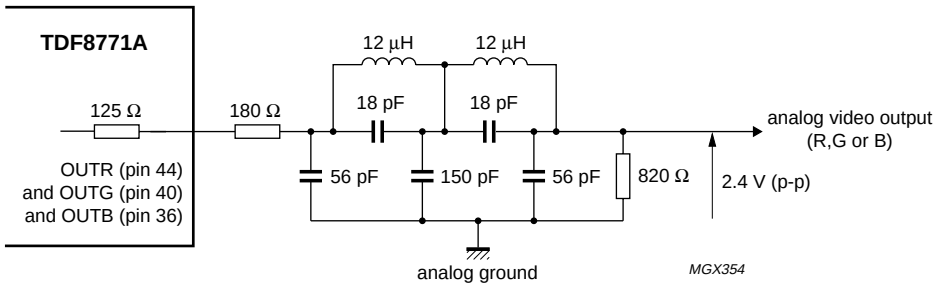


Fig.7 Example of anti-aliasing filter for 2.4 V output swing.

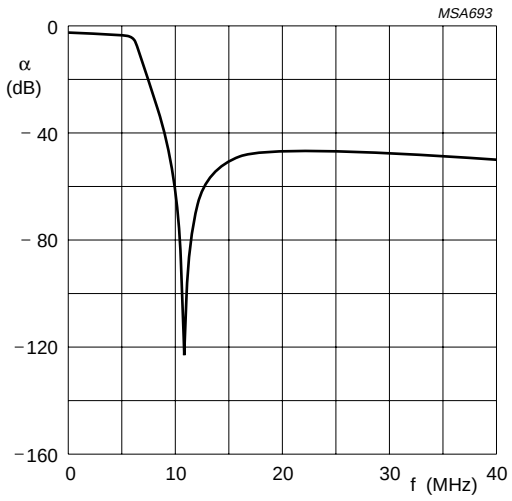


Fig.8 Frequency response for filter shown in Fig.7.

Characteristics of Fig.8

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \geq 0.7$ dB
- f at −3 dB = 6.2 MHz
- f_{NOTCH} = 10.8 MHz.

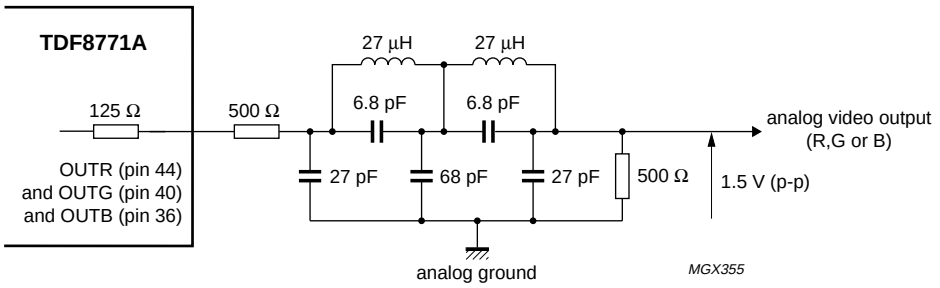


Fig.9 Example of anti-aliasing filter for 1.5 V output swing.

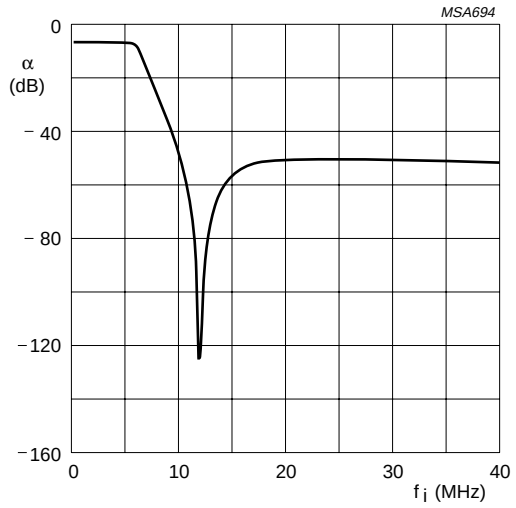


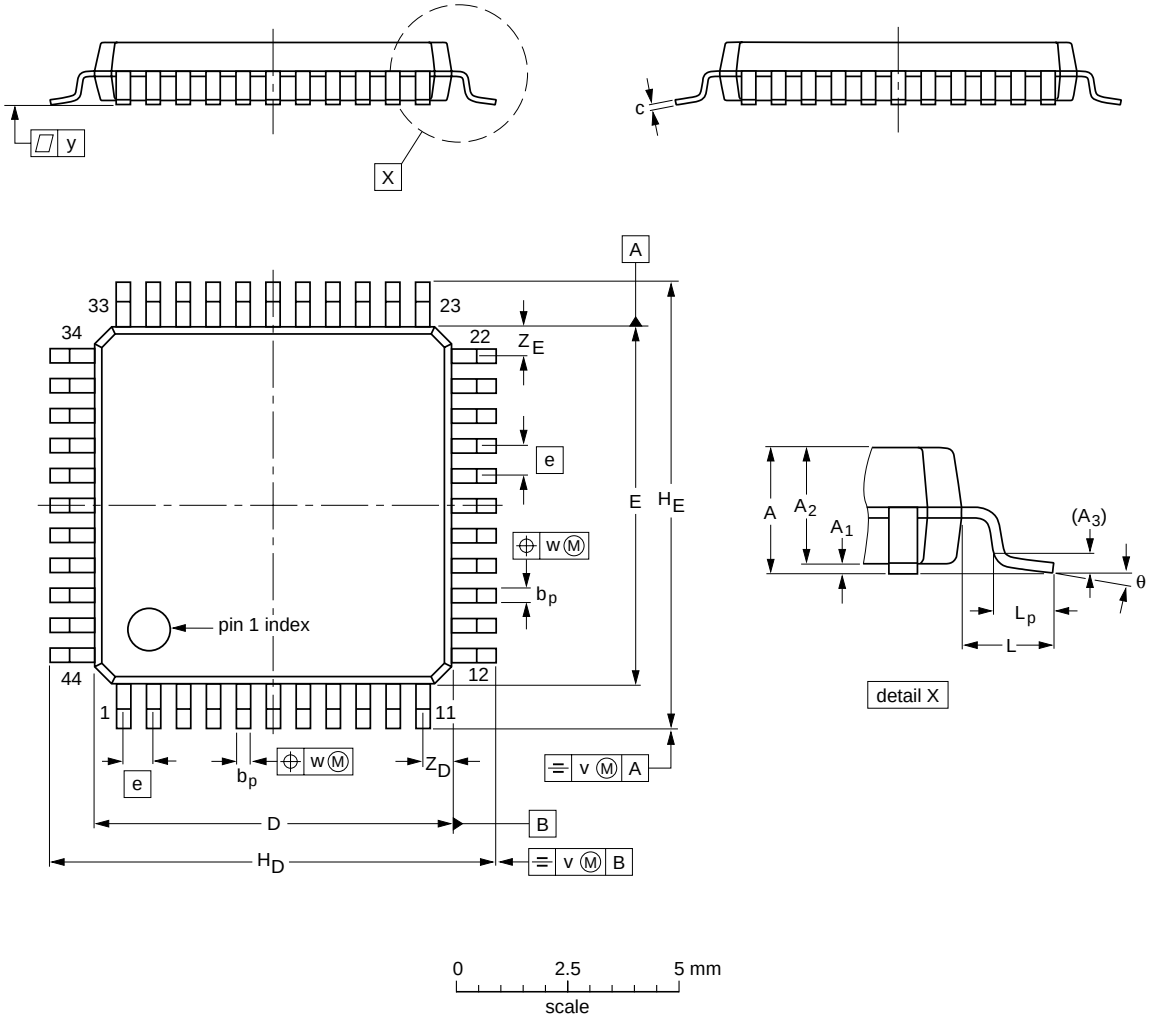
Fig.10 Frequency response for filter shown in Fig.9.

Characteristics of Fig.10

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \geq 0.25$ dB
- f at −3 dB = 5.6 MHz
- f_{NOTCH} = 11.7 MHz.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.1	0.25 0.05	1.85 1.65	0.25	0.4 0.2	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT307-2						~~97-08-01~~ 03-02-25

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept:

- below 220 °C for all the BGA packages and packages with a thickness ≥ 2.5mm and packages with a thickness <2.5 mm and a volume ≥350 mm^3 so called thick/large packages
- below 235 °C for packages with a thickness <2.5 mm and a volume <350 mm^3 so called small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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